Development of device isolation technologies for GaN-based field-effect transistors

窒化ガリウムトランジスタにおける

素子間分離技術の研究

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Abstract

Gallium nitride (GaN) semiconductor has the great advantage in the application of high-temperature and high-frequency power electronic devices owing to its unique properties, such as wide band-gap, high electron saturation velocity, high breakdown field and high electron conductivity of the two-dimensional electron gas (2DEG) in AlGaN/GaN heterostructure. AlGaN/GaN heterojunction field-effect transistor (HFET) and GaN metal-oxide-semiconductor field-effect transistor (MOSFET) are the classic devices of GaN-based field-effect transistors (FETs), which can be applied to microwave amplifying devices for wireless communication, military radar and power conversion devices for motor inverter. Device isolation is one of the primary processes for the fabrication of GaN-based FETs, and mesa structure is often adopted for device isolation through dry etching. However, dry etching damages increases high surface leakage current of the mesa-isolated region, leading to a high off-state current and power loss of AlGaN/GaN HFET. For the mesa-isolated linear GaN MOSFET, field isolation is impossible because a parasitic MOSFET exists in the mesa-isolated region, which widens the effective channel width, resulting in an overestimated mobility. Hence, developing the device isolation processes for AlGaN/GaN HFETs, field isolation processes for GaN MOSFET, and evaluating the isolation effectiveness of these processes are essential for GaN-based FETs.

In this thesis, evaluation technology of isolation effectiveness was investigated on the basic of fabrication processes and test methods for AlGaN/GaN HFET and GaN MOSFET. The effective O_2 plasma treatment process was established, the oxidation mechanism was analyzed, and isolation effectiveness of AlGaN/GaN HFETs with O_2 plasma treatment were characterized and evaluated. The boron field implantation for GaN MOSFET was developed, the elimination of the parasitic MOSFET in the isolation region was examined using electrical testing of several MOSFET structures, and the field isolation effectiveness of GaN MOSFET and the influence of implantation damage on device performance for different isolation structures were characterized and evaluated. The contents and conclusions of this thesis are as follows:

In chapter 2, the basic fabrication processes, test methods and evaluation technology of isolation effectiveness for AlGaN/GaN HFET and GaN MOSFETs were studied. On the basis of the fabrication processes of GaN-based FETs, device performances were characterized through the current-voltage (*I*–*V*) and capacitance-voltage (*C*–*V*) measurements, and the processes isolation effectiveness was evaluated through the transmission line model (TLM) structure and special MOSFETs fabricated in the isolation regions. In the TLM structure, the regions between every two ohmic electrodes were formed by different isolation processes, and the processes isolation effectiveness were evaluated by sheet resistance measurements or *I*–*V* characteristics of these regions. The circular MOSFETs were fabricated in the isolation regions to examine the existence of a parasitic MOSFET by *I*–*V* characteristics. The circular and linear MOSFETs with same fabrication processes were fabricated, the effectiveness of isolation

processes was evaluated through comparing their transfer characteristics, and the effect of field implantation on device performance was investigated through calculating the field-effect electron mobility and the density of interface traps (D_{it}) at SiO_2/GaN interface.

In chapter 3, the isolation effectiveness and oxidation mechanism of O_2 plasma treatment for AlGaN/GaN HFETs were studied. The process of O_2 plasma treatment on the mesa-isolated region of AlGaN/GaN HFETs was adopted, the optimal condition was established by *I–V* measurement on TLM structure, the oxidation effectiveness and mechanism of the mesa etching surface were analyzed through photoluminescence (PL) spectrum and X-ray photoelectron spectroscopy (XPS), and AlGaN/GaN HFETs with O_2 plasma treatment were fabricated and characterized. The *I–V* results of TLM structure indicated that the isolation current were strongly dependent on treatment temperature and the depth of etching damage. Treatment at 300 ℃ was confirmed to be the optimal condition, under which isolation current was reduced by four orders of magnitude to 10^{-11} A and photovoltaic response was suppressed, and the breakdown voltage of the mesa-isolated region increased from 171.5 to 467.2 V. The PL spectrum analysis showed a decrease in the density of defects related to the yellow luminescence band and the occurrence of defects related to the blue luminescence band. XPS results showed that O_2 plasma treatment can form high amounts of Ga_2O_3 than O_2 gas treatment, and the defect of substitutional oxygen on the nitrogen site was probably formed. The —*V* characteristics of AlGaN/GaN HFETs presented a high on/off drain current ratio of 1.73×10^{7}.

In chapter 4, the isolation effectiveness and influence of implantation damage on device performance for boron ion implantation process in GaN MOSFETs were studied. The process of boron field implantation was developed and improved for GaN MOSFETs, the elimination of parasitic MOSFETs was confirmed by the *I–V* characteristics of circular MOSFETs fabricated in the isolation regions, and isolation effectiveness of process was evaluated through the comparison of *I–V* characteristics between circular and linear device. The influence of implantation damage on device performance for different isolation structures were evaluated by the field-effect electron mobility and D_{it} according to *I–V* and *C–V* tests. The process of boron field implantation was altered and subsequently conducted after all the high-temperature processes, and implanted regions with high resistivity were achieved. The circular MOSFET fabricated in the isolation region presented an extremely low drain current of 7×10^{-8} mA/mm, demonstrating that the parasitic MOSFET in the isolation region was eliminated by boron field implantation. The off-state drain current of the linear MOSFET was reduced from 3×10^{-5} mA/mm of mesa isolation to 6×10^{-7} mA/mm of boron field implantation, which was only one order of magnitude higher than the 7×10^{-8} mA/mm of the circular device. Field isolation for GaN MOSFETs succeeded. The calculation of the field-effect electron mobility showed that implanting did not deteriorate the mobility. The D_{it} results indicated that the isolation structure of both mesa and implantation did not influence the interface state density.

Key words: Gallium nitride; device isolation; field isolation; AlGaN/GaN HFET; GaN MOSFET

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Chapter 1 Introduction

1.1 Material advantages of GaN

Since the 1950s, after the initial replacement of vacuum tubes by solid-state devices, semiconductor power devices have taken a dominant role with silicon serving as the base material and started the Second Electronic Revolution. However, silicon reached its limitation of physic property after decades of development. Gallium nitride (GaN) as a member of wide band-gap semiconductors has been viewed as a promising candidate to fulfill the requirements of high-frequency, wide bandwidth, high-temperature, and high power in the applications of automobile, wireless communications, military radar.

1.1.1 Material growth and properties

It is widely believed that Johnson *et al.* [1] first reported on the synthesis of GaN via the reaction of metallic Ga and NH_3 stream in 1932. For early GaN investigations of 1960s and 1970s, only the growth of GaN powder [2-8] and single crystalline GaN needles [9-11] could be achieved, and the popular epitaxial film growth methods were reactive sputtering [12-16], chemical vapor deposition (CVD) [17-22] and reactive molecular beam epitaxy (RMBE) [23]. The first large area GaN was formed on sapphire substrate through the hydride vapor phase epitaxy (VPE) method reported by H.P. Maruska et al in 1969, using flowing HCl vapor over metallic Ga, causing the formation of GaCl which was transported downstream and reacted with NH_3 [24]. However, GaN grown by this approach had large n-type background carrier concentrations, typically 10^{19} cm^{-3}. The origin of centers that give rise to background n-type conductivity is conflicting between nitrogen vacancies [25, 26] and residual impurities such as O and Si [27, 28]. Due to the compensation of n-type background carrier, the p-type doping in GaN was difficult. Until 1989, H. Amano et al [29] initially realized p-type conduction with Mg-doped GaN by the low-energy electron-beam irradiation (LEEBI) treatment and the hole concentration was 2×10^{16} cm^{-3}. In 1991, S. Nakamura et al [30, 31] succeeded in growing p-type GaN using MOCVD.

Another difficulty hindered the growth of high-quality GaN film was the lack of substrate material. Although so many years' efforts were expended to grow GaN and develop devices, high-quality, large single crystalline and cost-effective GaN native substrate are now in progress. Crystals are generally grown from liquid phase or gas phase. The challenges to the liquid-phase growth of GaN bulk crystal are **1)** the high vapor pressure of N on GaN for melt-grown crystal techniques [32-34], as shown in Figure 1.1; **2)** the low solubility of N in the Ga metal melts at

reasonable temperatures and pressures for solution-grown techniques [35-37]. Accordingly, the vapor-phase growth is widely used for epitaxial film growth of GaN due to its inherently slow growth rate.

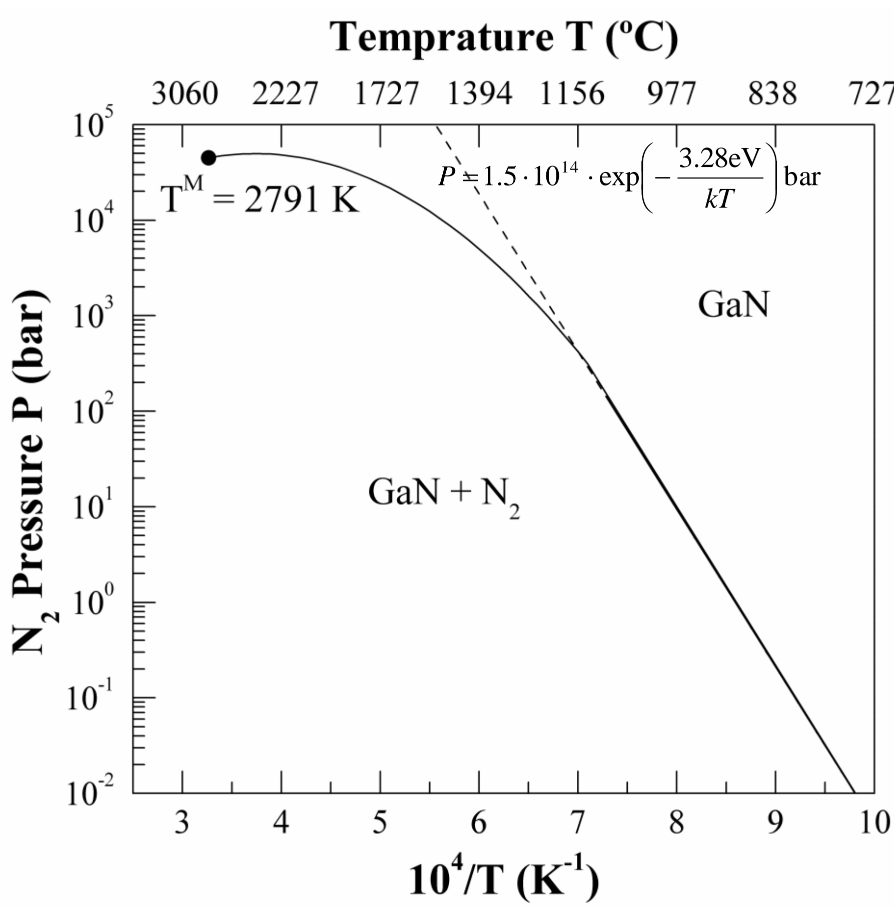


Figure1. 1 Equilibrium N_2 pressure over GaN(s) + Ga(l) system based on Ref. [32] and melting points TM from Ref. [34]. The dashed line was calculated for ideal gas [38] and the solid line was fitted with experimental data.

The preference of substrates towards sapphire could be attributed to hexagonal symmetry, simple pre-growth cleaning, and the stability under high concentrations of ammonia and hydrogen at high-temperature. But good epitaxial films could not be obtained due to the lattice mismatch as well as thermal mismatch between the GaN and sapphire until the late 1980s. S. Yoshida et al [23, 39] reported the initially deposition of AlN buffer layer on the sapphire, H. Amano et al [40] and I. Akasaki et al [41] obtained high-quality GaN epitaxial films using AlN buffer layer via metalorganic chemical vapor deposition (MOCVD), S. Nakamura et al [42] first reported the GaN epitaxial film with an n-type background concentration of 4×10^{16} cm^{-3}

using the GaN buffer layer. 6H-SiC and Si are also popular substrates: the former has a low lattice mismatch, good electrical conductivity and low film stress; the later has large wafer size, low cost and integration of Si devices. Nowadays, GaN wafers using sapphire, 6H-SiC and Si as substrate have been commercial available, which gives support to the wide range of electronic and optoelectronic applications.

GaN semiconductor has great application potential in high-power and high-frequency electronic devices because of its excellent material properties, such as wide band-gap, high electron saturation velocity, high breakdown field and high electron conductivity of the two-dimensional electron gas (2DEG) in AlGaN/GaN heterostructure. Table 1.1 summarized the material properties of GaN and other semiconductor.

Table 1. 1 Material properties of GaN and other semiconductor [43].

Material properties	Si	GaAs	4H-SiC	**GaN**	GaN
Crystal structure	Diamond	Zincblende	Hexagon	**Wurtzite**	Zincblende
Band-gap E_g (eV) 300 K	1.12	1.42	3.23	**3.39**	3.2
Breakdown field E_B (MV/cm)	0.25-0.8	0.3-0.9	3~5	**5**	5
Electron mobility μ_n (cm^2·v^{-1}·s^{-1})	1450	8000	≤900	**≤1000**	≤1000
Hole mobility μ_p (cm^2·v^{-1}·s^{-1})	500	400	≤120	**≤200**	≤350
Saturation electron velocity v_s (10^{7}cm/s)	1	0.7	1.9	**2.5**	2.5
Thermal conductivity χ (W·cm^{-1}·K^{-1})	1.56	0.46	3.7	**1.3**	1.3
Intrinsic carrier concentration n_i (cm^{-3}) 300K	9.65×10^9	2.1×10^6	8.2×10^{-9}	**3.85×10^{-10}**	1.04×10^{-8}

The band-gap of GaN (wurtzite structure) is 3.4 eV, which is three times larger than Si. The wide band-gap gives rise to a low intrinsic carrier concentration, which means GaN devices

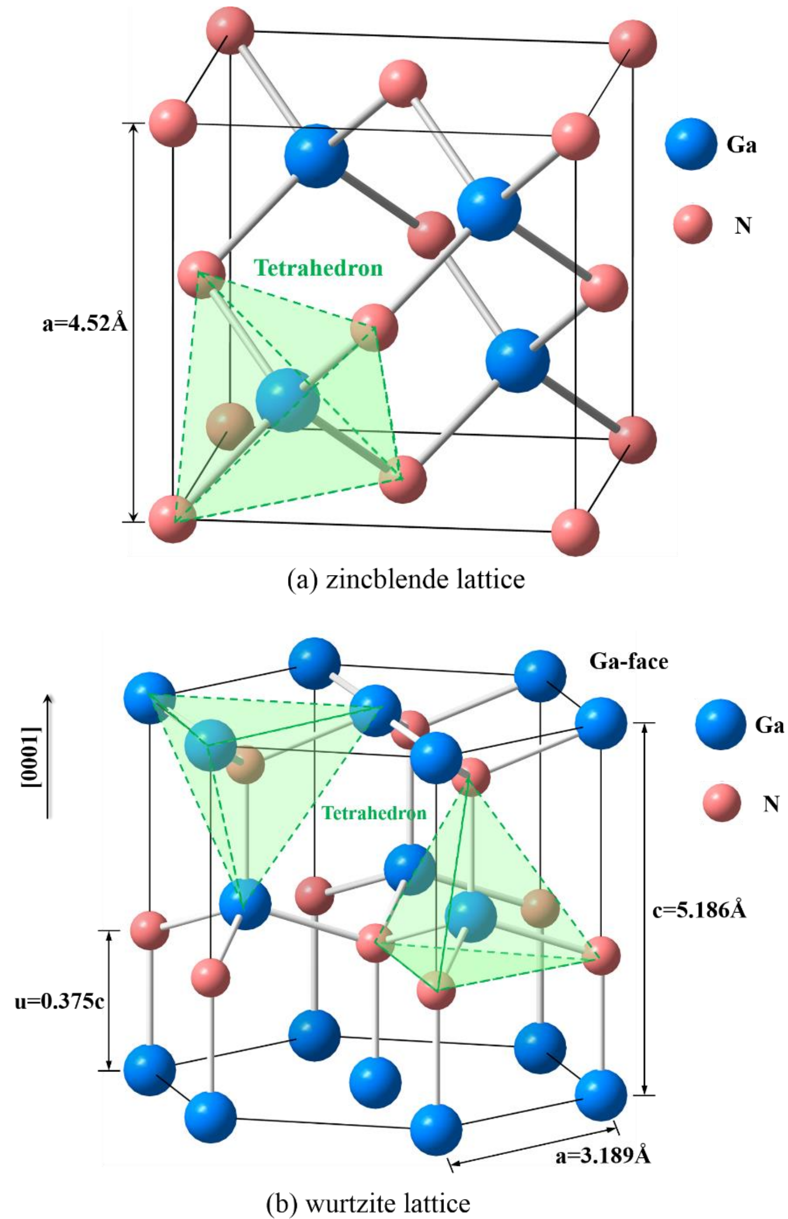
need to operate at higher temperature to reach the same intrinsic carrier concentration of Si at room temperature, namely, GaN-based devices can work at harsh temperature environment. GaN-based devices can also work at high voltage because the breakdown field of GaN is much higher than Si and GaAs. The high electron velocity characteristics make GaN devices operate at high frequency as well. In addition, as a direct wide band-gap semiconductor, GaN plays an important role in optoelectronics devices, such as green and short wavelengths emitters and detectors.

1.1.2 Crystal structure

GaN as III-N based semiconductors exist under different crystal structures, wurtzite, zincblende and rock-salt [44]. In general, as ambient conditions, for III-N based semiconductors wurtzite structure is thermodynamically stable; zincblende structure is thermodynamically metastable, while rock-salt structure is formed only under high pressure. GaN films of wurtzite structure have been grown on *c*-orientation substrates which generally transfer their hexagonal symmetry to GaN, such as (0001) sapphire or (0001) 6H-SiC. GaN films of zincblende structure can be stabilized by epitaxial growth on substrates of cubic structure, such as (001) GaAs, (001) 3C-SiC or (001) Si substrate. In this thesis, GaN samples involved in all the experiments are under wurtzite structure.

Both of zincblende and wurtzite structure have tetrahedral coordination: each atom is surrounded by four equidistant nearest neighbors which lie at the corners of a regular tetrahedron. The main difference between these two close-packed structures is the layer stacking sequence: for the zincblende structure, the stacking sequence of (1111) layers is ABCABCABC... along the <111> direction; for the wurtzite structure, the stacking sequence of (0001) layers is ABABAB... along the <0001> direction.

Figure1.2 shows the wurtzite and zincblende lattice structure of GaN. The zincblende lattice consists of two interpenetrating face-centered cubic (fcc) sub-lattice with the same dimension of lattice constant a=4.52Å [43]. One sub-lattice is gallium and the other is nitrogen, each sub-lattice are shifted against each other along the body diagonal of cubic cell by 1/4 of the width of the unit cell (Figure 1.2 (a)). The wurtzite structure has a hexagonal unit cell and consists of two interpenetrating hexagonal close-packed (hcp) sub-lattice, which constituted by gallium and nitrogen atoms respectively. The wurtzite structure is defined by two lattice constant, a=3.189Å, c=5.186Å, as shown in Figure 1.2 (b). Each sub-lattice are shifted against each other along the *c*-orientation (i.e. [0001] direction) by the distance u= (3/8) c=0.375c.



(a) zincblende lattice

(b) wurtzite lattice

Figure1. 2 Illustration of (a) zincblende lattice and (b) Gallium-face wurtzite lattice of GaN.

1.1.3 Polarization effects and 2DEG

The most unique feature of GaN-based semiconductor is the formation of high density of 2DEG in a quantum well along a heterojunction. The heterojunctions are commonly achieved by the use of alloys, and GaN is commonly alloyed with AlN to form AlGaN. The band-gap and resistivity of $Al_xGa_{1-x}N$ increase as a function of the Al mole fraction, while the carrier concentration and hall mobility decrease [45]. As shown in Figure 1.3, the band-gap of AlGaN is wider than that of GaN, the carrier accumulation would occur at the interface of AlGaN/GaN heterostructure.

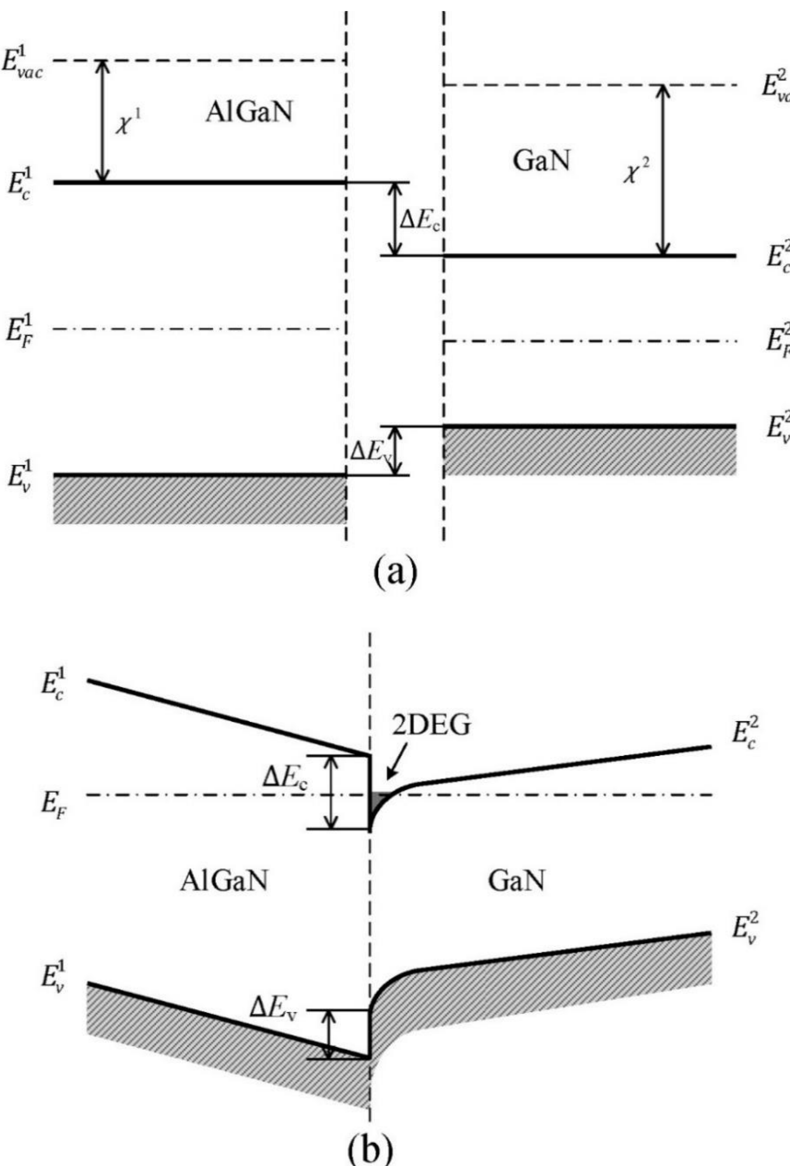


Figure1. 3 Band diagram of (a) seperating AlGaN and GaN; (b) the AlGaN/GaN heterostructure.

Unlike the 2DEG formation of AlGaAs/GaAs heterostructure, in which the electrons are mainly provided by the dopants in AlGaAs and GaAs. The high density of 2DEG in AlGaN/GaN heterojunction is induced by polarization effects. This sheet density of 2DEG in AlGaN/GaN is up to 1×10^{13} cm^{-2} without intentional doping. The polarization effects cause extremely strong electric field within the heterojunction, which would modulate the band structure and make the quantum well of GaN side deep and narrow, and this is benefit to attract and accumulate free electrons into the well.

Group III-N based semiconductor exist stronger spontaneous polarization and piezoelectric polarization comparing with other group III–V based semiconductor. Zincblende

group III–V compounds present no spontaneous polarization because lattice structure symmetry counteracts the polarization of covalent bonding. While wurtzite group III–V compounds present a spontaneous polarization along the c-axis direction. Both of structures present piezoelectric polarization. At an abrupt interface of a top/bottom layer heterostructure, the changes of polarization field within a bilayer would induce a sheet charge density σ defined by

$$\sigma = P_{Top} - P_{Bottom} \quad (1.1)$$

where P is polarization intensity [46]. If this sheet charge density is positive (+σ), free electrons will compensate this charge and form a 2DEG. If the sheet charge density is negative (−σ), holes would accumulate.

In general, Ga-face polarity is obtained in smooth morphology GaN films grown by MOCVD and N-face polarity is obtained in high-quality GaN films grown by molecular beam epitaxy (MBE). And the polarity of Ga-face wurtzite GaN is opposite to N-face wurtzite GaN, which would alter the sheet charge density's properties of positive or negative. Therefore, for Ga-face AlGaN on top of GaN heterostructure grown pseudo orphic, as shown in Figure 1.4, σ is positive and determined by

$$\sigma = P_{Top} - P_{Bottom} = \left(P_{SP,AlGaN} + P_{PE,AlGaN}\right) - P_{SP,GaN} \quad (1.2)$$

where P_{SP} and P_{PE} is intensity of spontaneous polarization and piezoelectric polarization, respectively.

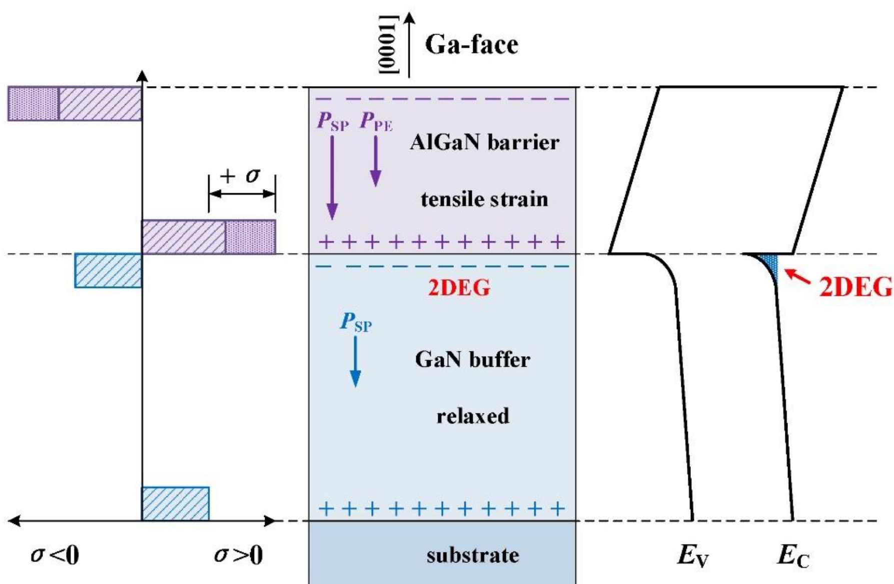


Figure1. 4 Scheme of sheet charge density, polarization directions and conduction band diagram of Ga-face AlGaN/GaN heterostructures.

1.2 Overview of GaN-based field-effect transistors

GaN-based power transistors can be generally divided into two categories: one is linear device for power amplification at high frequencies such as AlGaN/GaN heterojunction field-effect transistor (HFET); the other is switching power device for electricity conversion such as GaN metal-oxide-semiconductor field-effect transistor (MOSFET). This thesis mainly takes aim at AlGaN/GaN HFET and GaN MOSFET. After more than 20 year's efforts, remarkable progress in development of GaN-based field-effect transistors (FETs) has been achieved.

1. 2. 1 AlGaN/GaN HFET

The AlGaN/GaN HFET is based on AlGaN/GaN heterostructure. The field-effect transistor formed on the AlGaN/GaN heterostructure and using 2DEG as the channel is called AlGaN/GaN high electron mobility transistors (HEMTs). The mobility of AlGaN/GaN HEMTs is enhanced due to the high density of 2DEG, and up to 2000 $cm^2 \cdot v^{-1} \cdot s^{-1}$ [47]. AlGaN/GaN HEMT with impressive tradeoff between specific on-resistance and breakdown voltage is regarded as one of the prospective candidates for the next generation of microwave power devices.

In 1993, M. A. Khan et al fabricated the first GaN metal semiconductor field-effect transistor (MESFET) with a gate length of 4 μm and a maximum transconductance of 23 mS/mm at gate voltage of -1 V [48]. Subsequently, they reported the first fabrication of HEMT based on AlGaN/GaN heterojunction with a transconductance of 28 mS/mm at 300 K [49]. By means of a new ohmic contact using Ti/Al reported by M.E. Lin et al [50], several kinds of device structures were proposed. A. Ozgur et al fabricated GaN modulation-doped FETs (MODFETs) with a transconductance of 120 mS/mm and a 300 mA/mm current at gate bias of 3 V [51]. M.A. Khan et al fabricated doped-channel HFETs (DC-HFETs) with a gate length of 0.25 μm and obtained a cutoff frequency of 70.8 GHz [52]. In this period, the major obstacle to device improvement was poor crystal quality and poor thermal environment. Not until high-quality GaN films epitaxially grown on SiC substrate succeeded did the device fabrication technology for GaN-based FET start being mature. Y. F. Wu et al reported the first radio frequency (RF) power performance, which was a power density of 1.1 W/mm at 2 GHz with a power added efficiency (PAE) of 18.6% for 1 μm gate-length GaN MODFET [53].

Two important techniques had driven the progress in GaN-based power performance: first was the introduction of a SiN passivation layer [54], which had an effect on suppression of the current collapse and improving the output power density [55]; second was the adoption of field-

plate structures [56], which could both increase the breakdown voltage and reduce the current collapse effect, improving the power performance. In 2004, Y. F. Wu et al reported a continuous wave output power density of 32.2 W/mm and PAE of 54.8% at 4 GHz at gate bias of 120 V [57]. In 2008, Moon et al reported GaN HEMT with n^+ source ledges was fabricated and a PAE of 55% at 5 W/mm at 33 and 36 GHz was achieved [58]. To date, multiple companies announce commercial product of GaN HEMT devices with outstanding performance, including TriQuint, Cree, RFMD, Eudyna, and so on [59].

However, some critical issues still restrain the inherent high performance of AlGaN/GaN HFETs for practical application. One of these issues is the large leakage current along the isolation region, which causes off-state power loss, additional noise, and reliability problems. An effective electrical isolation around the active area is thus essential to achieve low off-state drain current.

1. 2. 2 GaN MOSFET

The breakdown characteristics of AlGaN/GaN HEMTs were limited by the large leakage current of Schottky gate. To reduce the gate leakage current and improve the breakdown voltage, F. Ren et al reported the first MOS gate using a Ga_2O_3 (Gd_2O_3) film [60]. M. A. Khan et al reported a SiO_2/AlGaN/GaN MOS-HFET and the gate leakage current reduced by six orders of magnitude than AlGaN/GaN HFET [61], and low gate leakage current was beneficial to improve low-frequency noise [62]. P. D. Ye et al reported atomic-layer-deposited (ALD) Al_2O_3 as the gate oxide for GaN MOS-HFET [63]. N.-Q. Zhang et al reported high voltage GaN MOS-HFET with an on-resistance of 1.7 $m\Omega{\cdot}cm^2$ and breakdown voltage of 1.3 kV [64].

Another critical issue for GaN-based FETs is normally-on operation. For power operation, normally-off operation is necessary to achieve safe operation and low power consumption. Y. Cai et al reported enhancement mode (E-mode) AlGaN/GaN HEMT with a threshold voltage of 0.9 V using fluoride-based plasma treatment on the gate region [65]. Some groups reported a recessed-gate structure forming by the selective reduction of 2DEG layer only under gate metal in AlGaN/GaN HEMT [66, 67]. The resistance from gate to channel was reduced by this structure and the threshold voltage could be controlled by the recess depth. Combining the advantages of MOS channel with recessed-gate, a recessed MOS-gate AlGaN/GaN HFET was proposed, previously called hybrid MOS-HEMT or MOS Channel-HEMT (MOSC-HEMT) [47]. The 2DEG layer under the gate region is completely removed and the channel is controlled by the MOS gate, this device called as GaN MOSFET. T. Oka et al reported an AlGaN/GaN MOSFET with a threshold voltage of 5.2 V and a maximum field-effect mobility of 120

$cm^2 \cdot v^{-1} \cdot s^{-1}$ using SiN film [68]. H. Kambayashi et al reported normally-off AlGaN/GaN MOSFET with the threshold voltage of 3.7 V [69]. K.-S. Im et al reported AlGaN/GaN MOSFET with an Al_2O_3 gate oxide and a maximum field-effect mobility of 225 $cm^2 \cdot v^{-1} \cdot s^{-1}$ [70].

GaN MOSFET have potential use for power integrated circuits (ICs) owing to its lateral structure. Not only device isolation but also field isolation is necessary for development of GaN MOSFET power ICs. However, little work of device isolation techniques has been performed. Thus, as one of key challenges, device isolation is necessary for GaN-based FETs.

1. 3 Significance of device isolation

Device isolation, meaning electrical isolation between devices, is an ability of technology to make each device operate independently and get rid of the influence of proximity devices. Device isolation is one of the primary process steps and significantly important for the high-voltage operation of GaN-based FET and for GaN ICs. In silicon IC technologies, three most commonly adopted isolation methods are junction isolation, local oxidation of silicon (LOCOS), and trench isolation [71].

Nevertheless, these methods are difficult to be adopted for GaN MOSFETs using the recent GaN technologies. The native oxide forming by thermal oxidation can achieve thick oxide on silicon, but for now it is not available to natively grow thick gallium oxide (Ga_2O_3) on GaN by thermal oxidation. The largest thickness of silicon oxide (SiO_2) forming by chemical vapor deposition (CVD) is usually limited, because the oxide film is easy to crack when thickness becomes large due to different thermal expansion coefficients between GaN and SiO_2. Moreover, it is difficult to obtain highly-doped p-GaN layer by selective ion implantation. For the reasons above, GaN MOSFETs are still developed on i-GaN or p-GaN layer without any field isolation structure.

1. 3. 1 Device isolation of AlGaN/GaN HFET

Currently, mesa isolation as the simplest technique is widely adopted for AlGaN/GaN HFETs through dry etching to remove the 2DEG layer around active region [72, 73]. However, the etching damage was introduced due to the plasma bombardment of the mesa surface during dry etching process, particularly nitrogen vacancy, which acts as donor-like defect and leads to high surface leakage current. The large leakage current causes off-state power loss, additional noise, and reliability problems. The mesa structure is commonly formed by Cl_2-based dry

etching process (Figure 1.5a), and the gas sources are Cl_2, $SiCl_4$, BCl_3/Cl_2, and so on [74-76]. To reduce the surface leakage current on the mesa-isolated region, dielectrics filling like Si_3N_4, SiO_2, and Sc_2O_3 were used [77-79]. Some groups employed surface treatment such as N_2/H_2 treatment, UV ozone, and O_2 plasma to eliminate etching damage and reduce leakage current [78, 80]. The fabrication process steps of dielectrics deposition and lithography are added for these two methods.

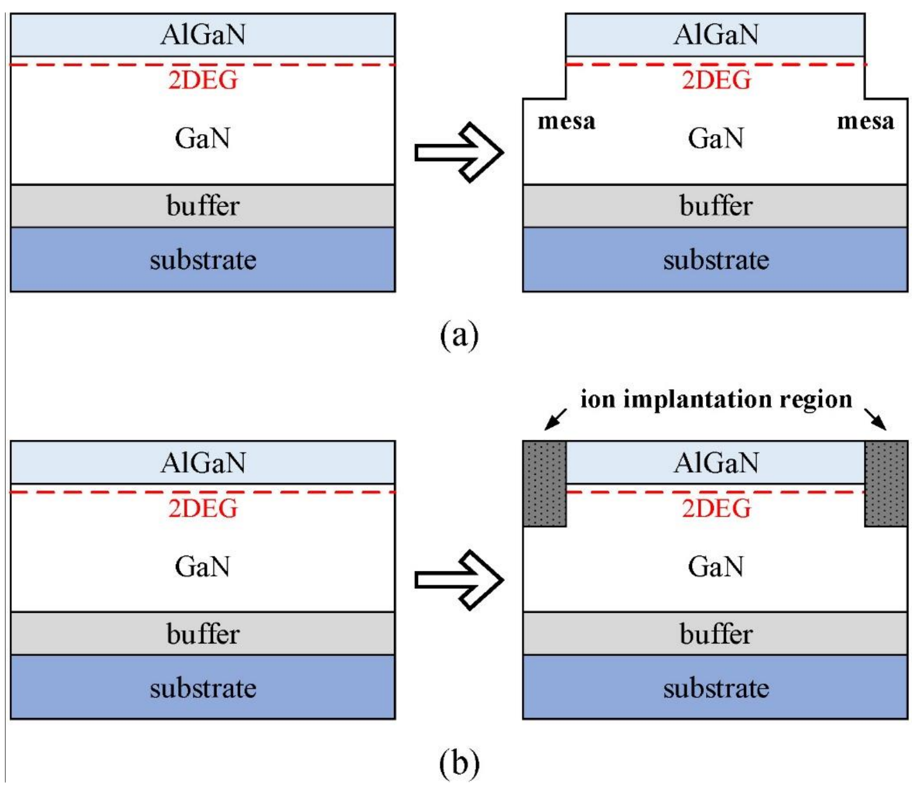


Figure1. 5 Schematic cross-section of (a) mesa structure and (b) ion implantation in AlGaN/GaN heterojunction.

For compound semiconductors, ion implantation, in addition to forming doped region, can also achieve device isolation through producing deep-level traps or recombination centers to form the high resistivity region. Implantation isolation offers the advantage of maintaining planar device morphology. Several ion species have been employed in GaN material or AlGaN/GaN HFETs, such as H^+, He^+, N^+, P^+/He^+, Zn^+, O^+, Fe^+ ions [81-88]. As shown in Figure 1.5b, ion implantation is usually used by eliminating the 2DEG in AlGaN/GaN heterojunction.

1. 3. 2 Field isolation of MOSFET

The isolation technologies in the Si MOSFET ICs is different from ordinary FETs, because a reverse channel appears beneath an field oxide since that an interconnection wire on the top of the field oxide can probably behave as a parasitic MOSFET-like device, as shown in Figure 1.6a. In order to prevent the formation of the reverse channel, field oxidation and field implantation (Figure 1.6b) are normally used to increase the threshold voltage according to

$$V_T = \phi_{ms} - \frac{Q_f + Q_B}{C_{ox}} + 2\psi_B \qquad (1.3)$$

The field region can be non-conductive even under high voltage and field isolation succeeds. Hence, field isolation is also indispensable for GaN MOSFET ICs.

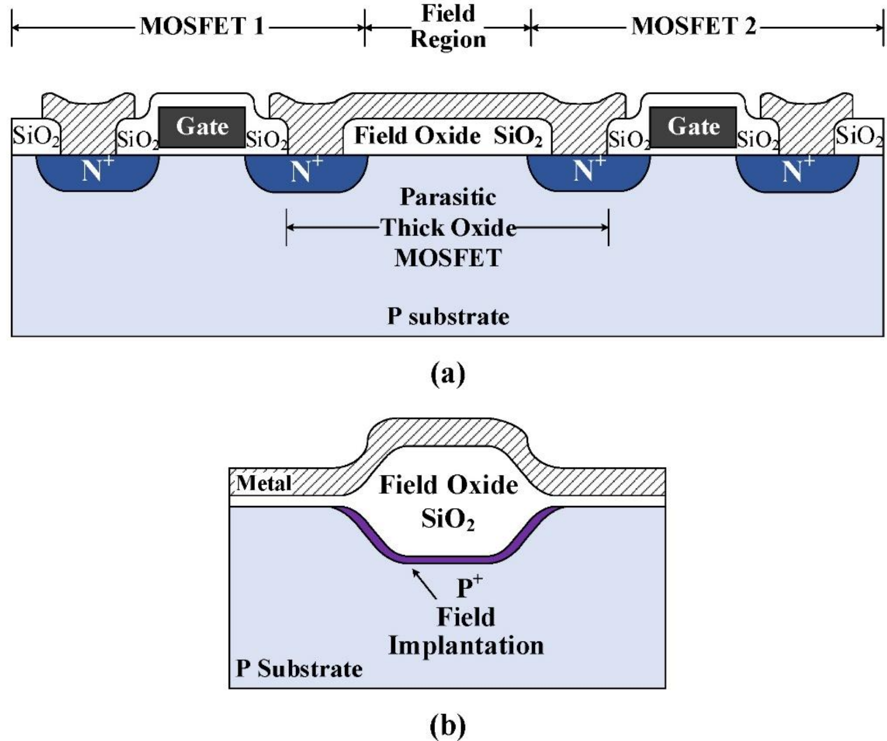
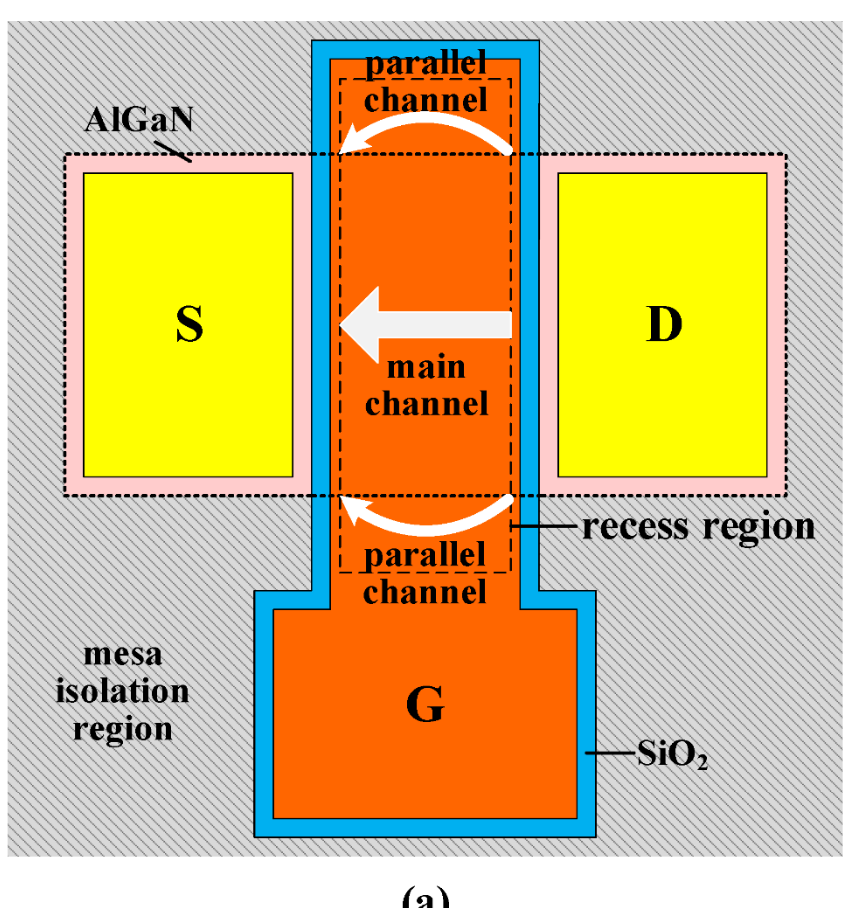


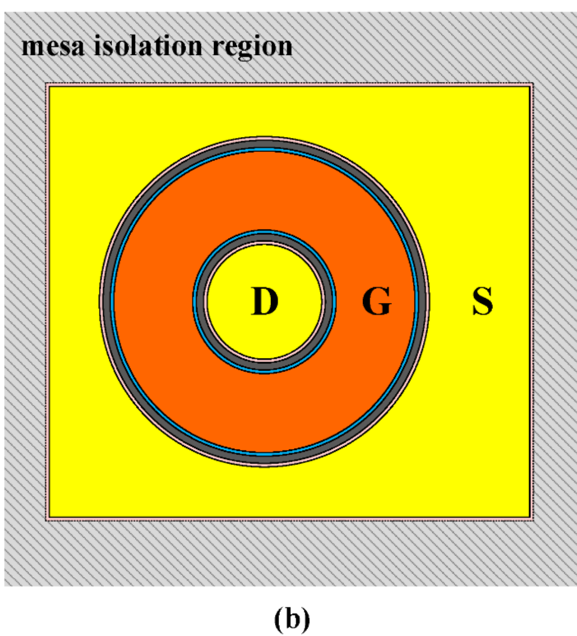
Figure1. 6 Schematic of (a) the parasitic MOSFET-like device in Si MOSFET ICs [89]; (b) field implantation and LOCOS isolation [71].

Similar to AlGaN/GaN HFET, the mesa structure is also simply adopted in many reports to achieve device isolation for the GaN MOSFETs. Unfortunately, in our previous work, we have found a phenomenon of parallel channel in a long-channel linear MOSFET (Figure 1.7a) if only mesa isolation was adopted. As shown in Figure 1.8, an overestimated maximum

mobility and off-state drain current of the linear device was about 192 $cm^2V^{-1}s^{-1}$ and 10^{-3} mA/mm, while for a long-channel circular device (Figure 1.7b) with the same recess and mesa condition it was about 150 $cm^2V^{-1}s^{-1}$ and 10^{-8} mA/mm, respectively. Besides this mobility discrepancy, two-step drain current and mobility were also appeared in the gate voltage range of around -4 V. The reason is considered that, a parasitic device could appear on the isolation region of a linear GaN MOSFET if a MOS-like structure is formed. Because the etching bias of the mesa process was higher than that of the recess process, leading to a greater plasma-induced damage on etching surface, and thus a negatively-shifted threshold voltage and relatively low mobility. As a result, the actual channel width is larger than the designed width and the field-effect mobility calculated from the transfer characteristics with the designed channel width will be overestimated. Therefore, it is necessary to develop effective field isolation methods for GaN MOSFETs and integrated circuits based on GaN MOSFETs in the future.



(a)



(b)

Figure1. 7 Schematic of (a) a long-channel linear and (b) a long-channel circular GaN MOSFET on AlGaN/GaN heterostructure.

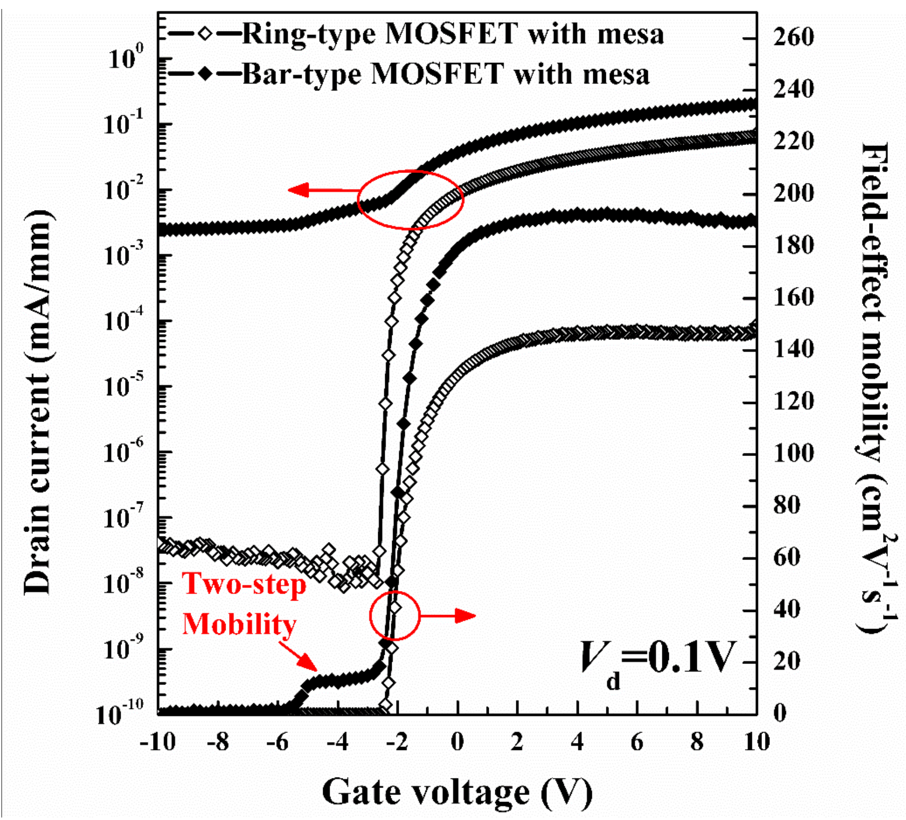


Figure1. 8 Transfer characteristics and field-effect electron mobility of a circular and a linear MOSFET. Both of devices were in the same recess condition and with only mesa isolation.

1. 4 Motivation and objectives

1. Motivation

For AlGaN/GaN HFET, the large leakage current of Schottky gate and current collapse effect have been attractive for a long time, and lots of investigations were reported. However, several work was focused on the leakage current caused by mesa etching damage, For example, dielectrics filling and surface treatment have been employed to eliminate etching damage and reduce leakage current. In these processes, O_2 plasma treatment is relatively easy and feasible because dielectrics deposition or lithography step is not needed and O_2 plasma can be generated by a plasma-enhanced chemical vapor deposition (PECVD) system. The oxidation mechanism of O_2 plasma treatment is not clear yet. Therefore, we studied the influence of O_2 plasma treatment on the mesa-isolated region of AlGaN/GaN HFETs by using the PECVD system, an effective treatment condition was established, and oxidation mechanism of O_2 plasma treatment were analyzed. Finally, AlGaN/GaN HFETs were fabricated with O_2 plasma treatment on the isolation region and characterized thereafter.

For GaN MOSFET, an ineffective isolation method like mesa structure would cause a parasitic MOSFET in the isolation region of linear device. Therefore, not only device isolation but also field isolation should be considered for GaN MOSFET. Ion implantation is a good option as device isolation method for compound semiconductor. However, the influence of thermal stability caused by annealing processes should also be considered. Therefore, the boron ion implantation for GaN MOSFET was used to prevent the formation of parasitic MOSFET in the isolation region. Circular and linear MOSFET was fabricated and compared to evaluate the isolation effectiveness. Moreover, the process sequences of annealing processes and implantation were altered to improve the resistivity of implanted-region.

2. Objectives

This thesis investigates the device isolation technologies for GaN-based FETs to overcome the disadvantages of mesa isolation. For AlGaN/GaN HFET, a process of O_2 plasma was employed on the mesa-isolated region to eliminate dry etching damage and reduce the leakage current; an effective treatment condition was established; oxidation mechanism of GaN surface treated by O_2 plasma were analyzed; the isolation effectiveness of AlGaN/GaN HFET with O_2 plasma treatment was evaluated. For GaN MOSFET, a process of boron ion implantation was adopted to prevent the formation of parasitic MOSFET in the isolation region and achieve field isolation; the implantation profile of boron ions and the sheet resistance of implanted region were described; the processes of annealing and ion implantation were improved; Circular and

linear MOSFETs were fabricated and characterized to evaluate the isolation effectiveness.

1. 5 Outline of dissertation

This thesis is divided into five parts.

In chapter 1, the advantages of GaN material and GaN-based device and the significance of device isolation and field isolation were introduced.

In chapter 2, the basic structure and fabrication processes, test methods and evaluation technology for AlGaN/GaN HFET and GaN MOSFETs were described in details. The basic fabrication processes included cleaning, mesa etching, ohmic contact, gate contact, recess etching (for GaN MOSFET), and gate oxide deposition (for GaN MOSFET). The current-voltage (*I–V*) and capacitance-voltage (*C–V*) measurements were conducted for AlGaN/GaN HFET and GaN MOSFETs and the transmission line model (TLM) and MOSFET structures were used to evaluate the isolation effectiveness. Circular and linear GaN MOSFETs were fabricated to examine the existence of a parasitic MOSFET-like device and evaluate the effectiveness of the isolation process, *I–V* and *C–V* characteristics were measured and the field-effect electron mobility could be calculated by a method of gate capacitance-transconductance and interface state density could be calculated using oxide capacitance and *I–V* characteristics.

In chapter 3, the influence of O_2 plasma treatment on the mesa-isolated region of AlGaN/GaN HFETs was studied. The effective condition was established by *I–V* characteristics, and the *I–V* results indicated that isolation current were strongly dependent on treatment temperature. The defect levels and chemical properties of the treated GaN surface were characterized through photoluminescence (PL) spectrum and X-ray photoelectron spectroscopy (XPS). AlGaN/GaN HFETs were fabricated with O_2 plasma treatment and characterized.

In chapter 4, GaN MOSFETs using boron ion implantation as field isolation process were fabricated and the effectiveness of boron field implantation was evaluated. The process of boron field implantation was developed and improved for GaN MOSFETs, the elimination of parasitic MOSFETs was confirmed by the *I–V* characteristics of circular MOSFETs fabricated in the isolation regions, and the isolation effectiveness of process was evaluated through the comparison of *I–V* characteristics between circular and linear device. The influence of implantation damage on device performance for different isolation structures were evaluated by the calculation of the field-effect electron mobility and the density of interface traps (D_{it}) according to *I–V* and *C–V* tests.

In chapter 5, the results are summarized and the future work is proposed.

Chapter 2 Fabrication process, test methods and evaluation technology of GaN-based FET

2. 1 AlGaN/GaN HFET

The ability of the generation of 2DEG layer by heterostructure is the most noteworthy advantage which distinguished GaN from other semiconductors. The AlGaN/GaN HFET is based on AlGaN/GaN heterostructure and used the 2DEG layer as a channel.

As mentioned above, the success of GaN epitaxial process is attributed to the viability of heteroepitaxy. There are three substrates that have been utilized to achieve commercial success with heteroepitaxial GaN-based devices: sapphire, SiC and Si. Table 2.1 compares the properties of sapphire, SiC, Si, and GaN.

Table 2. 1 The properties of substrate materials, sapphire, SiC, Si, and GaN.

Properties	Sapphire	6H-SiC	Si	GaN
Mismatch of lattice (%)	14	3.5	17	–
Thermal conductivity (relative)	0.4	4.9	1.56	1.3
Electrical Resistivity (Ω·cm)	$>10^{14}$	$>10^{5}$	10^{4}–10^{5}	$>10^{5}$
Thermal stability	Very high	Very high	Moderate	–
Band-gap E_g (eV) 300 K	9.9	3.0	1.2	3.39
Substrate size (inch)	6	6	8−12	2
Substrate cost (relative)	High	Very high	low	Very high
Compatibility with ICs	Low	Moderate	Very high	–

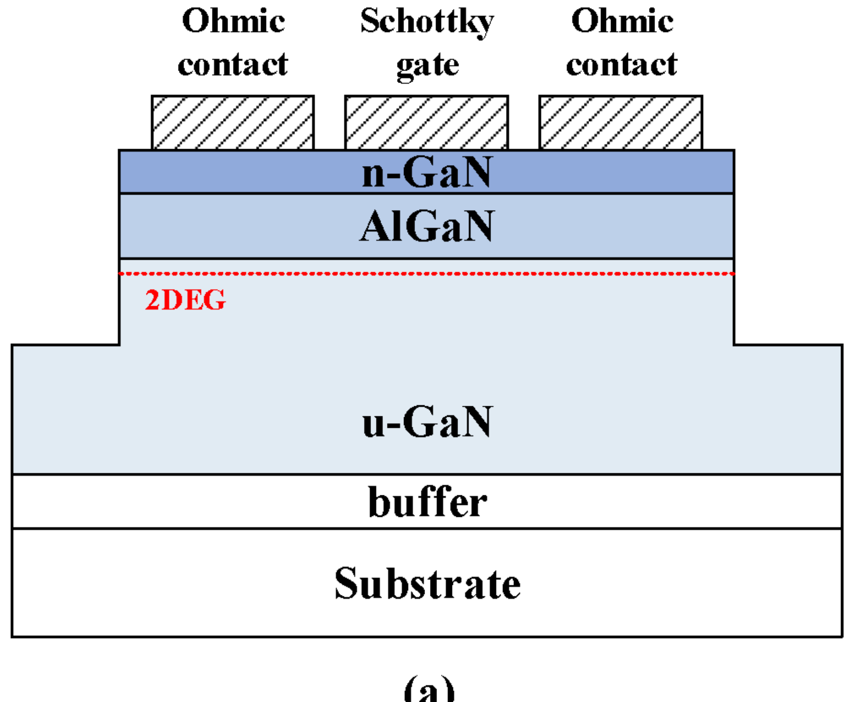
6H-SiC substrate has a lowest lattice mismatch and highest thermal conductivity, and is the best candidate for GaN heteroepitaxy growth in spite of the highest product cost. Sapphire substrate has highly thermal stability and a relative lower lattice mismatch, and is able to cut off the channel of GaN MOSFET due to the high resistivity. Silicon substrate is benefit for batch handling of integrated products due to the highest compatibility, lowest product cost, and largest substrate size. Therefore, tradeoffs must be considered for academic research, sapphire and silicon substrate are commonly used in our experiments.

Another crucial problem for AlGaN/GaN heterostructure is the current collapse effect by

the electron injection at the source and drain surface [90, 91]. Current collapse is a charging up of a second virtual gate appearing in the gate drain access region, which could modulate the 2DEG and finally make the device show strong hysteresis [92]. A n-type GaN cap layer with high doping density could be used to eliminate the current collapse effect [93]. Moreover, the use of n-GaN cap layer can not only eliminate the current collapse effect but also heal surface inhomogeneities and lower the ohmic contact resistance.

2. 1. 1 Structures of AlGaN/GaN HFET

A conventional linear AlGaN/GaN HFET with mesa isolation is shown in Figure 2.1a. The gate length L_G of the device is 3 μm, the gate width W_G is 50 μm, and the spacing between source/drain electrode and gate electrode is 3 μm (Figure 2.1b). There are several different gate structures like MIS-gate, recessed-gate (Figure 2.1c), the ordinary Schottky gate without thinning AlGaN layer was used because the whole attention is centered on the isolation region.



(a)

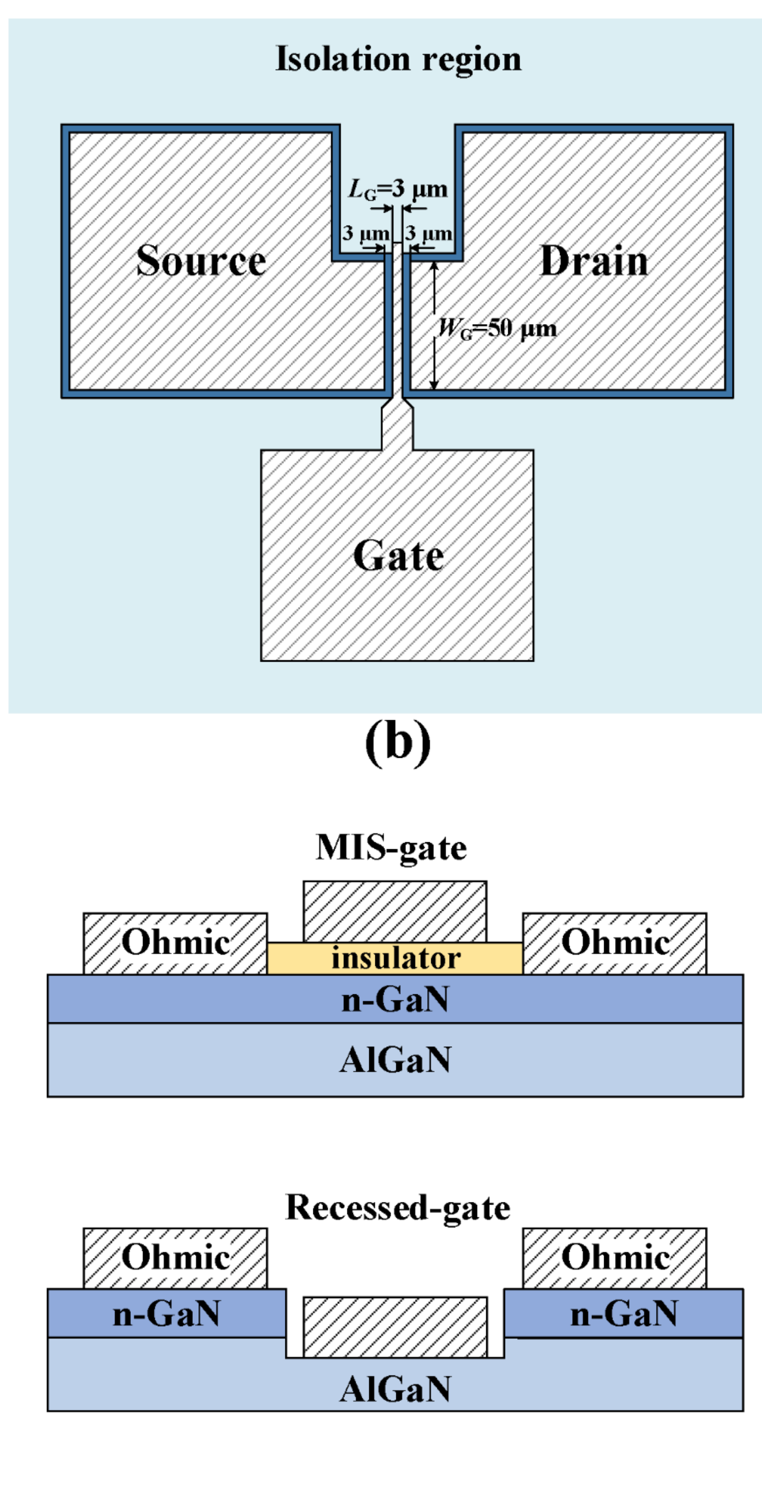


Figure 2. 1 The cross section (a) and bird view (b) of a linear AlGaN/GaN HFET with mesa isolation. (c) shows MIS-gate and recessed-gate structures.

2. 1. 2 Fabrication process of AlGaN/GaN HFET

Borrowing from GaAs p-HEMT technology, conventional AlGaN/GaN HFET processing schemes often proceed through a sequence of 1) wafer cleaning, 2) mesa isolation, 3) ohmic metalization and annealling, 4) gate and contact pad metalization, and 5) passivation, as shown in Figure 2.2. The process of passivation was not under our consideration because the gate region and isolation region were passivated by dielectric film simultaneously, which has an obvious influence on the isolation effectiveness evaluation.

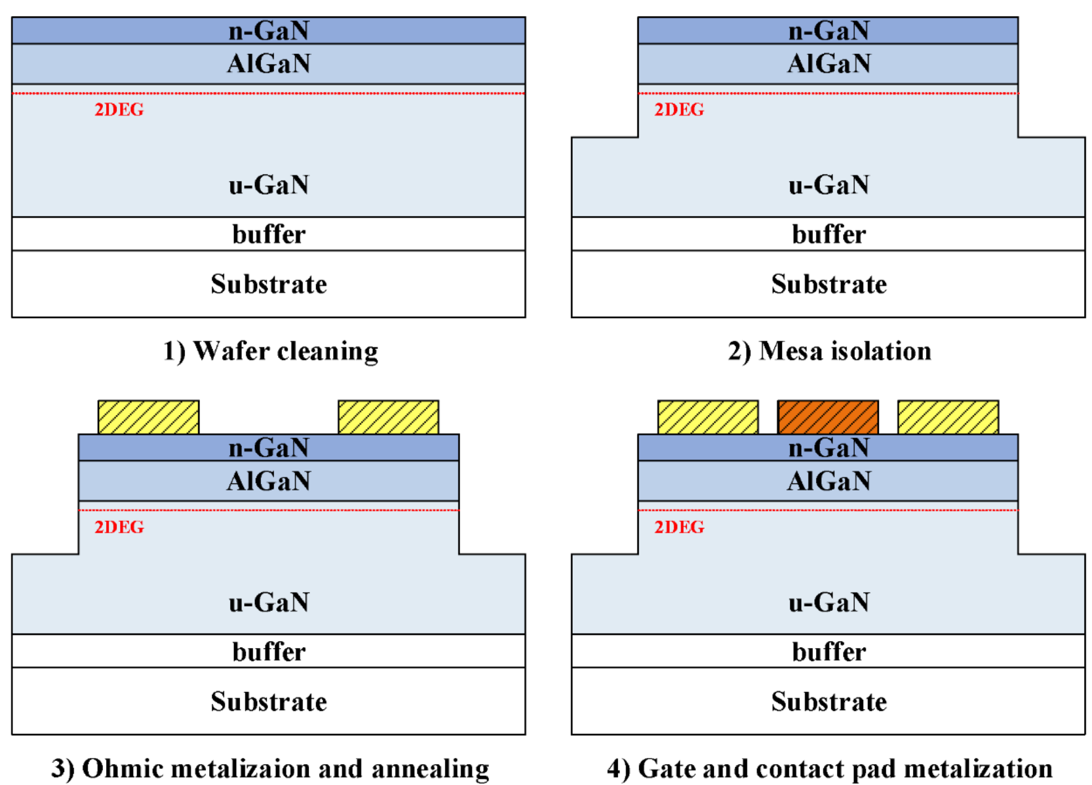


Figure 2. 2 The fabrication process of AlGaN/GaN HFET with mesa isolation.

The detailed instruction of each process will be introduced.

1) Wafer cleaning

The wafer was cleaning with SPM (H_2SO_4:H_2O_2 = 4:1, volume ratio) solution and organic solution in sequence. The wafer was dipped in SPM solution heating at 100 °C for 10 min, cleaned with deionized (DI) water and blow-dry using nitrogen gun. Then the wafer immersed in the acetone solution was cleaned with ultrasonic cleaner for a few minutes. Finally, the wafer was rinsed with acetone, methanol, and DI water.

2) Mesa isolation.

A mesa structure is formed through dry etching. Dry etching techniques for III–V nitrides includes chemically assisted ion beam etching, laser ablation, reactive ion beam (RIE) etching, and inductively coupled plasma (ICP) etching. At present, inductively-coupled chlorine-based plasmas have become the most common method to etch GaN due to high high-density plasma and high uniformity over large areas, lower ion bombardment energy relative to RIE, and lack of electromagnets and waveguides required for electron cyclotron resonance (ECR).

In our experiments, an ICP system–RIE-200-iPG (from SAMCO, Inc., Fushimi, Kyoto, Japan) was employed with a $SiCl_4$ source and a Cl_2 source. Figure 2.3 shows the internal components of the equipment. Inductively coupled coils generates plasma and the plasma density is controlled by ICP power. The bias power controlled the speed that plasma move towards sample, a higher bias power means a stronger ion bombardment on the sample. A helium gas was used for cooling to keep the sample stage at room temperature during the etching process.

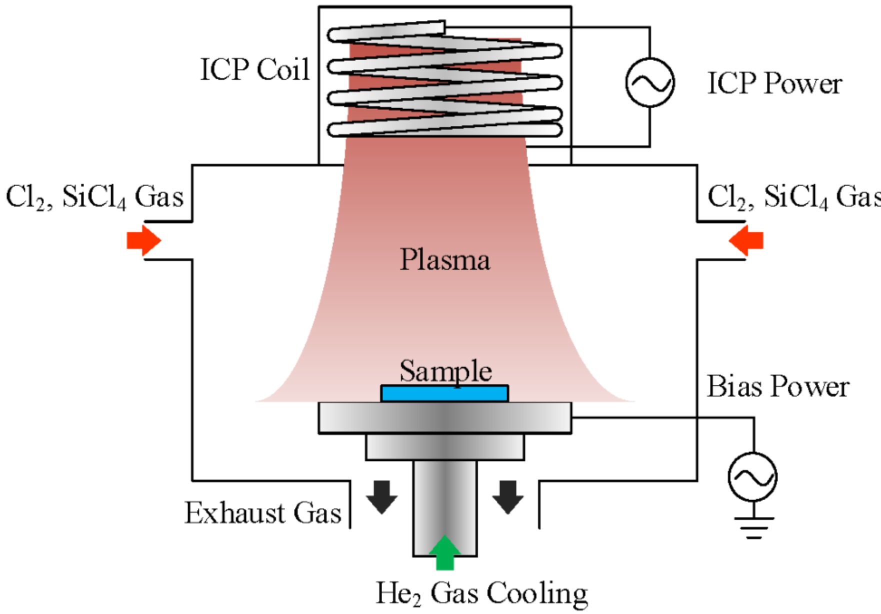


Figure 2. 3 Schematic of internal components in the ICP system.

In our previous work [94, 95], a two-step etching process was used for mesa formation. The first step was done by $SiCl_4$ gas with a flow rate of 4 sccm, ICP power of 50 W, bias power of 100 W and at a working chamber pressure of 0.25 Pa. The second step was done by Cl_2 gas with a flow rate of 4 sccm, ICP power of 50 W, bias power of 50 W and at a working chamber

pressure of 0.25 Pa. The second etching of Cl_2 gas was planned to remove any possible oxide induced by $SiCl_4$ gas. However, it was found that much more damage was produced by Cl_2 etching, and the details will be discussed in Chapter 3.

Afterwards, the mesa etching condition was altered to be same with the recess etching condition used for MOSFET. And this recess condition was $SiCl_4$ gas flow of 3 sccm, ICP power of 100 W, bias power of 20 W, and working chamber pressure of 0.25 Pa. The etching rate under this condition was approximately 1.25 nm/min [96].

Usually, a 2 μm positive photoresist (abbreviated as PR, HPR-1183L, Fujifilm Corp., Minato, Tokyo, Japan) layer was used as the etching mask. The mesa depth was approximately 100 nm, in which a good-quality GaN surface could be obtained. After dry etching, a HNO_3:HF buffered solution (BHF; 1:1, volume ratio) was used to remove possible Si contaminants on the etched surface and good for reduction of surface current on the mesa-isolated region.

3) Ohmic metallization and annealing.

Most GaN ohmic contact was achieved using multilayers of Ti/Al/x/Au, where x may be Ti, Ni, Pt, Mo, or Pd. Each kind of metal play different roles during the formation of ohmic contact, and their roles are not well agreed yet. One issue unique to GaN ohmic contact formation is the extremely high annealing temperature, typically 850 °C, which is beyond the melting point of Al (661°C) and leading to rough ohmic contact morphology.

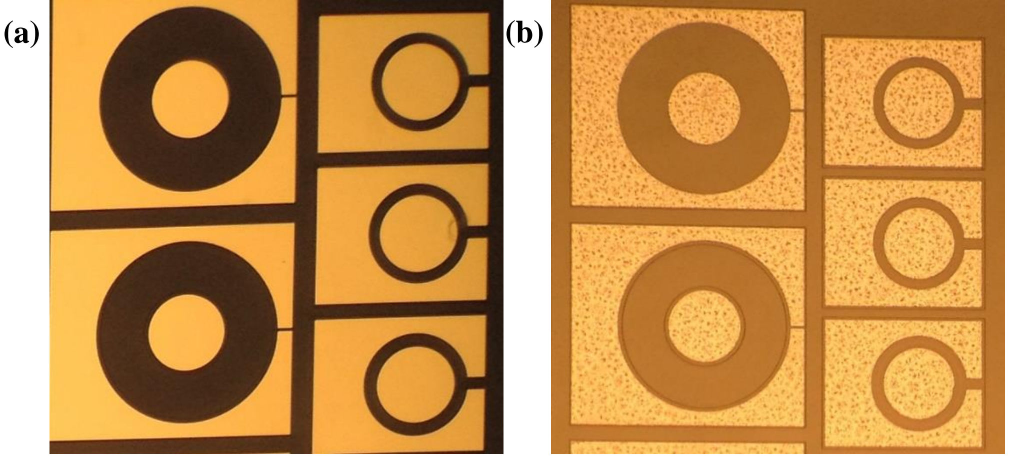


Figure 2. 4 Pictures of (a) before 850 °C annealing and (b) after 850 °C annealing.

A metal stack of Ti/Al/Ti/Au (50/200/40/40 nm) was deposited as ohmic electrodes through sputtering (ALVAC MNS-2000-RF-HS). After deposition, the extra metal layer was removed by a lift-off process and annealed at 850 ℃ for 1 min in nitrogen ambient. The ohmic

the contact resistance was usually 0.1–1 Ω·mm.

4) Gate and contact pad metallization.

Traditionally, most AlGaN/GaN HFET have employed Ni/Au as the Schottky gate contact due to good electrical properties and adhesion to the (Al)GaN surface. However, other candidates for gate electrode have been proposed, such as Pt/Au, TiN/W/Au [73, 97], a Ni/Au (70/30 nm) bi-layer was deposited as the gate metal in out experiments. The annealing is not needed for gate contact formation. Figure 2.5 shows a picture of AlGaN/GaN HFETs after finishing the gate metallization.

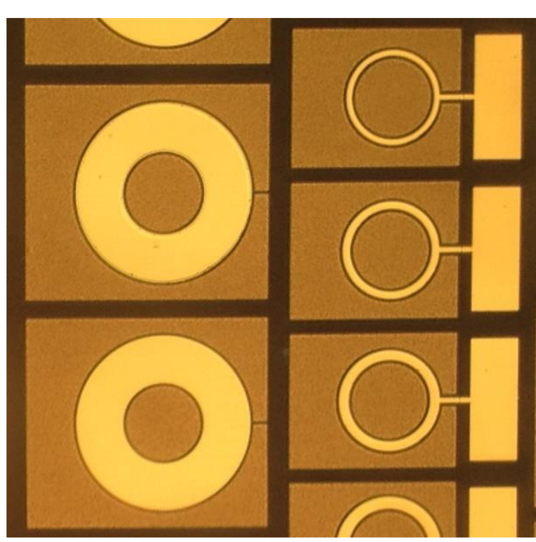


Figure 2. 5 The picture of AlGaN/GaN HFETs after finishing the gate metallization.

2. 1. 3 Test methods of AlGaN/GaN HFET

The AlGaN/GaN HFET are characterized by *I–V* measurement with semiconductor parameter analyzer (Agilent HP 4155C). The *I–V* characteristics of TLM test can extract the ohmic contact resistance and sheet resistance. The *I–V* test on the DC performance of AlGaN/GaN HFET includes gate current-gate voltage (I_g-V_g), drain current-drain voltage (I_d-V_d), and drain current-gate voltage (I_d-V_g). Transconductance G_m as an important parameter reflects the controlling ability of Schottky gate upon the channel current, and equals to the derivatives of I_d-V_g characteristics. The breakdown characteristics of TLM structure were conducted using *I–V* test.

2. 2 GaN MOSFET

GaN MOSFET can realize E-mode operation which is unable for AlGaN/GaN HFET. Four key factors are necessary to realize a good MOSFET:1) a good oxide layer with very low leakage current; 2) a good channel controlled by the gate bias to realize on and off state; 3) a good source and drain ohmic contacts to provide carriers and connecting the MOS channel; 4) a good interface between the oxide layer and substrate semiconductor with low interface state intensity.

In an ordinary Si n-MOSFET, the drain and source regions are formed through the heavily n-type doping in the P-type substrate, and gate oxide SiO_2 is formed by thermally oxidation, as shown in Figure 1.6a. Although some groups realized GaN MOSFET using this structure [98-100], it is still difficult to complicate with Si technology. Actually, consistent p-type doing in GaN is still the unresolved particular problem. The reasons for this difficulty are: 1) the native n-type background conductivity of GaN; 2) residual implant damage also has n-type character in GaN; 3) lots of nitrogen vacancies on the surface layer leading to a n-type surface. Table 2.2 summarized characteristics of different implanted dopant in GaN.

Table 2. 2 Characteristics of different implanted dopant in GaN.

	Max achievable doping level cm^{-3})	Ionization level (meV)
Donor		
Si	5×10^{20}	28
S	5×10^{18}	48
Se	2×10^{18}	
Te	1×10^{18}	50
O	3×10^{18}	30
Acceptor		
Mg	5×10^{18}	170
Ca	5×10^{18}	165
Be	5×10^{17}	
C	n-type	

2. 2. 1 Structures of GaN MOSFET

To replace the ion implantation structure, the 2DEG layer in the AlGaN/GaN heterojunction as drain and source, and recessed-gate structure are proposed, as shown in Figure 2.6. The 2DEG layer under gate contact is removed by dry etching, and a recess structure is formed, so this device is called as recessed-gate MOSFET. The remained 2DEG layer as source and drain provides high-intensity electrons, and the channel is formed on the u-GaN layer. To obtain a good coverage of the oxide on the sidewall, the gate recess depth should not be deep. The oxide thickness is usually smaller than 100 nm, hence, the gate recess depth is commonly around 50 nm considering the thickness of 2DEG layer.

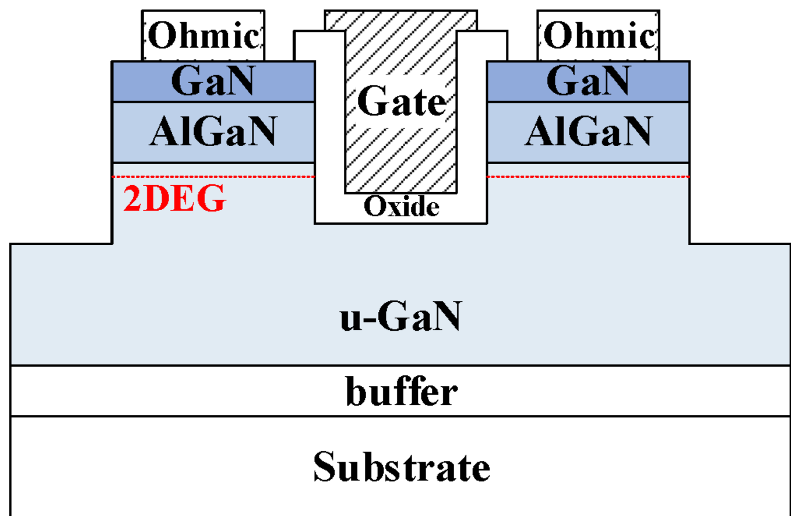
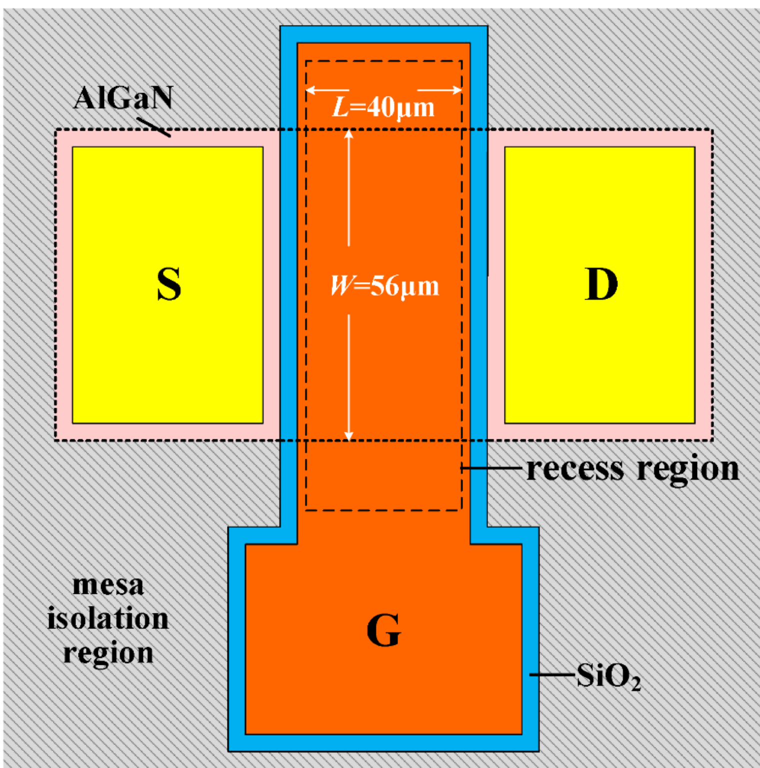


Figure 2. 6 Schematic of recessed-gate structure for GaN MOSFET with mesa isolation.

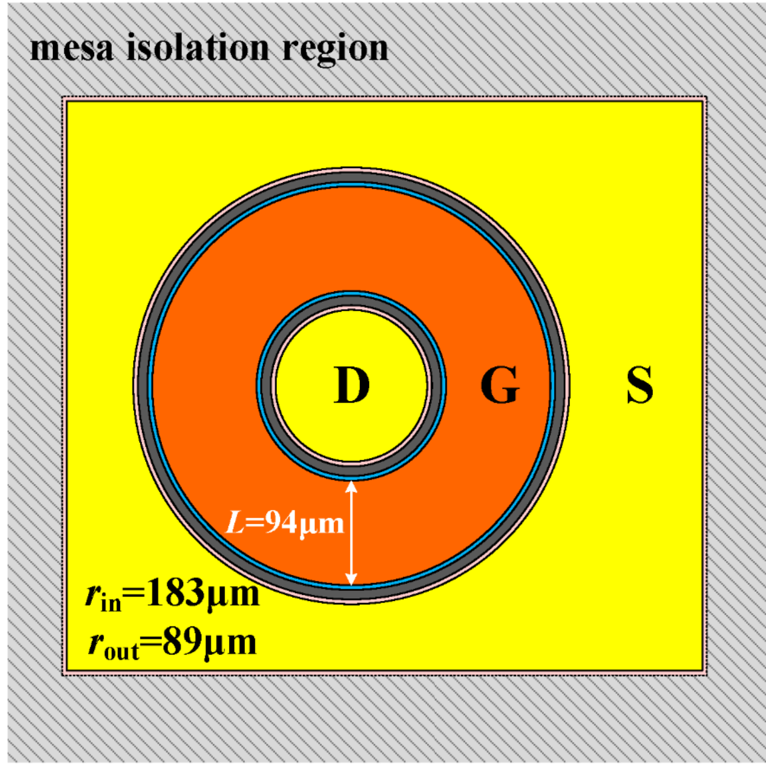
To avoid the short channel effect only long-channel MOSFET was fabricated, because the parasitic resistance can be ignored due to the large channel resistance. Both of circular and linear MOSFET were fabricated, as shown in Figure 2.7. The linear device has a gate length of 40 μm and gate width of 56 μm, respectively. The inner radius and the outer radius of the circular are 89 μm and 193 μm, respectively. The effective channel width W of 819 μm which was calculated from

$$W = \frac{2\pi L}{\ln r_{out} - \ln r_{in}} \quad (2.1)$$

where r_{out} and r_{in} is the outer and inner radius.



Bar-type MOSFET



Ring-type MOSFET

Figure 2. 7 Schematic of long-channel linear and circular GaN MOSFET.

2. 2. 2 Fabrication process of GaN MOSFET

The fabrication processes of GaN MOSFET are more complicated than AlGaN HFET. The fabrication process of an ordinary recessed-gate GaN MOSFET contains 1) wafer cleaning, 2) mark etching, 3) mesa isolation, 4) gate recess etching, 5) gate oxide deposition, 6) ohmic metallization and annealing, and 7) gate metallization as shown in Figure 2.8. The processes of gate recess etching and gate oxide deposition will be discussed.

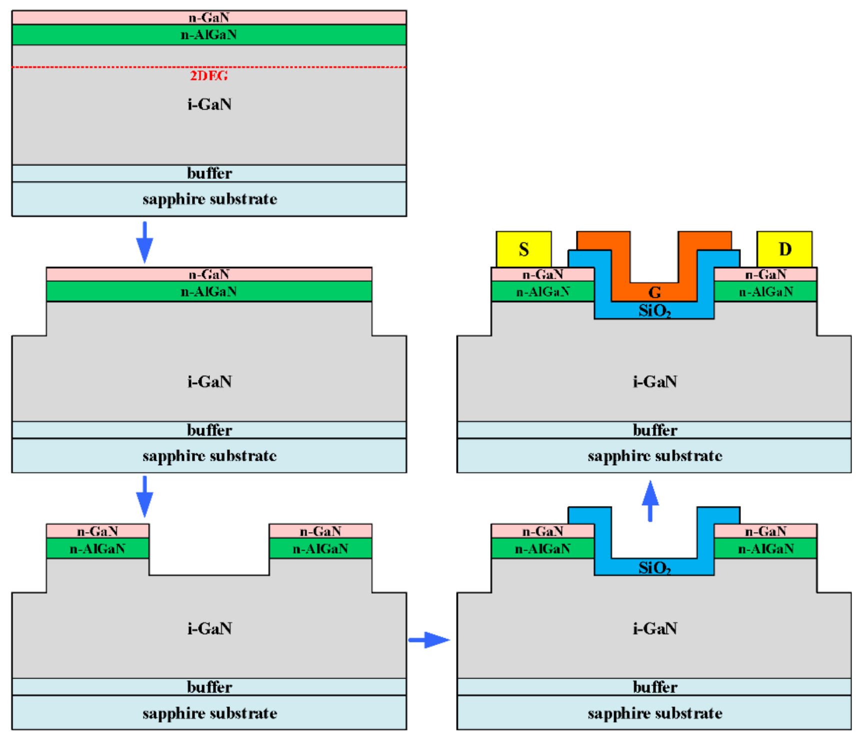


Figure 2. 8 The fabrication process of recessed-gate GaN MOSFET.

1) Gate recess etching

The gate recess was also formed by the same ICP system–RIE-200-iPG with a $SiCl_4$ source. The etching condition was $SiCl_4$ gas flow of 3 sccm, ICP power of 100 W, bias power of 20 W, and working chamber pressure of 0.25 Pa. The etching rate under this condition was approximately 1.25 nm/min. However, despite the extremely low etching rate, dry etch-induced lattice damage can severely degrade device performance. The avoidance of etching damage is required to obtain a high-quality channel with high carrier mobility and low interface states. Low ICP and bias power of ICP system could decrease the etching rate which is benefit to reduce etching damage. Low power might also get an irregular recess profile and even failure in the MOSFETs operation.

Etching mask is important for good etching profile. For easy fabrication, PR mask was often used to protect active region during the mesa etching. However, it was found that trenching effect at the bottom near the sidewall was observed if PR mask was adopted, and the SiO_2 as etching mask can improve the recess profile [101]. Therefore, The SiO_2 film of about 500 nm thickness deposited by tetraethylorthosilicate (TEOS) PECVD was used as the recess etching mask. After etching, the BHF solution and HNO_3: BHF = 1:1 solution were used to remove SiO_2 film and possible contamination of Si on the etched surface.

2) Gate oxide deposition

The types and oxidation methods of gate oxide also have an effect on device performance, especially mobility. The common SiO_2 film growth method is PECVD growth using silane- or TEOS-based source. The SiO_2 film deposited with silane-based PECVD was preferred to the film deposited with TEOS source because of a lower interface state intensity. The thickness of gate oxide was controlled under 100 nm. After deposition, a post-annealing process of 1000 °C for 10 min in N_2 ambient would be performed.

The summary of key points of GaN MOSFET fabrication process is as follows. 1) To obtain an etched surface with less damge, a condition of low etching rate and SiO_2 mask are preferred, as well as the use of HNO_3: BHF = 1:1 solution to clean the etched surface; 2) Silane-based SiO_2 film is prior to TEOS-based film.

2. 2. 3 Test methods of GaN MOSFET

The GaN MOSFET are characterized by I–V measurement with semiconductor parameter analyzer (Agilent HP 4155C), and C–V measurement with LCR meter (Agilent 4284A). The I–V characteristics of TLM test can extract the ohmic contact resistance and sheet resistance. The I–V test on the DC performance of GaN MOSFET includes gate current-gate voltage (I_g-V_g), drain current-drain voltage (I_d-V_d), and drain current-gate voltage (I_d-V_g). Transconductance G_m as an important parameter reflects the ability of the gate oxide controlling the channel current, and equals to the derivatives of I_d-V_g characteristics. The frequency of C–V measurement is determined by capacitance-frequency (C–f) measurement, 100 kHz with a signal level of 25 mV.

The gate capacitance-transconductance method was adopted to determine the electron field-effect mobility. According to the basis of the gradual channel approximation of MOSFETs, field-effect mobility could be calculated as

$$\mu_{FE} = \frac{G_M L}{C_{OX} W V_d} \quad (2.2)$$

where L is the gate length, C_{OX} is the oxide capacitance per unit area, and G_M is the transconductance.

The equivalent circuit of the MOS structure can be presented as the oxide capacitance C_{OX} connected in series with a parallel connection of the depletion capacitance C_D and the interface-related capacitance C_{it}. In this case, based on the definition, the subthreshold swing S could be expressed as

$$S = \frac{dV_g}{d\log I_{ds}} = (\ln 10)\left(\frac{kT}{q}\right)\left(1 + \frac{C_D}{C_{OX}} + \frac{C_{it}}{C_{OX}}\right) \quad (2.3)$$

where k is the Boltzmann constant, T is the absolute temperature, and q is the electron charge.

2. 2. 4 Fabrication of GaN MOSFET using BCl_3 etching gas

In our previous work, we achieved a precise control of ICP etching rate of 1.2 nm/min and determined the optimum ICP condition of GaN MOSFETs on AlGaN/GaN heterostructure with the etching gas of $SiCl_4$. However, the devices etched with $SiCl_4$ gas had a negative threshold voltage, the possible reason may be silicon (Si) contamination. Therefore, we tried to use BCl_3 instead of $SiCl_4$ as the gate recess etching gas in order to reduce the influence of Si contamination on threshold voltage.

The GaN MOSFETs on AlGaN/GaN hetero-structure with different recess etching conditions was fabricated and characterized. The device fabrication process was based upon standard photolithography and lift-off technologies. The gate recess was conducted utilizing ICP system with BCl_3 and $SiCl_4$ gas. The SiO_2 film of about 500 nm thickness deposited by tetraethylorthosilicate (TEOS) PECVD was used as the etching mask. The etching conditions of three samples are listed in Table 2.3.

Sample No. 1 and No. 2 were done with $SiCl_4$ gas, ICP power of 100 W and 50 W, respectively, bias power of 20 W, $SiCl_4$ gas flow rate of 3 sccm and working chamber pressure of 0.25 Pa (termed as: No. 1 $SiCl_4$ 100W/20W and No. 2 $SiCl_4$ 50W/20W, respectively). The etching rates of these two samples were about 1.2 nm/min and 1.0 nm/min, respectively. Sample No. 3 was etched with mixed BCl_3/Cl_2 gas (20/20 sccm), ICP power of 100 W, bias power of 25 W and at a working chamber pressure of 0.6 Pa. The etching depths were 110 nm and 60 nm respectively (termed as: No. 3 BCl_3/Cl_2, 60 nm), and the etching rates were about 30 nm/min.

During the etching processes, the sample stage was cooled by helium gas to keep at the room temperature.

Table 2. 3 Recess etching process conditions of all the samples.

No.	Term	ICP Power (W)	Bias Power (W)	Gas	Flow Rate (sccm)	Chamber Pressure (Pa)	Etching Rate (nm/min)	Recess Depth (nm)
1	$SiCl_4$ 100W/20W	100	20	$SiCl_4$	3	0.25	1.2	60
2	$SiCl_4$ 50W/20W	50	20	$SiCl_4$	3	0.25	1.0	60
3	BCl_3/Cl_2, 60 nm	100	25	BCl_3/Cl_2	20/20	0.6	30	60

After these dry etching processes, the samples were immersed in HNO_3: BHF = 1:1 solution to remove the possible contamination of Si on the etched surface. As the gate insulator, a 103.5-nm-thick SiO_2 layer was then deposited by PECVD (SAMCO PD-220LC) with silane-based source, followed by annealing at 1000℃ for 10 min in N_2 ambient. After the gate insulator patterning, the source and drain ohmic contacts were formed using Ti/Al/Ti/Au (50/200/40/40 nm) annealed at 850 ℃ for 1 min in N_2 ambient. TLM measurement showed that the contact resistance was approximately 0.15-0.36 Ωmm. A Ni/Au (70/30 nm) bi-layer was deposited as the gate metal.

The device used for evaluation is long channel circular MOSFET with a channel length L of 94 μm and an effective channel width of 819 μm. For all the samples, the gate leakage currents were below 10^{-9} A with gate voltage from -10 V to 10 V and drain voltage of 0.1 V, as shown in Figure 2.9. In particular, gate leakage is restrained even at a positive gate bias, which is beneficial to achieve the E-mode operation. To extract the capacitance of gate insulator, measurement of C–V characteristics was performed under frequency of 100 kHz and with gate voltage from -10 to 15 V. From Figure 2.10, we can observe the hysteresis and the negative threshold voltage from -5.5 to -3.5 V. The difference of threshold voltage by different etching gas is not clear. One reason is the possible positive charges existing in the gate insulator layer leading to a negative shift on the threshold voltage [102], and the other reason may be from the GaN channel layer of this work. Through the evaluation of device isolation, we confirmed that the isolation region had a large leakage current indicating that the GaN buffer layer is slight n-type rather than semi-insulating type.

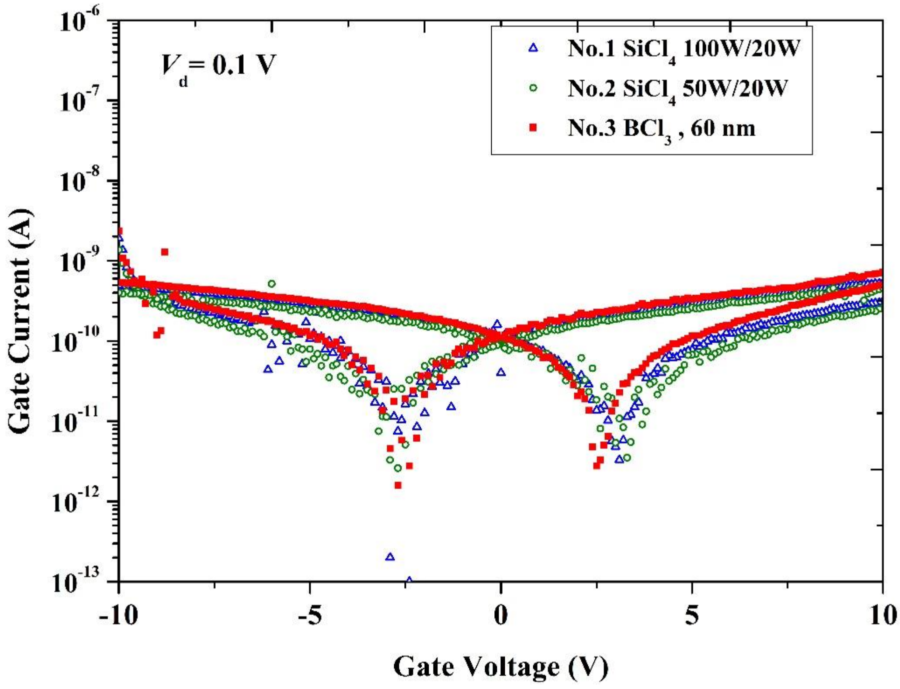


Figure 2. 9 Gate leakage current of GaN MOSFETs of all the samples with gate voltage from –10 to 10 V.

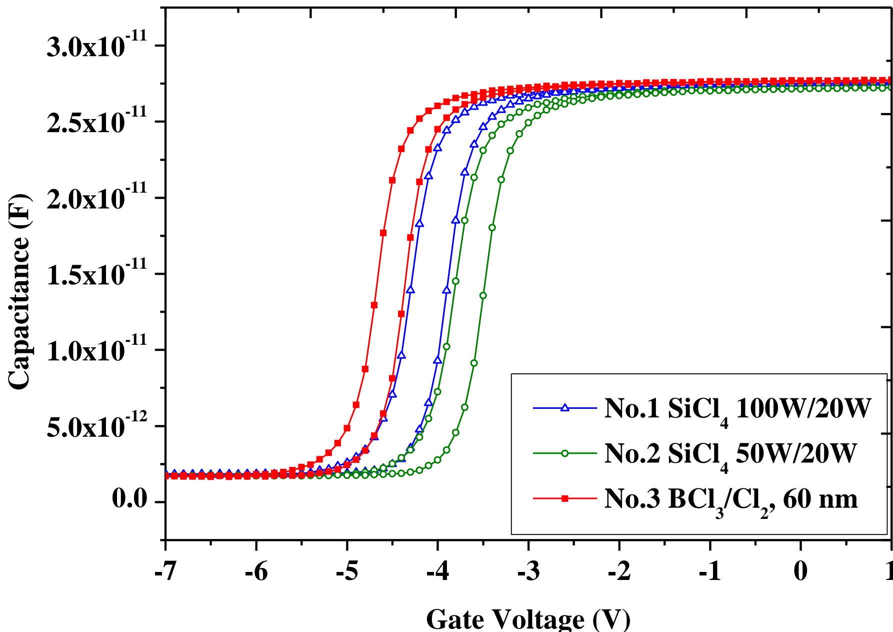


Figure 2. 10 The segment of *C–V* characteristics curve of GaN MOSFETs of all the samples with gate voltage from -7 to 1 V.

Figure 2.11 shows the I_d-V_d characteristics of the device etched with BCl_3 gas. Drain voltages range from 0 to 20 V and gate voltage range from 10 to -3 V. Device operation up to gate voltage of 10 V was confirmed. The gate capacitance-transconductance method was adopted to determine the electron field-effect mobility. The field-effect mobility of all the samples is showed in Figure 2.12. The electron mobility of device etched with BCl_3 gas is 141.5 $cm^2V^{-1}s^{-1}$, as listed in Table 2.3. The mobility is almost the same for the devices with 20 W bias power and different ICP power, implying that the mobility is more sensitive to the bias power instead of the ICP power. In reference [101], we have reported the influence of etching conditions on the recess profiles, mobility and interface state density for devices with ICP power from 50 to 100 W, bias power from 20 to 60 W and the etching mask of SiO_2. It showed that higher bias power would bring more interface states and lower mobility. It was considered to be due to the much serious surface damage and silicon contamination occurring at higher bias power.

Figure 2.13 shows the I_d-V_g characteristics of the devices in the subthreshold region. Considering the depletion capacitance is zero, C_{it} can be calculated from the extracted subthreshold swing S. The interface states density D_{it} can then be calculated from C_{it}. The device etched with BCl_3 gas and the recess depth of 60 nm obtained a low interface state density, as listed in Table 2.4.

Table 2. 4 The measured maximum field-effect mobility and interface state density of all the samples

No	Term	Average of C_{ox} (10^{-8} Fcm^{-2})	Field-effect Mobility μ_{FE} ($cm^2V^{-1}s^{-1}$)		Subthreshold Swing S (mV/dec)		Interface State Density D_{it} (10^{11} $cm^{-2}eV^{-1}$)	
			Forward	Reverse	Forward	Reverse	Forward	Reverse
1	$SiCl_4$ 100W/20W	3.45	133.3	133.9	141.5	137.6	2.96	2.82
2	$SiCl_4$ 50W/20W	3.41	133.9	134.5	177.1	154.9	4.21	3.41
3	BCl_3/Cl_2, 60 nm	3.47	141.1	141.5	112.1	139.7	1.91	2.91

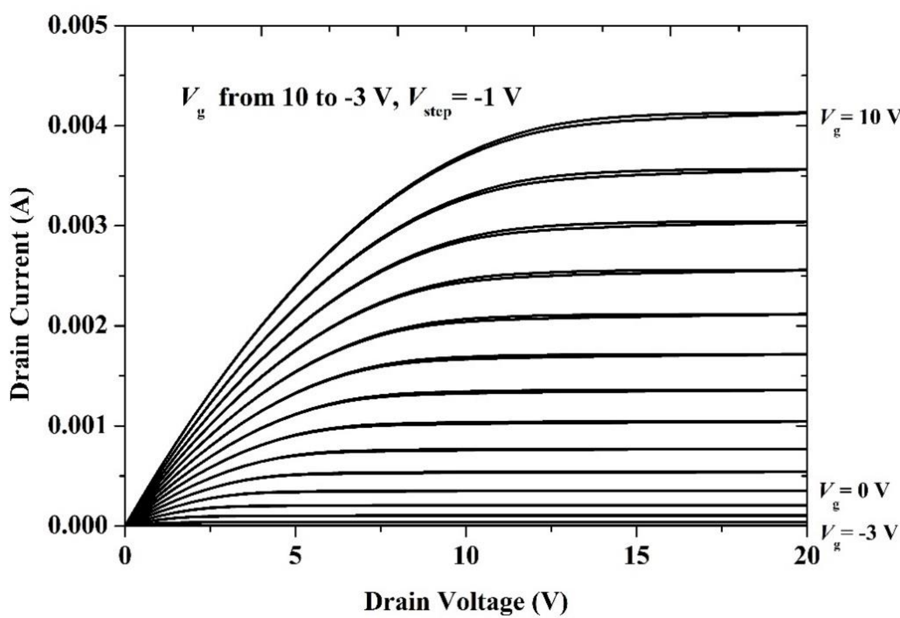


Figure 2. 11 I_d-V_d characteristics of the device etched with BCl_3 gas and the recess depth of 60 nm.

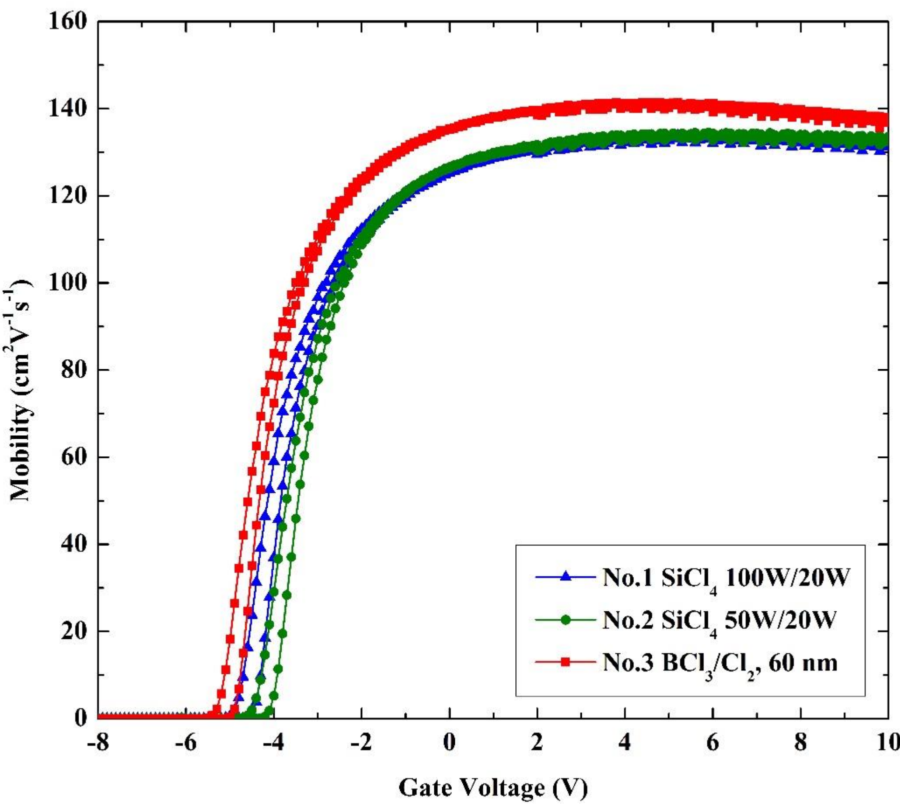


Figure 2. 12 The field-effect mobility of GaN MOSFETs of all the samples.

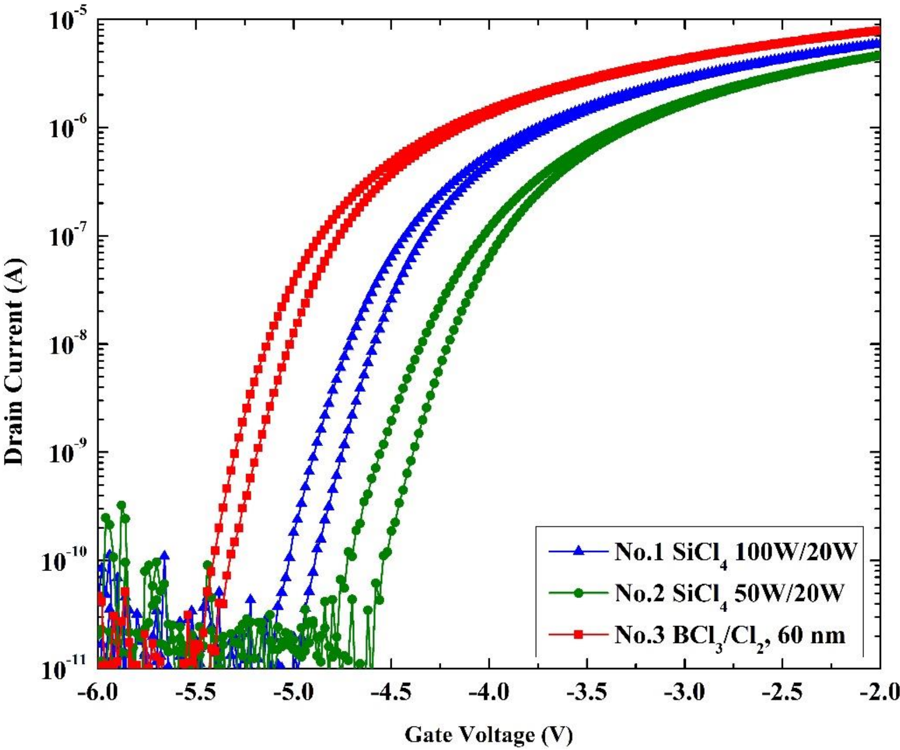


Figure 2. 13 I_d-V_g characteristics of GaN MOSFETs of all the samples in the subthreshold region.

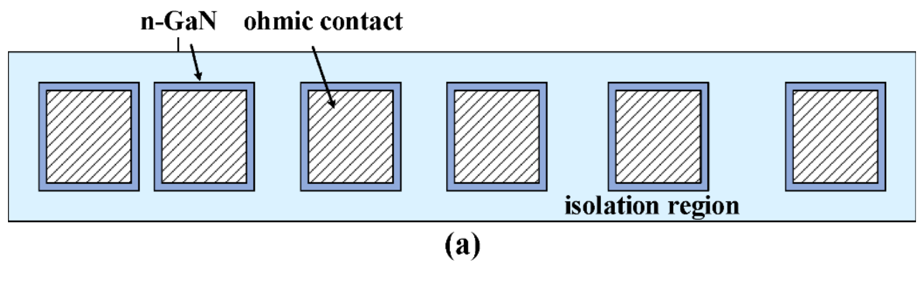
Although GaN MOSFETs on AlGaN/GaN heterostructure with BCl_3 based dry recess achieved a high maximum electron mobility of 141.5 $cm^2V^{-1}s^{-1}$ and a low interface state density, the threshold voltage was still negative. It implies that Si contamination is not the main reason for negative threshold voltage.

2. 3 Evaluation technology for device isolation

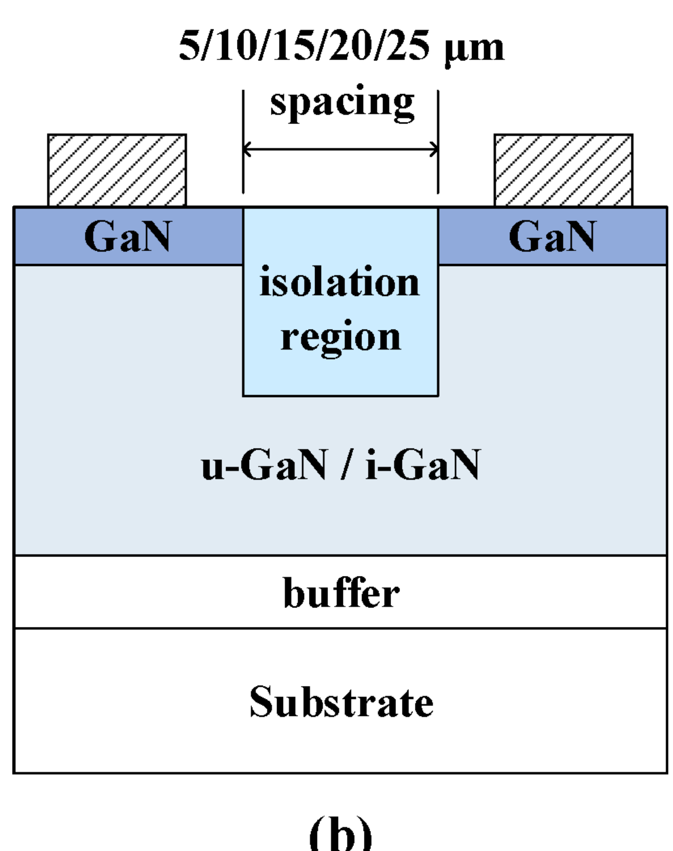
A TLM structure and a special designed MOSFET was used to evaluate the the resistance of isolation region and existence of parasitic MOSFET, respectively.

2. 3. 1 The structure of TLM and test methods

A TLM structure was used to measure the ohmic contact resistance and sheet resistance as shown in Figure 2.14. The ohmic electrodes formed on GaN cap layer or AlGaN layer, and the surrounding area including spacing was formed by different isolation methods. The spacing between each two electrodes were 5 μm, 10 μm, 15 μm, 20 μm, 25 μm, respectively.



(a)



(b)

Figure 2. 14 TLM for characterizing the isolation region. (a) top view; (b) cross-section view.

To obtain high-accuracy measurement, four probes are used in *I–V* test. The resistances *R* between each two electrodes changed with spacing *d*, and were measured by *I–V* test, then *R-d* characteristics was obtained

$$R = \frac{\rho_s d}{W} + \frac{2R_c}{W} \quad (2.4)$$

Where ρ_s is sheet resistance of isolation region (Ω/□), *W* is width of electrodes, and R_c (Ω·mm) is ohmic contact resistance.

2. 3. 2 The structure of MOSFET and test methods

Long-channel linear and circular recessed-gate GaN MOSFETs were used for characterizing the device performance. The parasitic resistance of a long-channel MOSFET can be ignored owing to the large channel resistance. For a circular MOSFET, the possible leakage current along the isolation region can be avoided. But for a linear MOSFET, only an effective isolation region can cut off the leakage current path. The *I–V* characteristics and the estimated electron mobility of the long-channel circular MOSFET can be considered as a reasonable value. Therefore, comparing with I_d-V_g characteristics of a circular device, the isolation effectiveness of a linear device with same recess condition was obtained. If both of I_d-V_g characteristics coincide, demonstrating an effective isolation; if off-state current of a linear device is much higher than the circular device, demonstrating a bad isolation. The electron mobility of linear and circular were under same level if the recess condition was same. If the mobility of a linear device is much larger than that of circular device, there is probably a parasitic MOSFET in the isolation.

Moreover, to examine if a parasitic MOSFET exists in the isolation region, we designed and fabricated another kind of circular and linear MOSFET in the isolation region. To distinguish two kinds of devices, the ordinary recessed-gate MOSFET is termed as R-MOSFET, and this MOSFET used for isolation evaluation is termed as I-MOSFET. Figure 2.15 shows the fabrication processes of I-MOSFET with mesa isolation. The mesa etching and recess etching were conducted simultaneously, namely the recess of I-MOSFET was formed with a mesa isolation condition.

From the I_d-V_g characteristics of a circular MOSFET, the isolation effectiveness was obtained. If this device operated normally, demonstrating an existence of parasitic MOSFET and a bad isolation methods. If the device can’t operate even under a large gate bias, demonstrating no parasitic MOSFET in the isolation region, or at least the parasitic exists but is in off-state under this gate bias. If the device can’t operate and maintain an extremely low drain current close to the level of circular device, which means high-resistivity isolation region was obtained and field isolation succeeds.

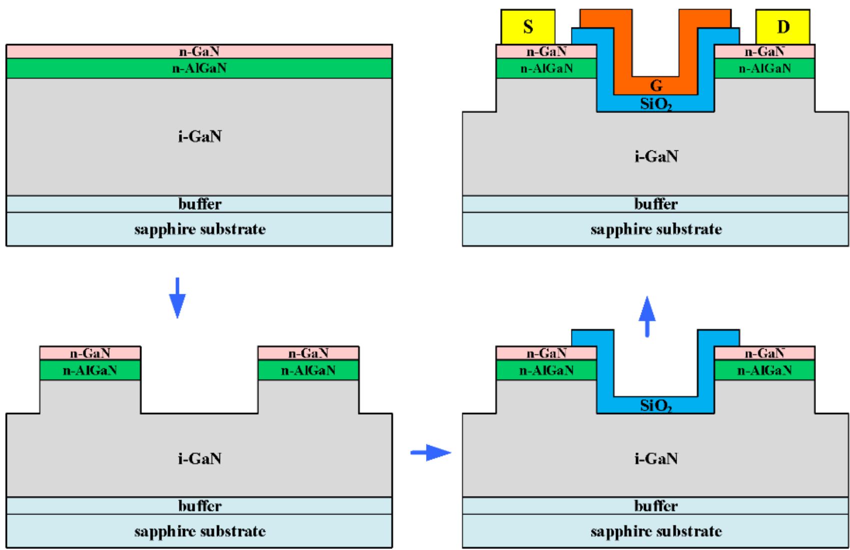


Figure 2. 15 the fabrication processes of I-MOSFET with mesa isolation

2. 4 Summary

In this chapter, the basic structure and fabrication processes, test methods and evaluation technology of isolation effectiveness for AlGaN/GaN HFET and GaN MOSFETs were described in details. On the basis of the fabrication processes of GaN-based FETs, device performances were characterized through *I–V* and *C–V* measurements, and the processes isolation effectiveness was evaluated through the TLM structure and special MOSFETs fabricated in the isolation regions. In the TLM structure, the regions between every two ohmic electrodes were formed by different isolation processes, and the processes isolation effectiveness were evaluated by sheet resistance measurements or *I–V* characteristics of these regions. The circular MOSFETs were fabricated in the isolation regions to examine the existence of a parasitic MOSFET by *I–V* characteristics. The circular and linear MOSFETs with same fabrication processes were fabricated, the effectiveness of isolation processes was evaluated through comparing their transfer characteristics, and the effect of field implantation on device performance was investigated through calculating the field-effect electron mobility and D_{it} at SiO_2/GaN interface. This work solved the problem of evaluating the device isolation effectiveness and laid a foundation of developing and improving isolation processes purposefully.

Chapter 3 O_2 plasma treatment for device isolation of AlGaN/GaN HFET

3.1 O_2 plasma treatment process

To eliminate the dry etching damage and reduce the leakage current of AlGaN/GaN HFET, a process of dielectrics filling (Si_3N_4, SiO_2, Sc_2O_3) or surface treatment (N_2/H_2 treatment, UV ozone, oxygen plasma) is added. In these processes, O_2 plasma treatment is relatively easy and feasible because dielectrics deposition or lithography step is not needed and O_2 plasma can be generated by a PECVD system. In this chapter, we studied the influence of O_2 plasma treatment on the mesa-isolated region of AlGaN/GaN HFETs by using the PECVD system.

3.1.1 Process flow of O_2 plasma treatment

A 2 µm-thick undoped GaN (u-GaN) layer grown on a sapphire substrate was used in the experiments. A 30 nm-thick n-GaN cap layer was deposited on the u-GaN to form the ohmic electrodes. The process flow includes ohmic contact, mesa formation, and O_2 plasma treatment. Figure 3.1 shows the structure for characterizing the mesa-isolated region. The current between the two ohmic electrodes is called isolation current.

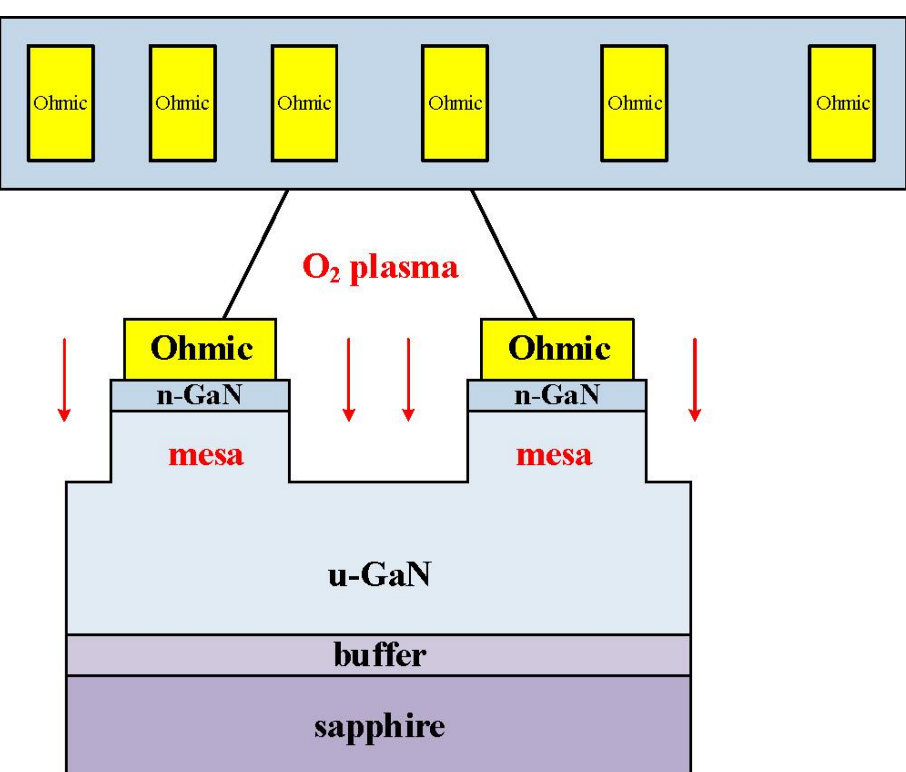


Figure 3. 1 The TLM structure for characterizing the mesa-isolated region.

A metal stack of Ti/Al/Ti/Au (50/200/40/40 nm) was subjected to a lift-off process to fabricate ohmic electrodes and annealed at 850 ℃ for 1 min in nitrogen ambient. A mesa structure was formed through ICP dry etching with a $SiCl_4$ gas flow of 3 sccm, ICP power of 100 W, bias power of 20 W, and working chamber pressure of 0.25 Pa to achieve device isolation. The etching rate under this condition was approximately 1.2 nm/min, and the etching mask was 2 μm positive photoresist (HPR-1183L, Fujifilm Corp., Minato, Tokyo, Japan). The mesa depth was approximately 90 nm. After dry etching, a HNO_3:HF buffered solution (BHF; 1:1, volume ratio) was used to remove possible Si contaminants on the etched surface. The samples were then exposed to O_2 plasma or O_2 gas in the PECVD chamber (PD-220LC, Samco, Inc., Fushimi, Kyoto, Japan) under different experimental conditions, as listed in Table 3.1. For all conditions, the chamber pressure was 80 Pa and the O_2 flow rate was 300 sccm. In condition D, the chemical vapor deposition (CVD) power was 0 W, which indicates that no plasma was generated; this condition was designated as O_2 gas treatment.

Table 3. 1 List of O_2 plasma and O_2 gas treatment conditions in the PECVD chamber.

Condition	Temperature (°C)	Time (min)	CVD power (W)	Pressure (Pa)	Flow rate of O_2 (sccm)
A	300	15	250	80	300
B	200	15	250	80	300
C	100	15	250	80	300
D	300	15	0[a]	80	300
E	300	15	50	80	300
F	300	15	150	80	300
G	300	25	250	80	300
H	300	5	250	80	300

[a]The CVD power of 0 W means that no plasma was generated and condition D was O_2 gas treatment.

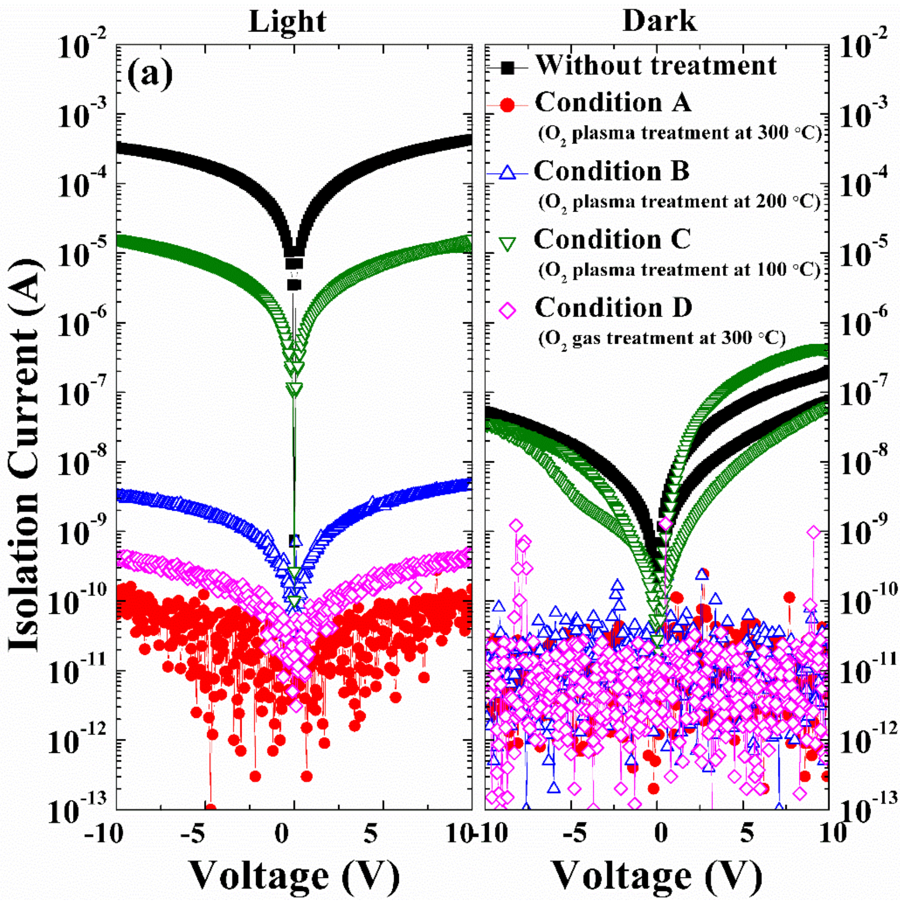
3.1.2 Selection of O_2 plasma treatment conditions

The *I–V* measurement of the mesa-isolated region with 25 μm spacing was conducted for all the samples under dark condition and visible light (light from a halogen lamp in the microscope), respectively. Figure 3.2a shows *I–V* characteristics of the mesa-isolated region with conditions A, B, C and D. A sample without any treatment (as-etched u-GaN layer) was used for comparison.

Under dark conditions, isolation current in condition C (O_2 plasma treatment at 100 ℃)

was approximate 10^{-7} A and similar to that in condition without treatment. This finding demonstrates that O_2 plasma treatment at 100 ℃ did not affect isolation current. Meanwhile, isolation currents in condition A (O_2 plasma treatment at 300 ℃), B (O_2 plasma treatment at 200 ℃) and D (O_2 gas treatment at 300 ℃) reduced by four orders of magnitude to approximately 10^{-11} A. Testing under visible light revealed that isolation current in condition A (lower than 10^{-10} A) was lower than that in conditions B and D. This result implies that O_2 plasma treatment at 300 ℃ suppressed the photovoltaic response by completely oxidizing the dry damaged GaN layer. In addition, as shown in Figure 3.2b and 3.2c, isolation current did not differ among conditions A, E, F, G, and H. Therefore, the oxidation process is strongly dependent on treatment temperature, rather than treatment time and CVD power.

Therefore, to maintain an effective isolation process, we used condition A (O_2 plasma treatment at 300 ℃ for 15 min at 250 W) for subsequent experiments.



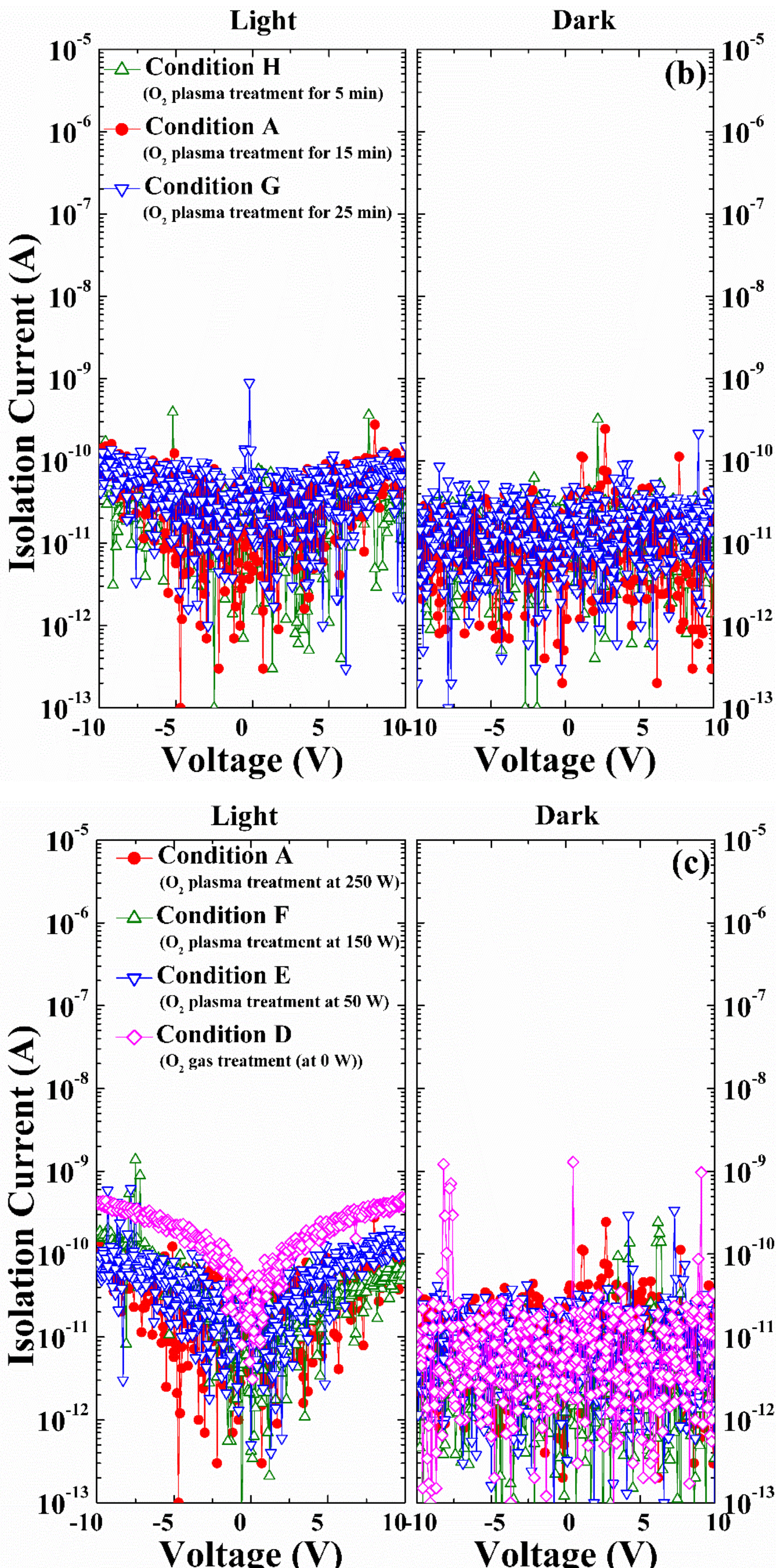


Figure 3. 2 *I–V* characteristics of the mesa-isolated region with different conditions, (a) under different temperature, (b) for different time, and (c) at different power.

3.1.3 The influence of O_2 plasma treatment on ohmic contacts

A TLM structure with 2DEG layer was also fabricated as shown in Figure 3.3. The epitaxial layers were grown on a sapphire substrate, which consisted of a buffer layer, a 2 μm-thick u-GaN layer, 25 nm-thick u-AlGaN layer, and a 2–3 nm-thick n-GaN cap layer . The mesa isolation with same condition was used to achieve electrical isolation. The sheet resistance and ohmic contact resistance were measured before and after O_2 plasma treatment. As Table 3.2 listed, after O_2 plasma treatment, the sheet resistance of 2DEG layer decreased because the oxidation of GaN surface changed the polarity intensity of the material. And the ohmic contact resistance increased slightly, which had little influence on the DC performance of AlGaN/GaN HFET.

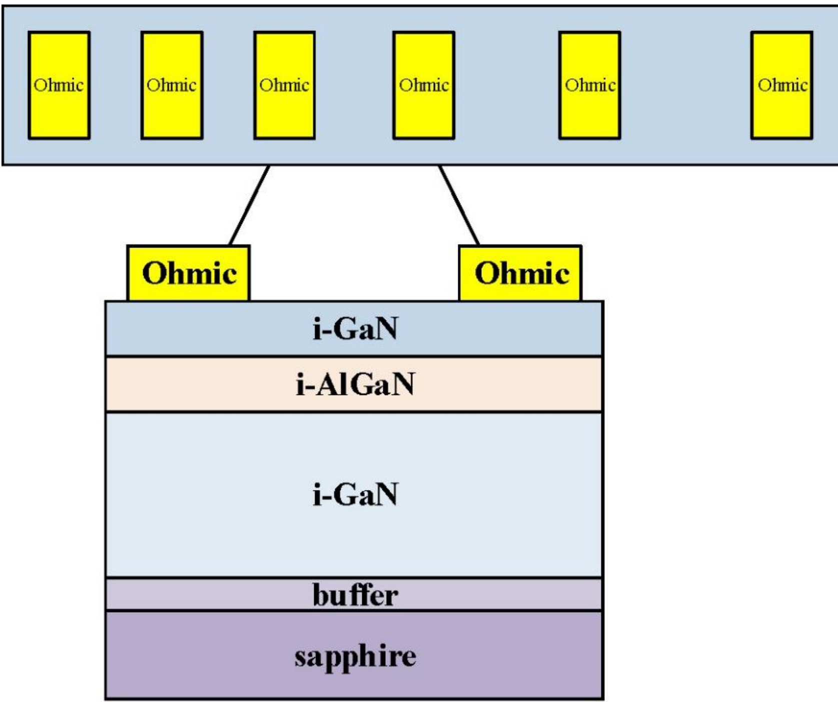


Figure 3. 3 The TLM structure with 2DEG layer.

Table 3. 2 The sheet resistance and ohmic contact resistance measured before and after O_2 plasma treatment.

	Before treatment	After treatment
Sheet resistance R_s (Ω/□)	0.87	1.12
Ohmic contact resistance R_c (Ω·mm)	599	554

3.1.4 The influence of dry etching conditions on treatment results

In our previous work[94], the mesa etching was conducted by two-step condition. The first step was done by $SiCl_4$ gas with a flow rate of 4 sccm, ICP power of 50 W, bias power of 100 W and at a working chamber pressure of 0.25 Pa. The second step was done by Cl_2 gas with a flow rate of 4 sccm, ICP power of 50 W, bias power of 50 W and at a working chamber pressure of 0.25 Pa. the average etching rate was about 20 nm/min. The O_2 plasma treatment was employed to the mesa surface formed under this condition, and Figure 3.4 shows *I*–*V* results. The isolation current in the condition of mesa etching with two steps was about 10^{-6} A. After O_2 plasma treatment at 300 ℃ for 30 min, the isolation current was only reduced one order of magnitude due to the serious damage induced by Cl_2 etching. A second dry etching with condition A was performed for 30 min on the same sample, the isolation current almost didn't change meaning that the damage induced by condition A was lower than two-step etching. After second O_2 plasma treatment at 300 ℃ for 15 min, the isolation current was reduced to around 10^{-8} A. The possible reason is that the first etching damage still existed even the second etching depth was approximated 36 nm.

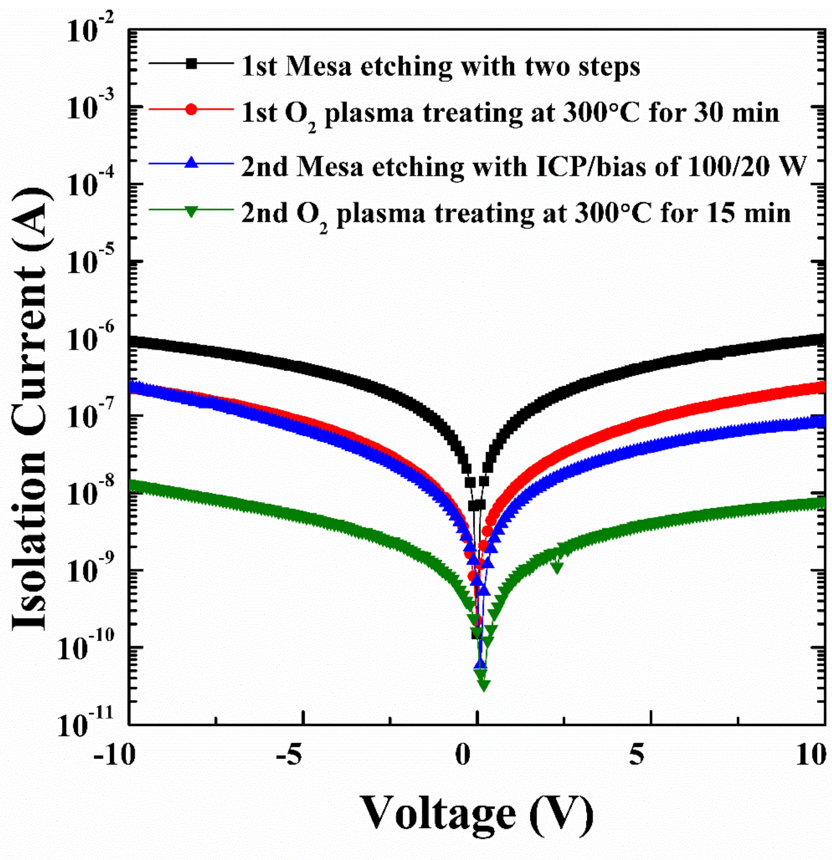


Figure 3. 4 *I*–*V* characteristics of the mesa-isolated region with two-step mesa etching.

3.1.5 Breakdown characteristics of isolation region treated by O_2 plasma

The breakdown characteristics of the mesa-isolated region without treatment and treated under condition A were determined using the structures presented in Figure 3.1 with 5 μm spacing. As shown in Figure 3.5, breakdown voltages of 171.5 and 467.2 V were confirmed for samples without treatment and treated under condition A. Isolation current reduced by several order of magnitudes through O_2 plasma treatment, and breakdown voltage significantly improved.

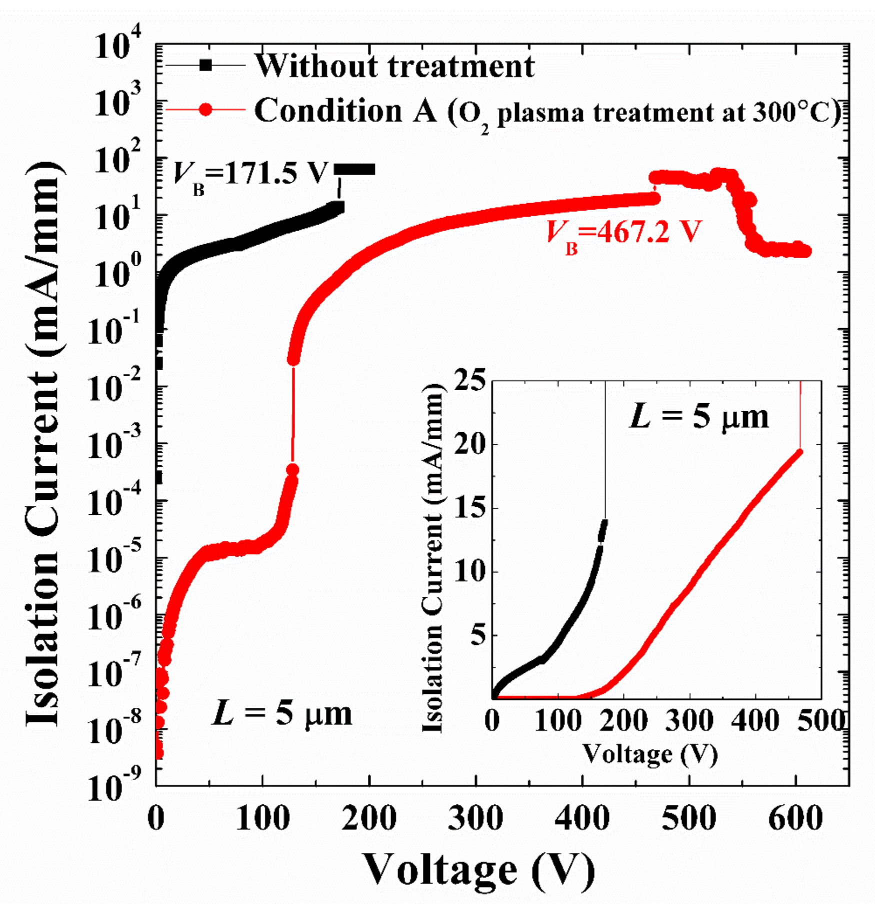


Figure 3. 5 Breakdown characteristics of the mesa-isolated region without treatment and treated by condition A.

3.2 Analysis of oxidized etching surface

O_2 plasma treatment on the Schottky gate region of AlGaN/GaN HFET was reported by many groups [103-109], whereas a few work was focused on O_2 plasma treatment on mesa surface [80, 110, 111], and the oxidation mechanism was not clear yet. To clarify the oxidation mechanism of O_2 plasma treatment, PL spectrum was used to investigate the variation in defect

levels on the etched GaN surface before and after O_2 plasma or O_2 gas treatment, XPS was then conducted to investigate chemical property variation induced by O_2 plasma treatment on the etched u-GaN surface.

3.2.1 PL spectrum analysis

PL spectroscopy is a non-contact and no-damage method used for detection on electronic structure of materials. Photoluminescence is using light as an excitation, the electrons in the material turn to the excited state after absorbing the energy of photons, when the electrons transited back to the equilibrium state, then they will emit photons. The wavelength of emitted photons is relevant to the energy level difference between the excited state and the equilibrium state, the numbers of emitted photons are relevant to the relative contribution of radiation. During the transition of electrons come back to the equilibrium state, there are six different recombination centers emitting photons, free-carrier recombination as intrinsic centers is the recombination between the electrons from the bottom of conduction band and the holes from the top of valence band. Therefore, using PL Spectra, the band-gap of sample was obtained through the detection on the light emitted by free-carrier recombination.

PL spectrum excited with a 325 nm He-Cd laser were measured at room temperature. Figure 3.6 shows the PL spectra from samples without treatment and treated under condition A (O_2 plasma treatment at 300 ℃) and D (O_2 gas treatment at 300 ℃). The inset shows the near band-edge luminescence of samples without treatment and treated under conditions A and D, with peaks at 3.46 eV, 3.47 eV, and 3.46 eV, respectively. For samples without treatment, a so-called yellow luminescence (YL) band expanded from 1.6 eV to 2.6 eV and centered near 2.2 eV. This broad luminescence band could be attributed to transition from a shallow donor to a deep acceptor [112, 113]. The shallow donor of the etched u-GaN may be the etching damage of the nitrogen vacancy V_N according to our previous work [101, 114], whereas the deep acceptor may be the native defect of the gallium vacancy V_{Ga} [115-117]. The near band-edge luminescence intensity of all the samples was weaker than the YL intensity, which could be primarily attributed to the non-radiative centers at low doping concentrations in the u-GaN layer [118-120]. The ripples visible in the YL band from samples without treatment (Figure 3.6) are attributed to the effect of microcavity formed by the GaN-air and the GaN-substrate interface [121].

After treatment under condition D, the YL band narrowed from 1.7 eV to 2.3 eV and the PL intensity was slightly reduced. After treatment under condition A, the luminescence band shifted from 1.8 eV to 2.65 eV and the PL intensity decreased, with the maximum peak located

at 2.28eV (YL band). The decrease in the PL intensity implies a decrease in the density of defects related to YL. A reasonable explanation is that, O_2 plasma treatment at 300 ℃ oxidized a large number of extra gallium atoms on the etched surface, resulting in elimination of nitrogen vacancy. By contrast, O_2 gas treatment at 300 ℃ oxidized only a small number of extra gallium atoms and thus only a small amount of nitrogen vacancy was eliminated. After treatment under condition A, a new peak with a low PL intensity located at 2.88 eV appeared in the blue luminescence (BL) band; this peak could be attributed to oxygen terminating the site of nitrogen vacancy and forming substitutional oxygen on the nitrogen site (O_N) as a shallow donor [117]. This BL band in u-GaN may be due to the transition from O_N to V_{Ga}-related complex [122-124].

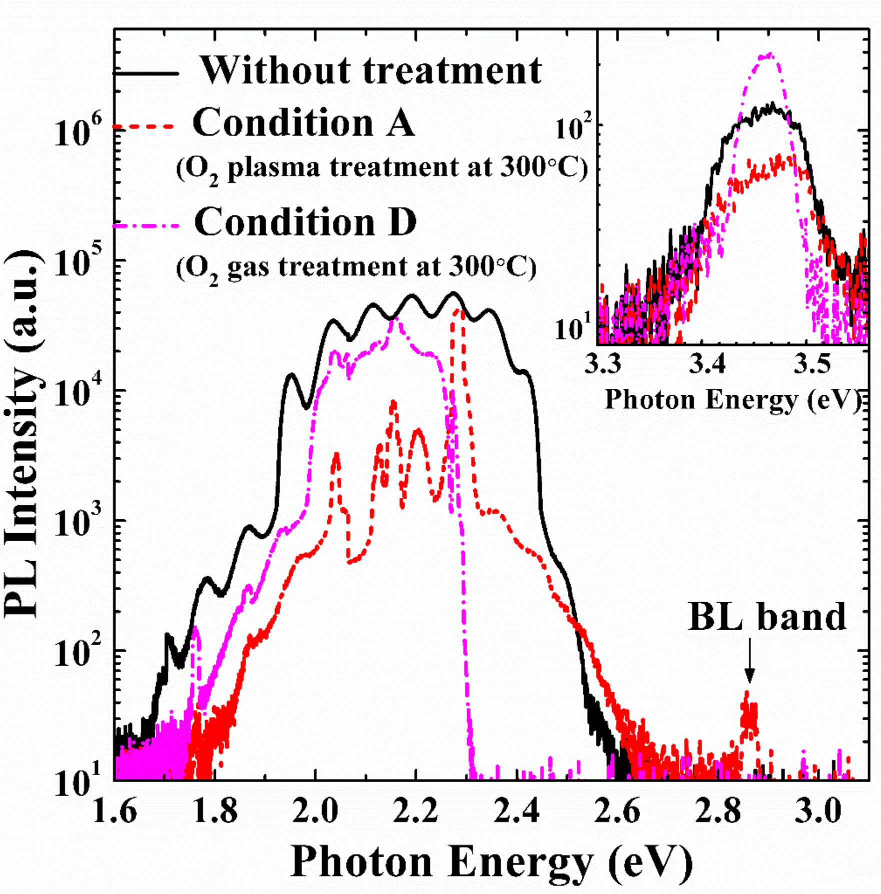


Figure 3. 6 PL spectrum at room temperature of all the samples. The inset shows the near band-edge luminescence band.

3.2.2 XPS analysis

XPS, also known as Electron Spectroscopy for Chemical Analysis (ESCA), is the most widely used surface analysis technique to obtain composition and chemical state information from the surfaces of solid material. XPS is a surface sensitive technique because only those electrons generated near the surface escape and are detected. The average depth of analysis for an XPS measurement is approximately 5 nm.

XPS is typically accomplished by exciting a samples surface with mono-energetic Al kα or Mg kαx-rays causing photoelectrons to be emitted from the sample surface. An electron energy analyzer is used to measure the energy of the emitted photoelectrons. From the binding energy and intensity of a photoelectron peak, the elemental identity, chemical state, and quantity of a detected element can be determined. Spatial distribution information can be obtained by scanning the micro focused x-ray beam across the sample surface. Depth distribution information can be obtained by combining XPS measurements with ion milling (sputtering) to characterize thin film structures.

In our experiments, the XPS system was equipped with a monochromatic Al Kα radiation source (hv = 1486.6 eV), and the C1s peak of adventitious carbon (284.8 eV) was used for calibration. XPS data were analyzed after Shirley background subtraction, and the peaks were fitted using a sum of Gaussian and Lorentzian functions (at fixed 30% Gaussian). Figure 3.7 shows the core level spectra of Ga 3d, N 1s and O 1s for all the samples.

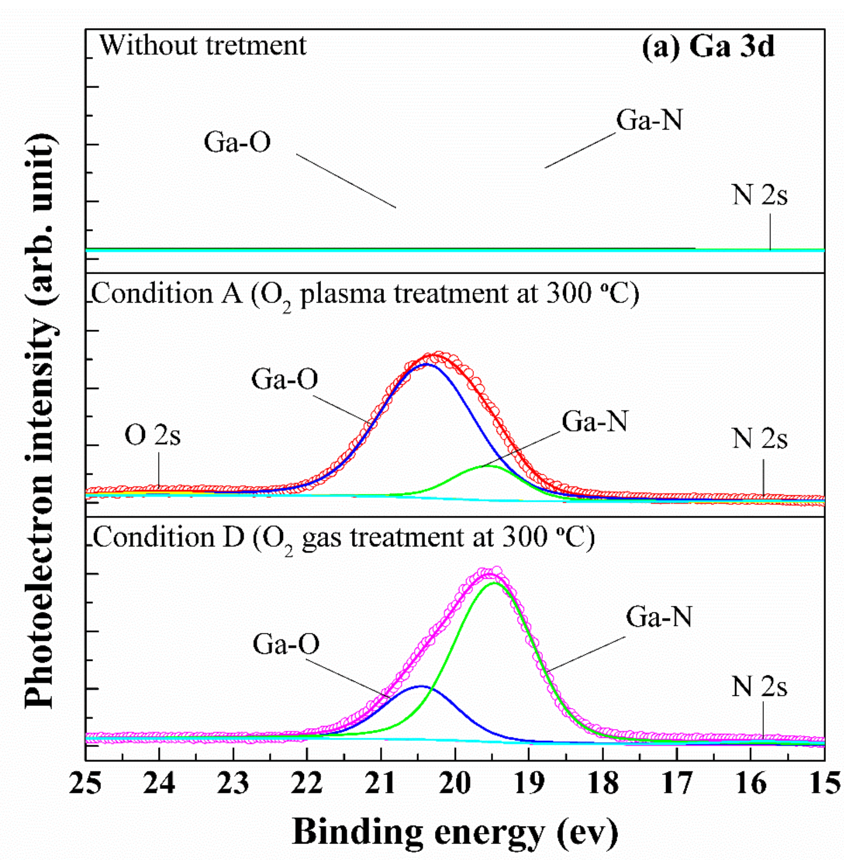
In Figure 3.7a, the Ga 3d peak can be deconvoluted into two contributions attributed to Ga–N bond at 19.3 ±0.1 eV (full width at half maximum {FWHM} 1.1 ±0.2 eV) and Ga–O bond at 20.3 ±0.1 eV (FWHM 1.2 ±0.2 eV) [125-128], with the Ga $3d_{3/2}$–Ga $3d_{5/2}$ spin–orbit splitting at 0.44 eV [129]. The peaks at 15.8 eV and 24.0 eV are assigned to the N 2s and O 2s lines, respectively [129, 130].

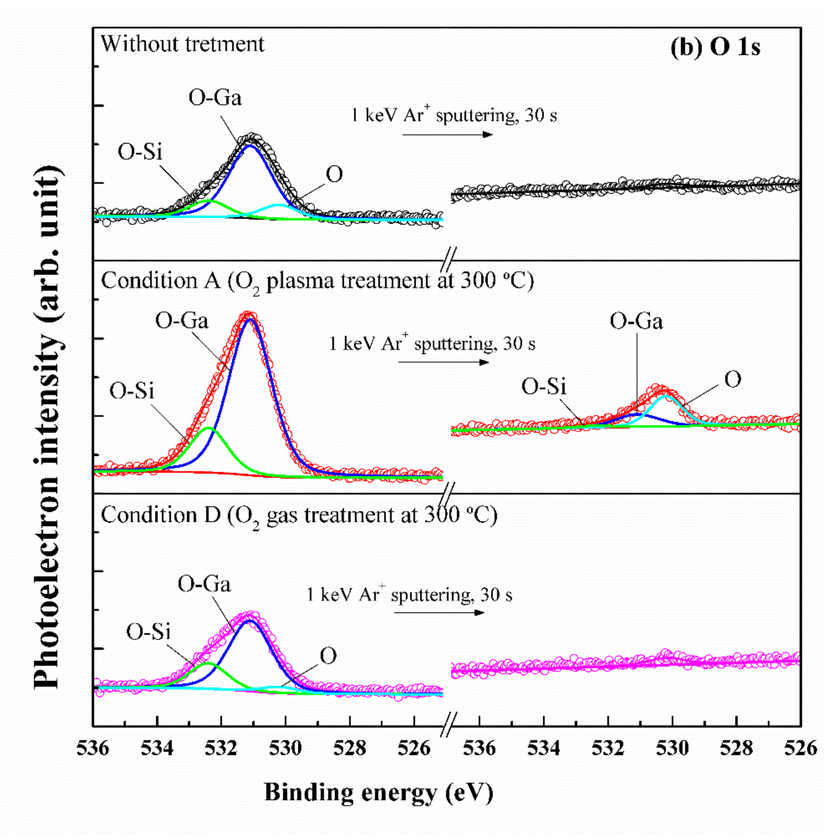
In Figure 3.7b, the O 1s peak can be deconvoluted into three contributions attributed to O–Ga bond (Ga_2O_3) at 531.1 eV (FWHM 1.6 eV), O–Si bond at 532.4 eV (FWHM 1.4 eV), and a less covalent form of oxygen bond at 530.2 eV (FWHM 1.4 eV) [125, 127, 131, 132]. The silicon component was probably derived from contamination during dry etching, and the binding energy corresponds to the partially oxidized silicon Si^{2+} at 101.7 eV in Si 2p spectrum [133].

As shown in Figure 3.7c, the N 1s spectrum overlapped with the Ga $L_2M_{45}M_{45}$ Auger electron spectrum because of Al Kα excitation. The N 1s peaks can generally be deconvoluted into four contributions, namely, N–Ga bond at 397.1 ±0.2 eV (FWHM 1.1 eV), N-H_2 bond at 397.7 ±0.2 eV (FWHM 2.5 ±0.2 eV), and Ga Auger peaks at 395.3 ±0.2 eV (FWHM 3.0–3.7

eV) and 392.1 ± 0.2 eV (FWHM 2.5 ± 0.1 eV) [127, 128, 131, 134, 135].O_2 plasma-treated sample exhibited Ga–O peak intensity higher than that of the other treatments and presented an O 2s peak. In the O 1s spectra of O_2 plasma-treated sample, the O–Ga peak intensity was higher than that of the other treatments and the less covalent form of oxygen bond did not appear. This finding perhaps explains the difference between O_2 plasma and O_2 gas oxidation; that is, the former can completely oxidize the GaN surface, whereas the latter can only partially oxidize the GaN surface.

After 1 keV Ar ion sputtering for 30 s, the O 1s peaks of the as-etched and O_2 gas-treated samples almost disappeared, whereas the O 1s peak of O_2 plasma-treated samples significantly diminished and the less covalent form of oxygen peak appeared. The occurrence of the peak corresponding to the less covalent form of oxygen could be due to Ar ion bombardment that broke O–Ga and O–Si bonds. As such, large amount of Ga_2O_3 were formed by O_2 plasma treatment at 300 ℃ than that by O_2 gas treatment at 300 ℃. The thickness of Ga_2O_3 was estimated to be a few nanometers [136].





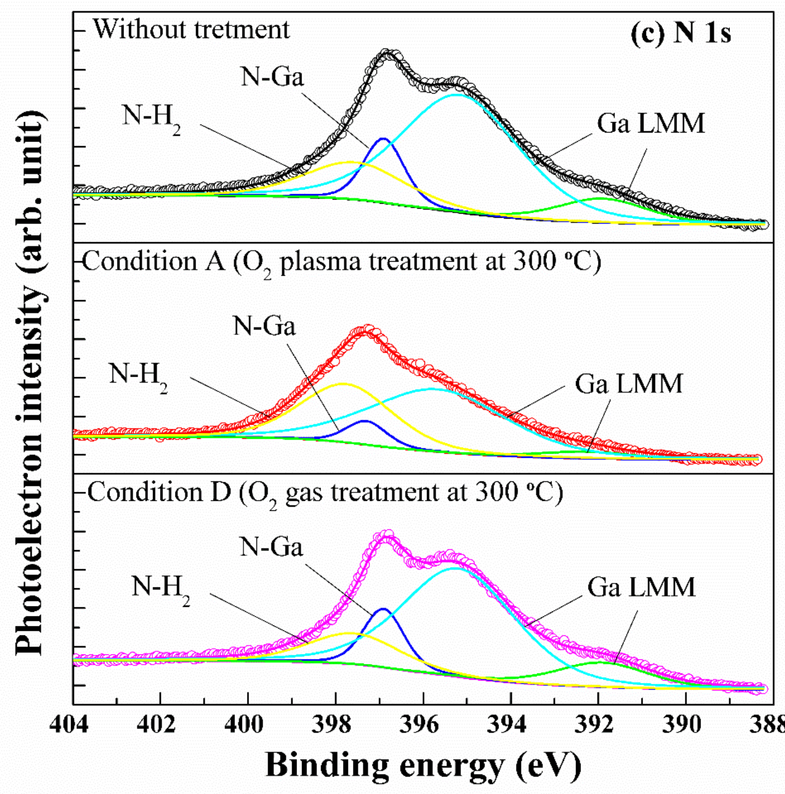


Figure 3. 7 the core level spectra of Ga 3d, O 1s and N 1s for all the samples.

For O_2 plasma-treated samples, the intensities of the N–Ga and Ga *LMM* Auger peaks were lower than that of the other peaks. The main reason is that gallium nitride was oxidized and Ga_2O_3 was formed. Aside from the increase in oxygen content, another possible reason for the decrease in nitrogen content is that some nitrogen atoms were substituted by oxygen atoms, leading to the formation of O_N as evidenced by the occurrence of the BL band of O_2 plasma-treated sample in the PL spectra.

3.3 AlGaN/GaN HFET using O_2 plasma treatment

3. 3. 1 Fabrication process flow of AlGaN/GaN HFET using O_2 plasma treatment

The AlGaN/GaN HFETs were fabricated on sapphire and silicon substrate with six kinds of wafer samples, as listed in Table 3.3. Sample 1-4 are grown on sapphire substrate, sample 5 and 6 are grown on silicon substrate, sample 1-3 and 6 have a GaN cap layer. The sheet resistance and ohmic contact resistance were measure using TLM structure with 2DEG layer after O_2 plasma treatment.

Table 3. 3 Wafer samples used for AlGaN/GaN HFET.

Sample	No. 1	No. 2	No. 3	No. 4	No. 5	No.6
Layer 4	u-GaN 5 nm	i-GaN 5 nm	i-GaN 2-3 nm			i-GaN 2-3 nm
Layer 3	u-AlGaN 20 nm	i-AlGaN 20 nm	i-AlGaN 25 nm	i-AlGaN 25 nm	i-AlGaN 25 nm	i-AlGaN 25 nm
Layer 2	u-GaN 8 um	i-GaN 10 um	i-GaN 2 um	i-GaN 2 um	i-GaN 1 um	i-GaN 1 um
Layer 1	buffer	nucleation	nucleation	buffer	buffer	buffer
Substrate	sapphire	sapphire	sapphire	sapphire	Si	Si
Sheet resistance (Ω/□)	547	487	554	443	959	1219
Ohmic contact resistance (Ω·mm)	1.67	1.62	1.12	12.06	1.96	2.94

The device fabrication process was based upon the standard photolithography and lift-off technologies. The mesa structure was formed through ICP dry etching with a $SiCl_4$ gas flow of 3 sccm, ICP power of 100 W, bias power of 20 W, and working chamber pressure of 0.25 Pa. The etching mask was 2 μm PR, the mesa depth was approximately 90 nm. After dry etching, a HNO_3:HF buffered solution (BHF; 1:1, volume ratio) was used to remove possible Si contaminants on the etched surface. The ohmic contacts of Ti/Al/Ti/Au (50/200/40/40 nm) were

formed and annealed at 850 ℃ for 1 min in nitrogen ambient. The samples were then exposed to O_2 plasma at 300 °C for 15 min in PECVD, the chamber pressure was 80 Pa and the O_2 flow rate was 300 sccm. Finally, a Ni/Au (70/30 nm) bilayer was deposited as the gate metal.

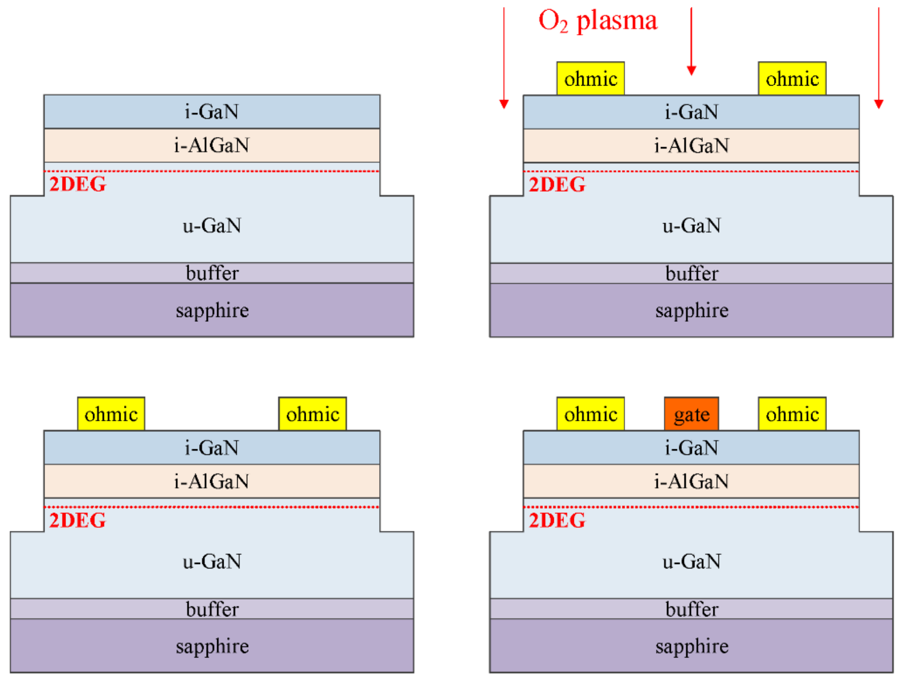


Figure 3. 8 The fabrication process of AlGaN/GaN HFET with mesa isolation and O_2 plasma treatment.

3. 3. 2 Characterization of AlGaN/GaN HFET using O_2 plasma treatment

Figure 3.9 presents the plots of the drain-source *I–V* characteristics of AlGaN/GaN HFETs treated under condition A (O_2 plasma treatment at 300 ℃) on all the samples. All the HFETs can normally operate under gate voltage of 1 to -5 V. The devices on sample 3 and 4 presented larger on-state current because of a high intensity of 2DEG due to a thicker i-AlGaN layer [137]. The devices on sample 5 and 6 presented a lowest on-state current because using silicon substrate caused a relative poor GaN epitaxy film and a relative low intensity of 2DEG. An apparent hysteresis induced by the so-called current collapse was observed in the devices on sample 1 and 2. During O_2 plasma treatment, the active region was also oxidized because the surface of the active layer was not protected. Traps were probably induced on the surface of the AlGaN layer or in the AlGaN/GaN heterostructure [109]. And these two samples were more sensitive to the treatment comparing with others. As such, protecting the active layer during treatment and effectively cleaning the surface before gate formation may improve the process.

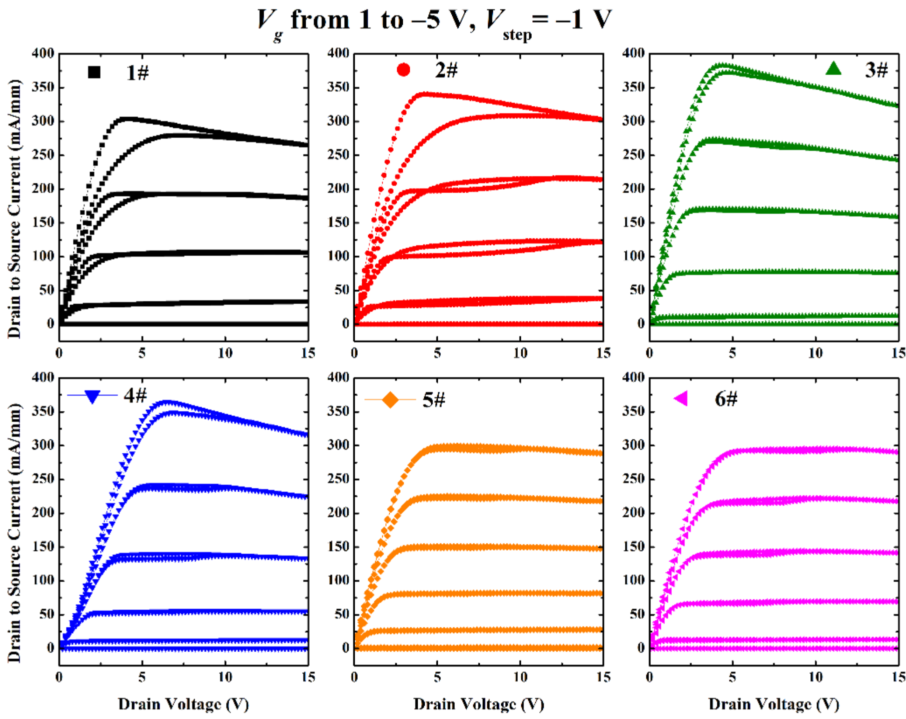


Figure 3. 9 *I–V* characteristics of AlGaN/GaN HFETs with O_2 plasma treatment on all the samples.

Figure 3.10 shows the transfer characteristics of AlGaN/GaN HFETs with O_2 plasma treatment on all the samples. For sample 3, under a gate voltage of 2 V and a drain voltage of 10 V, the on-state drain current I_{on} reached 346.6 mA/mm and the off-state drain current I_{off} was lower than 2×10^{-5} mA/mm. Thus, an on/off drain current ratio of 1.73×10^{7} was achieved by O_2 plasma treatment, which was substantially improved compared with that of traditional AlGaN/GaN HFETs with a typical off-state current of 10^{-1}–10^{-3} mA/mm under similar fabrication process [138]. Figure 3.11 shows the transconductance G_m of AlGaN/GaN HFETs with O_2 plasma treatment on all the samples. The devices on sample 5 and 6 presented the lowest G_m, and other devices presented the apparent hysteresis. Figure 3. 12 shows the I_g-V_g characteristics of AlGaN/GaN HFETs with O_2 plasma treatment on all the samples. The gate leakage current of all the samples were in the range of 10^{-5} to 10^{-3} mA/mm due to the Ni/Au Schottky gate.

The breakdown characteristics of the mesa-isolated region treated by O_2 plasma on all the samples were determined using the structures presented in Figure 3.1 with 5 μm spacing. As shown in Figure 3.13, the devices on sample 5 and 6 presented the lowest breakdown voltage due to the poor quality of GaN film. The device on sample 3 demonstrated a largest breakdown voltage of 467.2 V as mentioned in section 3.1.5.

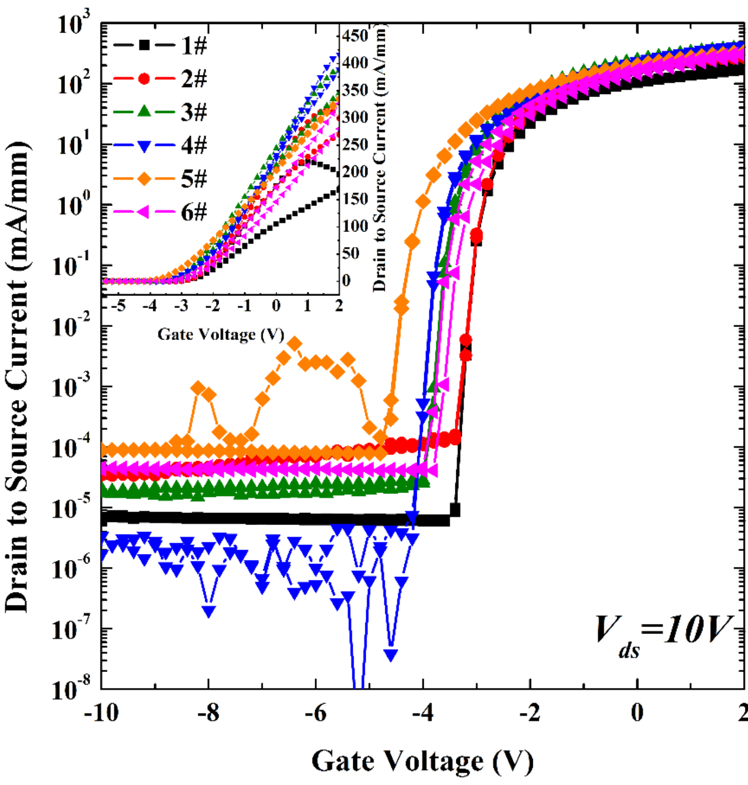


Figure 3. 10 The transfer characteristics of AlGaN/GaN HFETs with O_2 plasma treatment on all the samples.

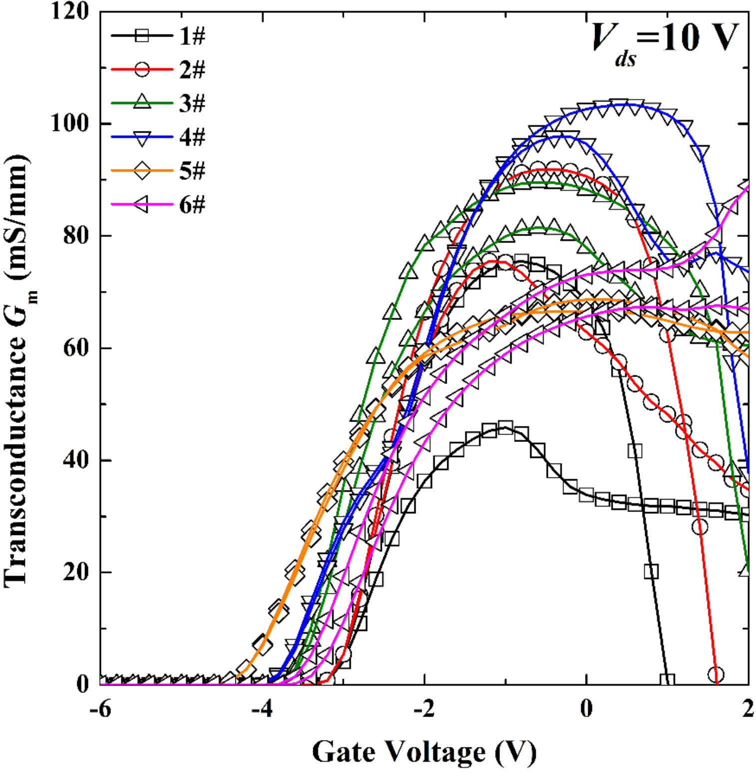


Figure 3. 11 The transconductance of AlGaN/GaN HFETs with O_2 plasma treatment on all the samples.

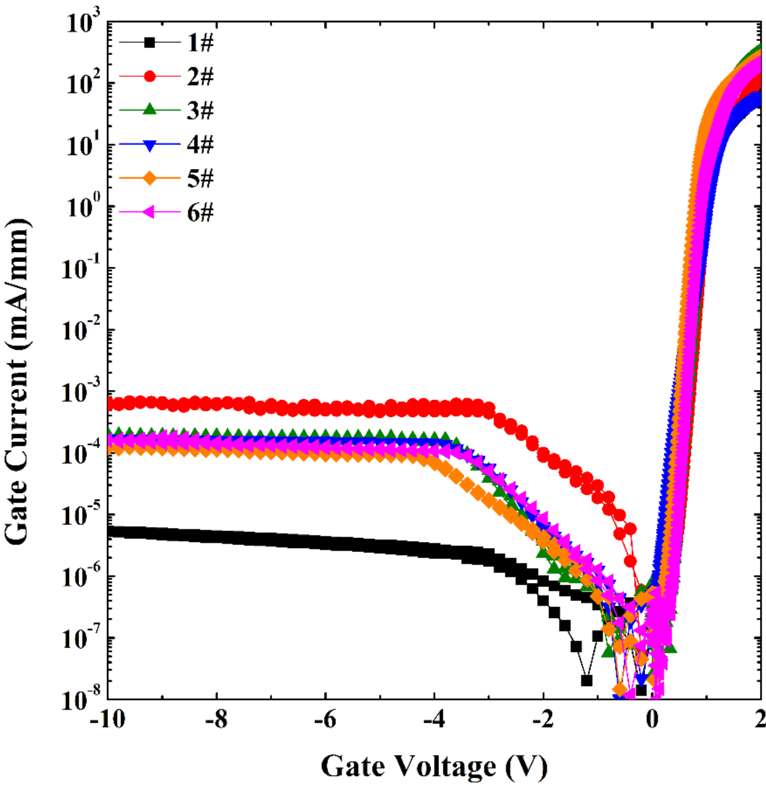


Figure 3. 12 The I_g-V_g characteristics of AlGaN/GaN HFETs with O_2 plasma treatment on all the samples.

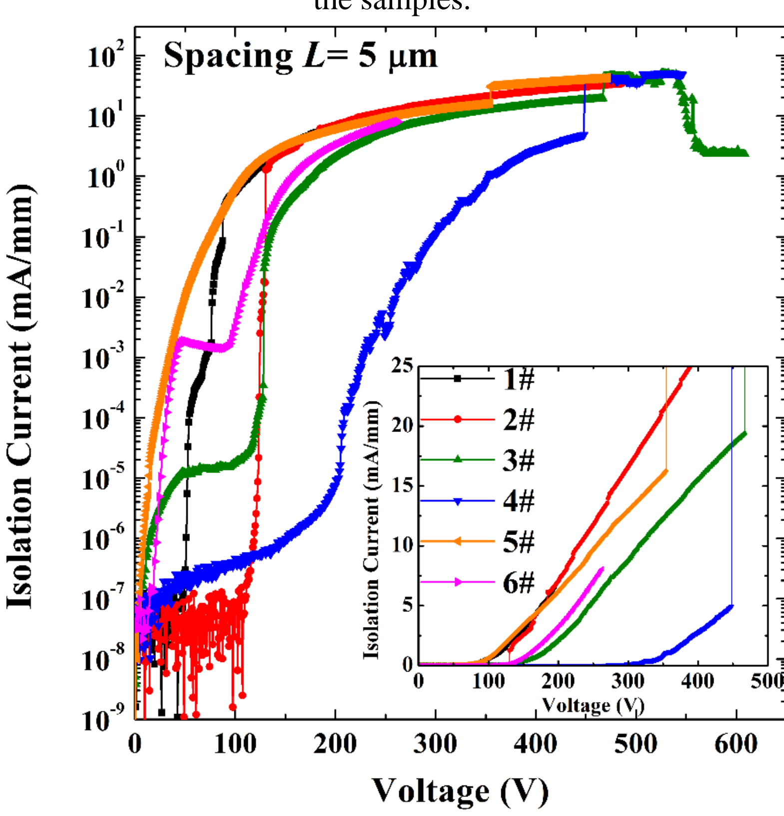


Figure 3. 13 Breakdown characteristics of the mesa-isolated region treated by O_2 plasma on all the samples.

3.4 Summary

In this chapter, the isolation effectiveness and oxidation mechanism of O_2 plasma treatment for AlGaN/GaN HFETs were studied. The process of O_2 plasma treatment on the mesa-isolated region of AlGaN/GaN HFETs was adopted, the optimal condition was established by *I–V* measurement on TLM structure, the oxidation effectiveness and mechanism of the mesa etching surface were analyzed through PL spectrum and XPS, and AlGaN/GaN HFETs with O_2 plasma treatment were fabricated and characterized. The *I–V* results of TLM structure indicated that the isolation current were strongly dependent on treatment temperature and the depth of etching damage. Treatment at 300 ℃ was confirmed to be the optimal condition, under which isolation current was reduced by four orders of magnitude to 10^{-11} A and photovoltaic response was suppressed, and the breakdown voltage of the mesa-isolated region increased from 171.5 to 467.2 V. The PL spectrum analysis showed a decrease in the density of defects related to the YL band and the occurrence of defects related to the BL band. XPS results showed that O_2 plasma treatment can form high amounts of Ga_2O_3 than O_2 gas treatment, and the defect of O_N was probably formed. The *I–V* characteristics of AlGaN/GaN HFETs presented a high on/off drain current ratio of 1.73×10^7. This work provided an effective process of O_2 plasma treatment for device isolation in AlGaN/GaN HFETs, identified a probably formation of defect, and gave reference for the further improvement in device performance.

4 Boron ion implantation as field isolation process for GaN MOSFET

For compound semiconductors, ion implantation, in addition to forming doped region, is usually used to achieve device isolation by eliminating the 2DEG in AlGaN/GaN heterojunction. However, there is no report on the device field isolation on GaN MOSFET. For field isolation, ion implantation is an attractive method to introduce significant lattice damage, leading to defect generation, and a formation of high resistivity region to avoid the surface channel formation along the isolation region. We investigated an isolation process of boron ion implantation for GaN MOSFETs, and boron ion implantation is expected to prevent the formation of parasitic MOSFET on isolation region and achieve field isolation.

4.1 Simulation of ion implantation profile

The investigated implantation conditions are the implantation dose of 7×10^{14}, 1×10^{15}, 1×10^{14} cm^{-2} at 110 keV and 5×10^{14}, 1.4×10^{15}, 1.4×10^{14} cm^{-2} at 30 keV, respectively. The energy/dose of 110 keV/7×10^{14} cm^{-2} and 30 keV/5×10^{14} cm^{-2} is a condition for the device isolation on AlGaN/GaN heterostructure. The implanted boron ions profile can be approximated by a Gaussian distribution function [139]:

$$n(x)=\frac{S}{\sqrt{2\pi}\sigma_{\mathrm{p}}}\exp\left[-\frac{(x-R_{\mathrm{p}})^2}{2{\sigma_{\mathrm{p}}}^2}\right] \quad (4.1)$$

where x is the distance in implanted layer, S is the ion dose per unit area, R_{p} is the projected rage, σ_{p} is the projected struggle. With a reference to Transport of Ions in Matter (TRIM) ion stopping and range tables, the implantation depth was estimated as 490 nm on the condition that 99.99% of ions were distributed in the area from the implant surface to the distance of 490 nm. Using Gaussian distribution function, it can be also confirmed that the mask of double layers of 2 μm PR (HPR 1183L, Fuji film) and 500 nm SiO_2 was thick enough to stop 99.99% of ions and protect the non-implantation region, as shown in Figure 4.1.

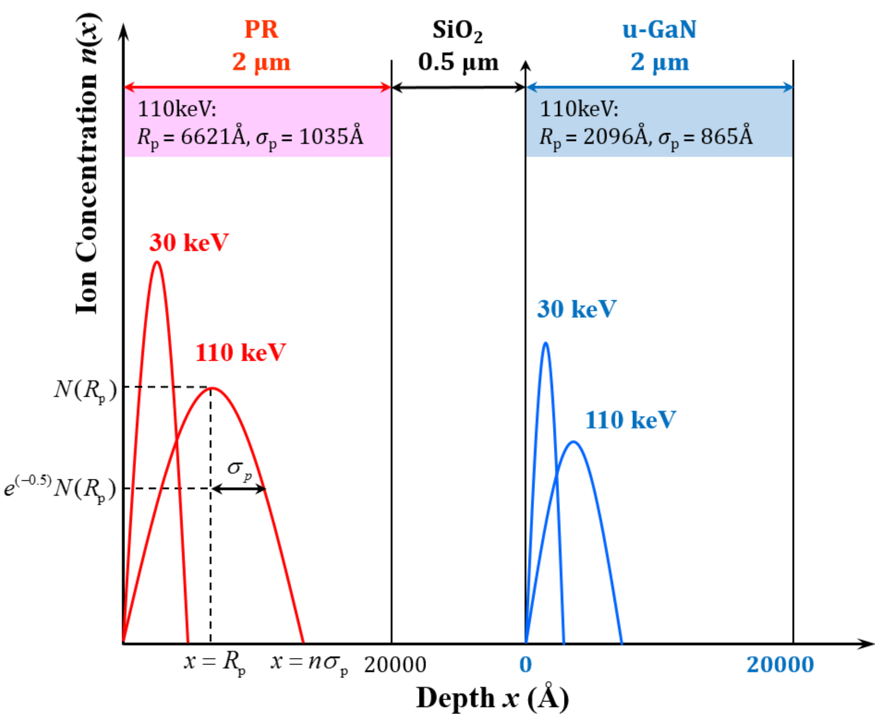


Figure 4. 1 Diagram of simple Gaussian distribution of boron ions in PR and u-GaN.

4. 2 GaN MOSFETs with boron ion implantation

4. 2. 1 Fabrication process flow of GaN MOSFETs with boron ion implantation

All the four kinds of devices, circular R-MOSFET, linear R-MOSFET, circular I-MOSFET, and linear I-MOSFET were fabricated on sample A to E. Figure 4.2. shows schematic cross-section of R-MOSFET and I-MOSFET on sample A, B, and C. The fabrication process was based upon the standard photolithography and lift-off technologies, as described in the following.

(1) The first step was the field isolation process. For comparison, sample A was with a mesa isolation structure only. Sample C was with boron ion implantation, while sample B was with both mesa isolation structure and boron ion implantation. The mesa was formed by ICP dry etching with two steps. The first step was done by $SiCl_4$ gas with a flow rate of 4 sccm, ICP power of 50 W, bias power of 100 W and at a working chamber pressure of 0.25 Pa. The second step was done by Cl_2 gas with a flow rate of 4 sccm, ICP power of 50 W, bias power of 50 W and at a working chamber pressure of 0.25 Pa. To keep the sample stage at the room temperature, helium gas was used for cooling during the etching process. After the mesa process, boron ions were implanted into sample B, C, D, and E. The mask for the implantation was double layers of 2 μm PR (HPR 1183L, Fuji film) and 500 nm SiO_2.

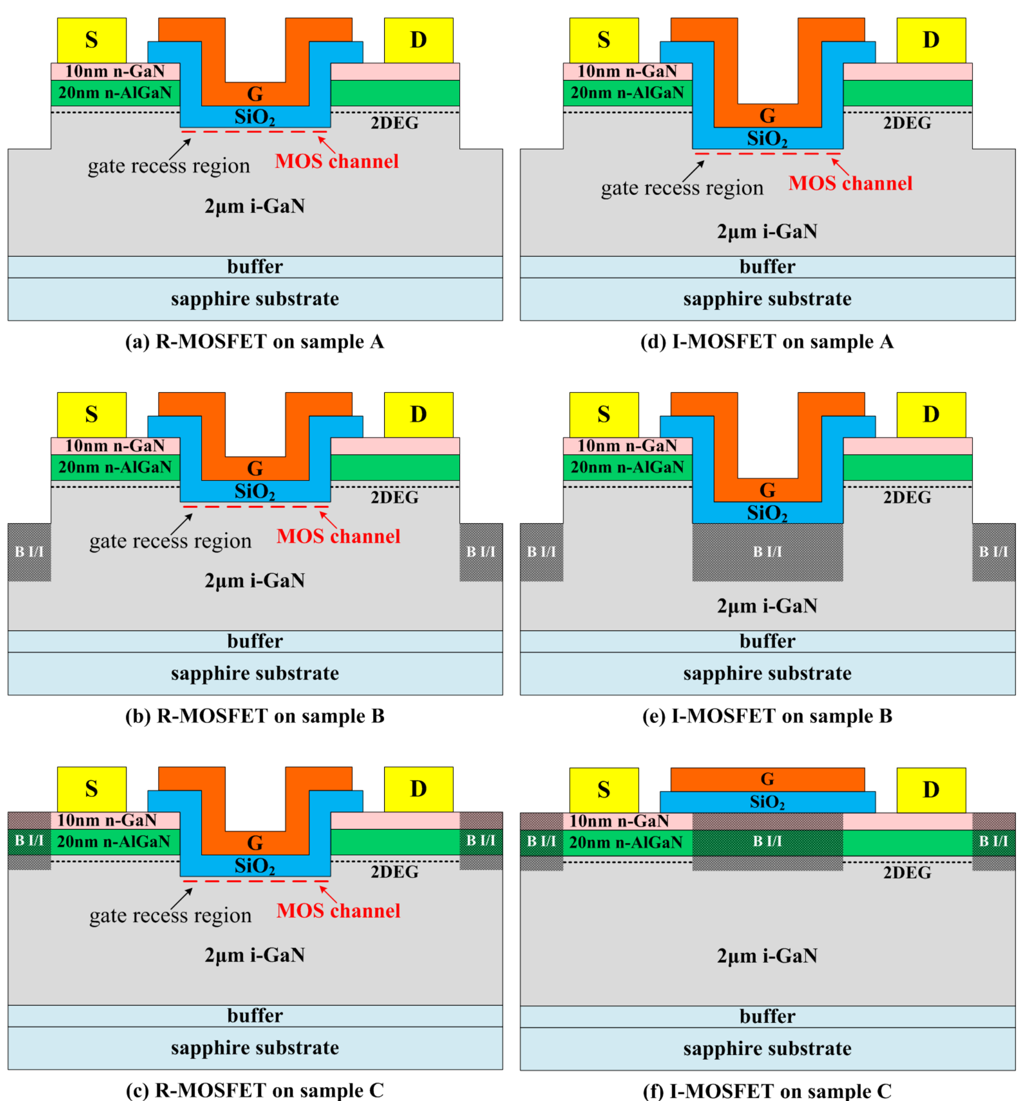


Figure 4. 2 Schematic cross-section of (a)-(f): the R-MOSFETs and the I-MOSFETs of sample A, B and C, respectively.

(2) The second step was the gate recess process to form the normal MOSFET channel. To remove the 2DEG layer, ICP system was used with $SiCl_4$ gas to a depth of 40 nm. The etching condition was ICP power of 100 W, bias power of 20 W, $SiCl_4$ gas flow rate of 3 sccm and working chamber pressure of 0.25 Pa. The recess etching mask was the SiO_2 film of about 500 nm thickness deposited by TEOS PECVD.

(3) The third step was the dielectric deposition. Silane-based PECVD was used to deposit SiO_2 (103.5 nm) as the gate oxide. As a post-annealing process, the samples were annealed at 1000 ℃ for 10 min in N_2 ambient.

(4) The final step was the electrode formation. The source and drain ohmic contacts were

formed using Ti/Al/Ti/Au (50/200/40/40 nm) and annealed at 850 ℃ for 1 min in N_2 ambient. The gate contact was formed using Ni/Au (70/30 nm).

4. 2. 2 Sheet resistance of implanted region

The sheet resistances of isolation region were measured by a TLM method at the temperature of 295 K, 313 K, 353 K, 393 K and 433 K, as shown in Figure 4.3. The sheet resistances of the implanted isolation regions are 1.41×10^{6} and 2.38×10^{6} $\Omega\cdot\text{sq}^{-1}$ at 295 K for sample B and C, respectively. The resistance of mesa isolation region without implantation (sample A) is 4.32×10^{5} $\Omega\cdot\text{sq}^{-1}$. The sheet resistances of sample D and E are 6.81×10^{5} and 8.66×10^{5} $\Omega\cdot\text{sq}^{-1}$ at 295 K, and lower than that of sample B and C, as listed in Table 4.1. The activation energy E_a is derived by

$$R_s = R_{s0}\exp\left(\frac{E_a}{kT}\right) \quad (4.2)$$

where R_s is the measured sheet resistance, R_{s0} is the sheet resistance extrapolated to the infinite temperature, E_a is activation energy, k is Boltzmann coefficient, and T is measurement temperature. The sheet resistance does not increase linearly with the implantation dosage. The derived activation energy E_a was around 0.19 eV for all the implanted samples. It may correspond to several defect levels, such as nitrogen vacancy. It should be noted the resistivity of the samples with ion implantation is not so high comparing with the sample with only mesa isolation. A possible reason was that the implanted ions were partly activated during the following high-temperature post-annealing processes of gate oxide.

Table 4. 1 Measured sheet resistance of isolation region of all the samples

Sample	Mesa	Boron implantation condition energy (keV) /dose (cm^{-2})	Sheet resistance at 295 K (Ω sq^{-1})	E_a (eV)
A	mesa	–	4.32×10^{5}	–
B	mesa	110 / 7×10^{14}, 30 / 5×10^{14}	1.41×10^{6}	0.187
C	no mesa	110 / 7×10^{14}, 30 / 5×10^{14}	2.38×10^{6}	0.186
D	no mesa	110 / 1.4×10^{15}, 30 / 1×10^{15}	6.81×10^{5}	0.198
E	no mesa	110 / 1.4×10^{14}, 30 / 1×10^{14}	8.66×10^{5}	0.175

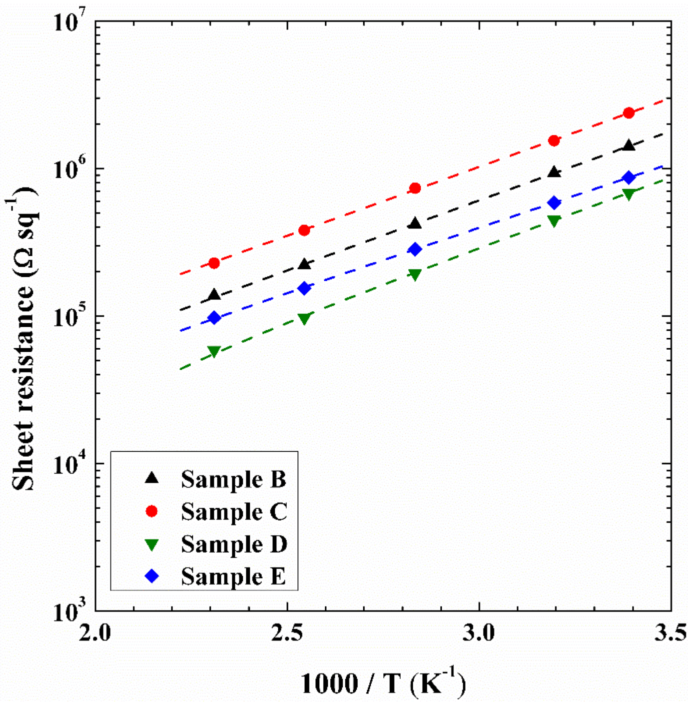


Figure 4. 3 Measured sheet resistance of isolation regions at various temperatures.

4. 2. 3 Evaluation of isolation effectiveness for GaN MOSFET

Figure 4.4 shows that the measured gate leakage currents of all the MOSFET samples were almost below 10^{-10} A with gate voltage V_g from 10 to -10 V and the drain and source voltage of 0 V. Proper device operations up to gate voltage of 10 V were confirmed for the circular and linear R-MOSFETs on each samples.

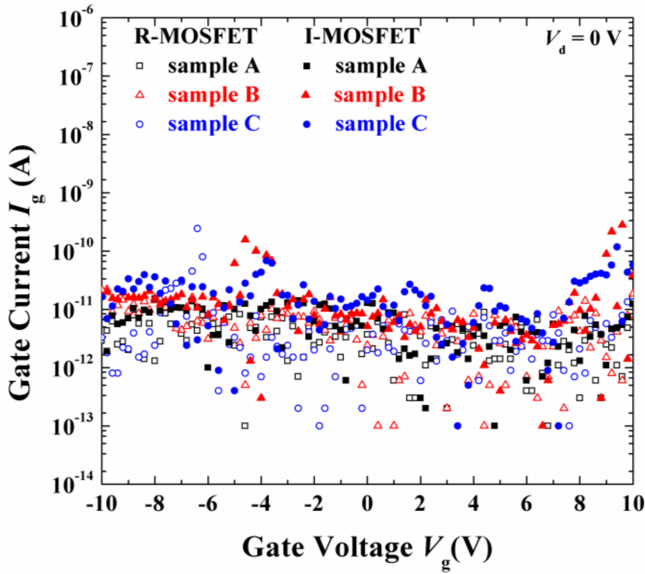


Figure 4. 4 The I_g-V_g characteristics of the circular MOSFETs on all the samples.

The current-voltage (I_d-V_d) characteristics of a circular R-MOSFET on sample A is plotted in Figure 4.5. Similar results were obtained for the same devices on sample B and C, indicating that the ion implantation process had no obvious effect on the normal devices. The I_d-V_d characteristics of a circular I-MOSFET with mesa isolation channel on the sample A is shown in figure 4.6. Similar to the R-MOSFET, device operation up to a gate voltage of 10 V was observed. This indicates that there still exists a MOS-channel in the mesa isolation. Figure 4.7 plots the I_d-V_d characteristics of the circular I-MOSFETs on sample B (with both mesa and boron ion implantation) and sample C (with boron ion implantation). Sweep I_d-V_d characteristics disappeared even with the gate voltage V_g from -10 to 10 V and drain voltage up to 20 V. The I_d of both devices increased linearly from 10^{-7} to 10^{-2} mA/mm when V_d was swept from 0 to 20 V and almost unchanged when V_g was varied from -10 to 10 V. This indicates that there are no MOS-channels appearing in the MOS-like structure fabricated on the ion-implanted isolation region.

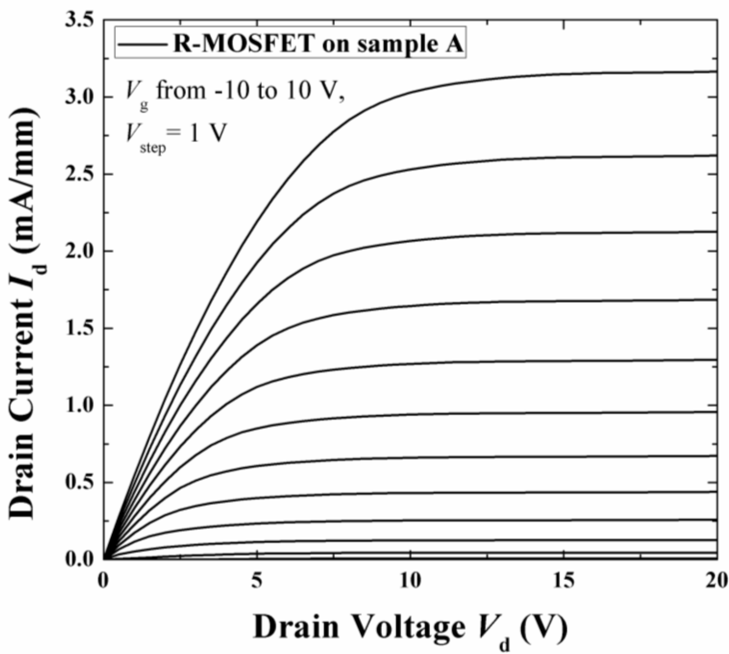


Figure 4. 5 The I_d-V_d characteristics of a circular R-MOSFETs on sample A with gate voltage V_g from -10 to 10 V and step of 1 V.

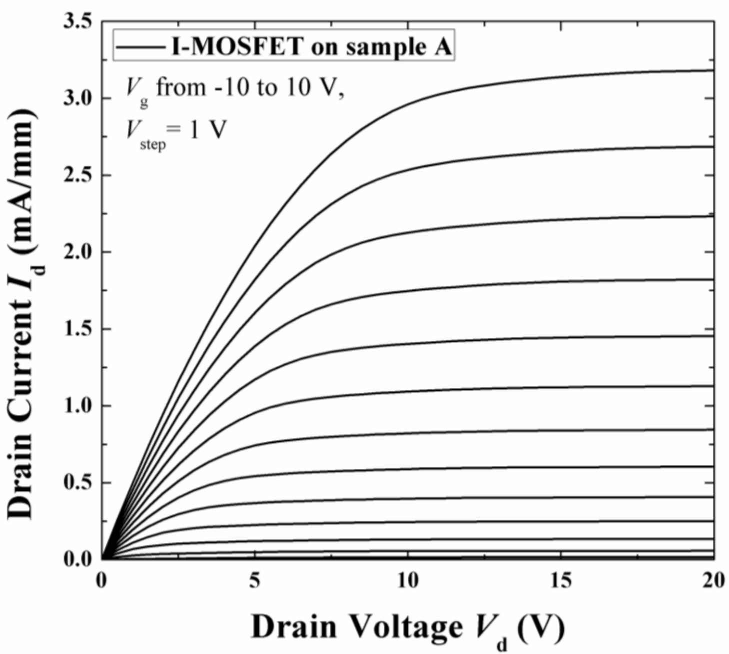


Figure 4. 6 The I_d-V_d characteristics of a circular I-MOSFETs on sample A with gate voltage V_g from -10 to 10 V and step of 1 V.

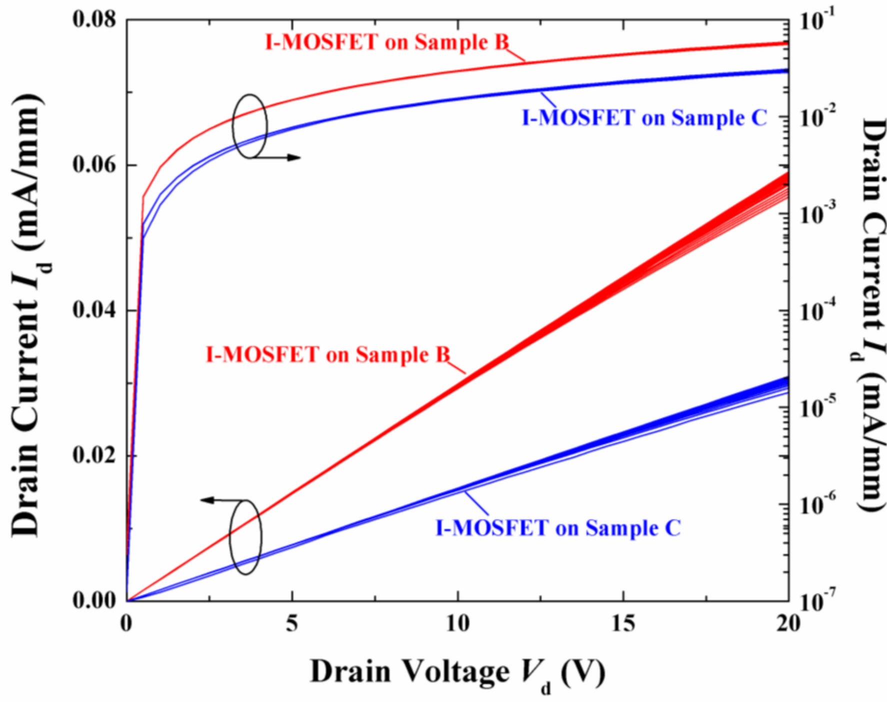


Figure 4. 7 The I_d-V_d characteristics of circular I-MOSFETs on sample B and C with linear and logarithm plots.

Figure 4.8 plots the transfer (I_d-V_g) characteristics of the circular I-MOSFETs on all the samples under drain voltage of 0.1 V. The device on sample A presented a good on-state characteristics with drain current up to 5.5×10^{-2} mA/mm. 5.5×10^{-2} mA/mm at gate voltage of 10 V and an extremely low off-state leakage current level in the range of 10^{-8} to 10^{-10} mA/mm. Contrarily, the devices on sample B and C presented a low drain current level of about 10^{-4} mA/mm when gate voltage was swept to 10 V. In other words, the MOS-channel didn't exist due to the damage caused by the ion implantation and the implanted region was turned to be a region with high resistivity. Boron ion implantation can be used as a device field isolation method on GaN MOSFET technology. However, although the drain current level at the on-state was reduced by two orders, the current level of 10^{-4} mA/mm for the I-MOSFETs on sample B and C was still higher than that of 10^{-8} to 10^{-10} mA/mm for the I-MOSFET on sample A.

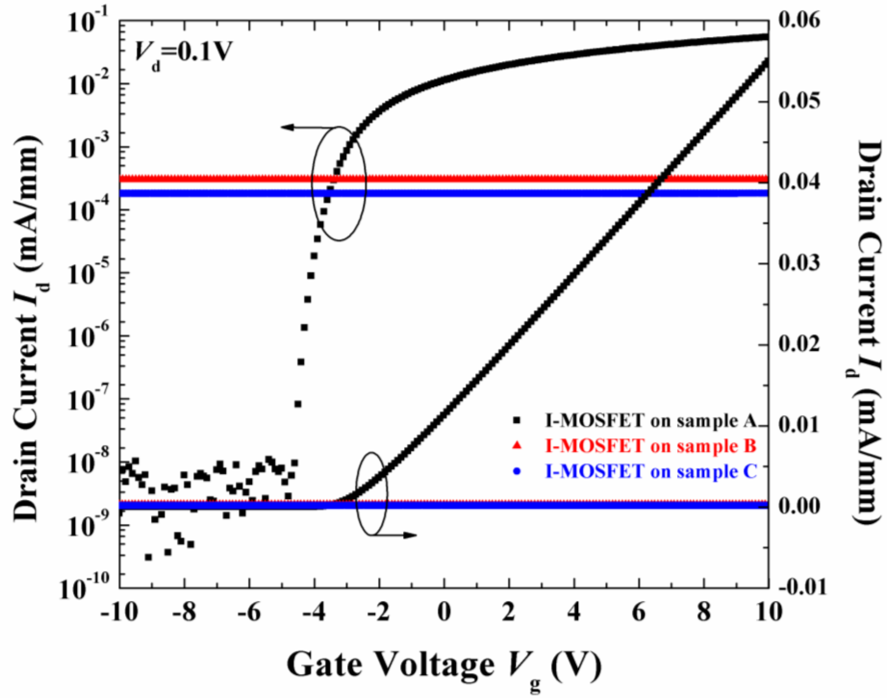


Figure 4. 8 The transfer (I_d-V_g) characteristics of the circular I-MOSFETs on all the samples at V_d of 0.1 V.

A comparison of the transfer (I_d-V_g) characteristics between a linear and a circular R-MOSFET on sample A, B, and C is shown in Figure 4.9 a, b, and c, respectively, under drain voltage of 0.1 V. For comparison, the transfer characteristics of a circular I-MOSFET on sample A was also plotted in Figure 4.9a. In figure 4.9a, drain current of the linear device is higher than that of the circular device due to the ineffective field isolation. Fortunately, the on-state drain

currents of the linear and circular R-MOSFETs in sample B and C are with the same level indicating that the field isolation process are effective (Figure 4.9 b and c). However, the off-state drain leakage current level of 10^{-3} mA/mm was still four orders of magnitude larger than that of circular MOSFET owing to the low resistivity in the field isolation regions. This result proves that boron ions implanted into the isolation region of a MOSFET would prevent the formation of a parasitic MOS-channel in the isolation region.

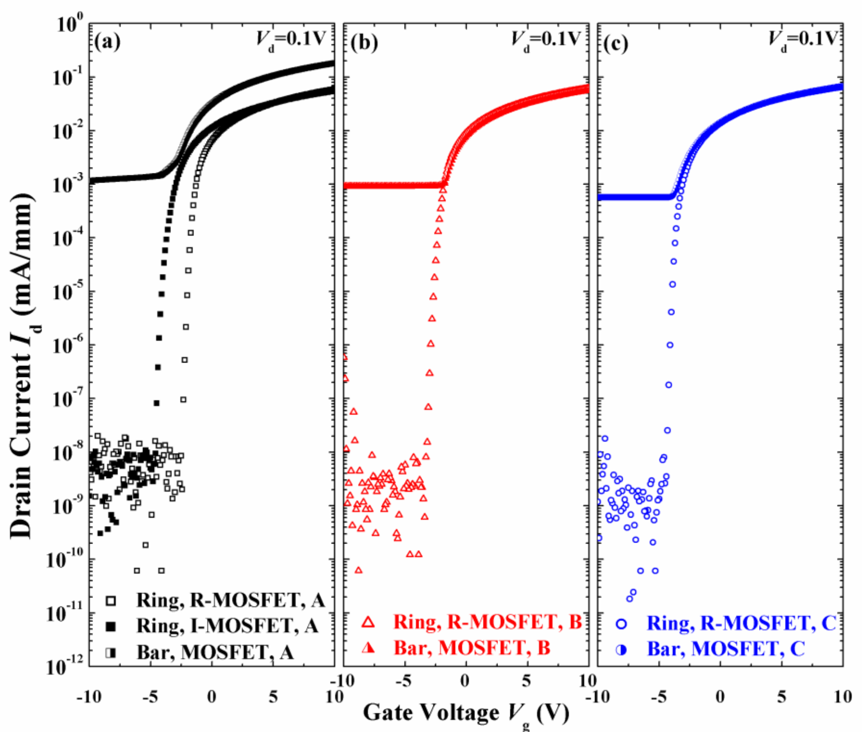


Figure 4. 9 The comparison of the transfer characteristics between a linear and a circular R-MOSFET on (a) sample A, (b) sample B, and (c) sample C, at $V_d = 0.1$ V.

The field-effect electron mobility was determined by a method of gate capacitance-transconductance. Figure 4.10 shows the field-effect mobility of a linear and a circular R-MOSFET on sample A, B, and C comparing with that of a circular I-MOSFET on sample A. The mobility of R-MOSFET on sample A, B and C was 147.7, 148.1, and 150.7 $cm^2V^{-1}s^{-1}$, respectively. The mobility of I-MOSFET on sample A (without B I/I) was 119.4 $cm^2V^{-1}s^{-1}$ and the reduction of mobility was attributed to the greater plasma-induced damage on etching surface. No degradation of field-effect electron mobility was observed demonstrating that this process of boron ion implantation would not decrease the field-effect mobility of GaN MOSFETs. A little variation of threshold voltages was also observed among all the devices.

The reason is considered to be due to the charges existing in the gate oxide [102]and the donor-like nitrogen vacancy introduced from the dry etching process [101]. The more negative threshold voltage of I-MOSFET (ring) than R-MOSFET (ring) in Figure 4.10a may be also related with more nitrogen vacancy caused by higher bias power. It should be mentioned that the estimated mobility of the linear device coincides with that of the circular devices for sample B and C, clearly indicating that the overestimation of field-effect mobility of the linear MOSFETs was eliminated due to the fact that boron ion implantation prevented the formation of parasitic MOS-channel in the isolation region.

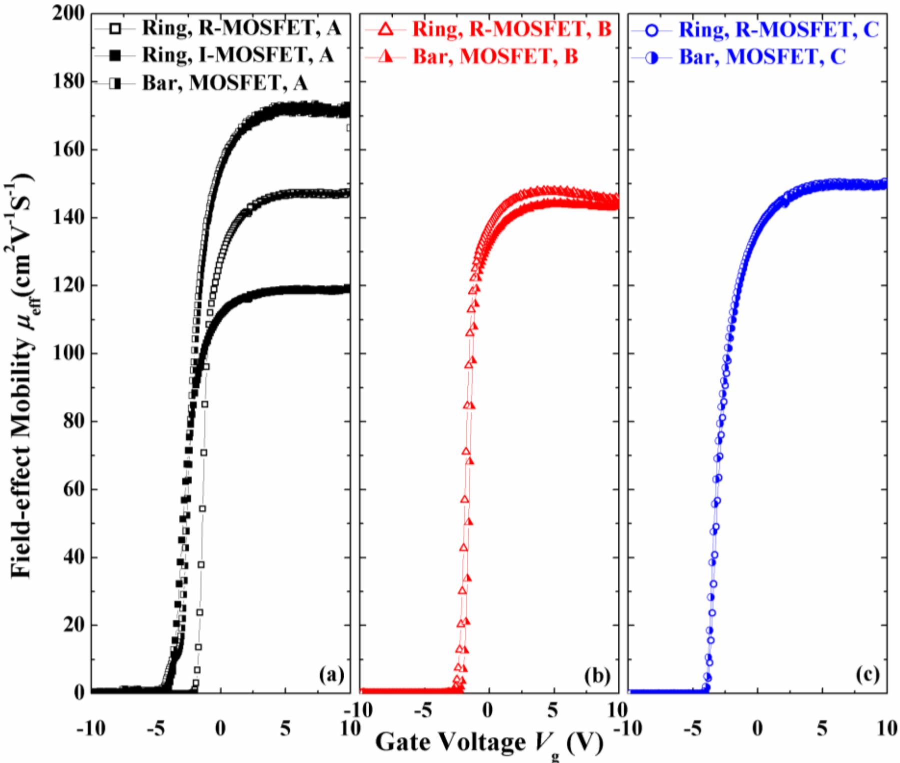


Figure 4. 10 The field-effect mobility of a linear and a circular R-MOSFET on sample A (a), B (b), and C (c) comparing with that of circular I-MOSFET on sample A (a).

4. 3 GaN MOSFETs with improved process of annealing and boron ion implantation

Although boron ion implantation eliminated the parasitic MOSFET in the isolation region of the linear GaN MOSFETs, the off-state drain current was only 10^{-4} mA/mm and the sheet resistance of implanted region was 10^6 Ω/□ at room temperature. The low resistivity may be attributed to the recovery of the implantation damage by the subsequent annealing process of ohmic annealing at 850 °C and the gate oxide thermal treatment at 1000 °C. To achieve an extremely low off-state drain current and successful field isolation for the linear devices, GaN MOSFETs using boron ion implantation and mesa structure as the device isolation methods were fabricated and the effectiveness of the two methods were evaluated. All the annealing process steps were completed before the boron field implantation during the fabrication.

4. 3. 1 Fabrication process flow of improved GaN MOSFETs

Epitaxial layers were grown on a c-plane sapphire substrate, which consisted of a buffer layer, a 2 μm-thick undoped GaN (u-GaN) layer, and a 30 nm-thick Si-doped n-GaN layer with a concentration of 1.0×10^{19} cm^{-3} from the bottom to the top. The gate length and width of the linear MOSFET were 100 μm and 102 μm, respectively. The gate length and effective channel width of the circular MOSFET with 89 μm inner radius and 193 μm outer radius were 94 μm and 819 μm, respectively.

Four samples were used in the experiments as listed in Table 4.2. The R-MOSFET and I-MOSFET structures on samples ME, IM1, and IM2 are shown in Figure 4.11. The structure of sample IM3 is the same as that of sample IM2.

Table 4. 2 The samples with different structures and implant conditions.

Sample	Structure	Boron ion implantation condition
ME	mesa	no implantation
IM1	no mesa	110 keV /5×10^{14} cm^{-2}, 30 keV /7×10^{14} cm^{-2}
IM2	mesa	110 keV /1.4×10^{14} cm^{-2}, 30 keV /1×10^{15} cm^{-2}
IM3	mesa	110 keV /5×10^{14} cm^{-2}, 30 keV /7×10^{14} cm^{-2}

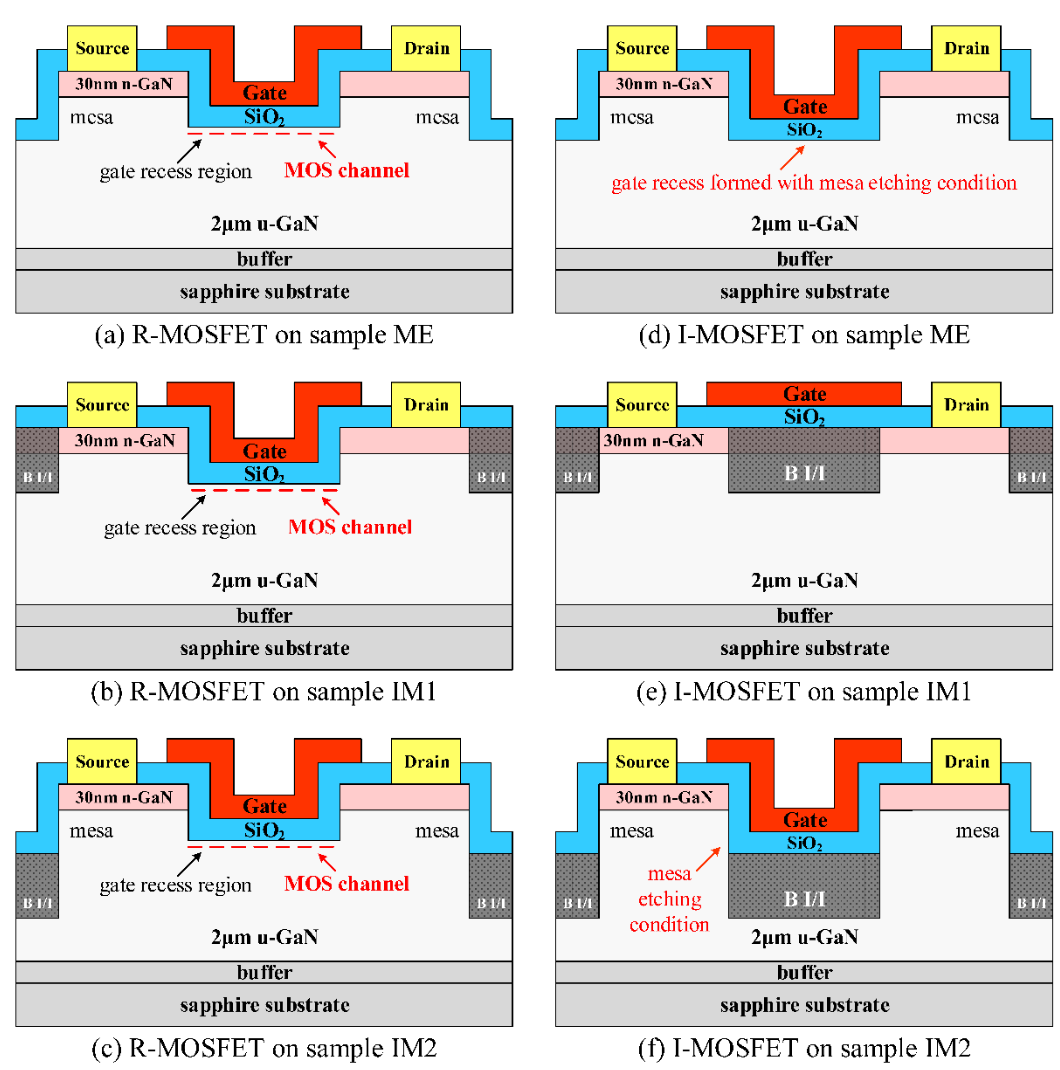


Figure 4. 11 Structures of (a)–(c) ordinary recessed-gate R-MOSFETs and (d)–(f) I-MOSFETs fabricated on the different isolation regions.

The device fabrication began with the 90 nm-deep mesa structure through the inductively coupled plasma (ICP) dry etching system with SiCl4 etching gas. A 2 μm-thick positive photoresist (HPR-1183L, Fujifilm Corp., Minato, Tokyo, Japan) was utilized as the mesa etching mask. For the R-MOSFETs of all the samples, the 54 nm-deep gate recess was formed by the ICP system using the same dry etching condition. The recess etching mask was a 500 nm-thick SiO_2 film deposited by plasma enhanced chemical vapor deposition (PECVD) system with a tetraethylorthosilicate (TEOS)-based source. After the completion of all the dry etching processes, the samples were immersed in a HNO_3:HF buffered solution (BHF; 1:1, volume ratio) to remove the possible Si contamination on the etched surface. The gate oxide was a 100 nm-

thick SiO_2 layer deposited by PECVD (PD-220LC, SAMCO, Inc., Fushimi, Kyoto, Japan) with a silane-based source. A gate oxide post-annealing process was performed at 1000 ℃ for 10 min in nitrogen ambient. After ohmic electrodes patterning, a metal stack of Ti/Al/Ti/Au (50/200/40/40 nm) was deposited by the lift-off process and annealed at 850 ℃ for 1 min in nitrogen ambient.

A 2 μm-thick photoresist was utilized as an implantation mask to protect the active region. Subsequently, sample IM1–3 were subjected to double-energy implantation by boron ions. The implantation profile was estimated through a Gaussian distribution function. According to TRIM software, the 100 nm-thick SiO_2 layer on top of the isolation region can stop 15.2% of the boron ions, and the implantation depth in the GaN layer was estimated to be approximately 400 nm. Finally, a Ni/Au (70/30 nm) bi-layer was deposited as gate electrode.

4. 3. 2 Evaluation of isolation effectiveness for improved GaN MOSFET

Figure 4. 12 plots the *I–V* characteristics (a) and the transfer characteristics (b) of the circular I-MOSFETs on all the samples. The circular I-MOSFET with mesa isolation (sample ME) presented good on-state characteristics with a gate voltage of up to 10 V, indicating that a parasitic MOSFET existed on the mesa-isolated region. By contrast, the circular I-MOSFETs with B I/I isolation (sample IM1–3) presented an extremely low drain current of 7×10^{-8} mA/mm, which was nearly constant when the gate voltage was swept from −10 V to 10 V. This result demonstrates that the B I/I isolation eliminated the parasitic MOSFET in the isolation region by the creation of high resistance from significant implantation damage.

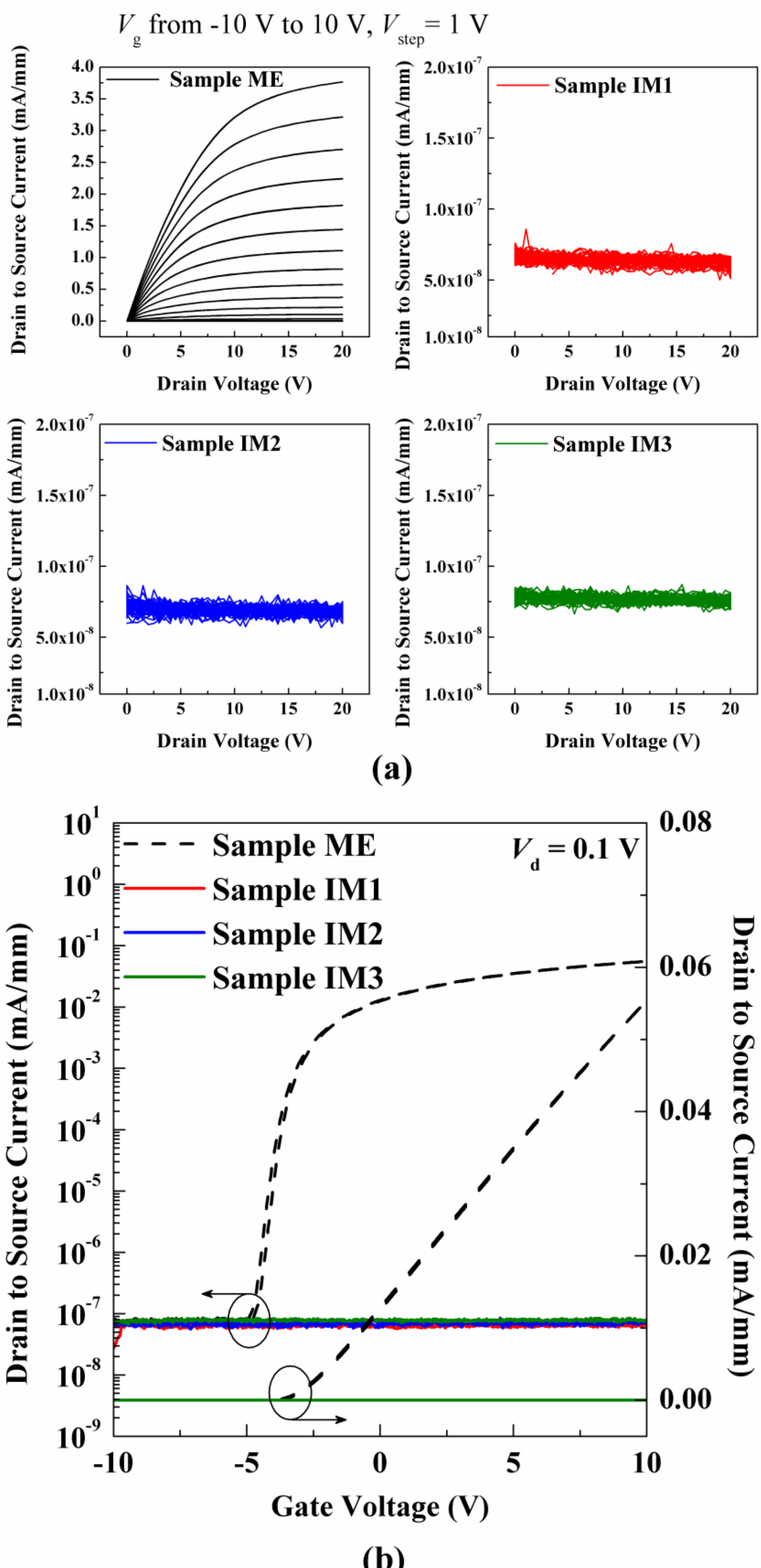


Figure 4. 12 (a) *I*–*V* and (b) transfer characteristics of the circular I-MOSFETs on all the samples.

Figure 4.13 plots the transfer characteristics of circular and linear R-MOSFETs on sample A and B, under drain voltage of 0.1 V. The linear R-MOSFET on sample B (B I/I isolation) presented a low off-state drain current of about 6×10^{-7} mA/mm, which was only one order of magnitude higher than the 7×10^{-8} mA/mm of the circular R-MOSFET. The linear R-MOSFET on sample A presented a high off-state drain current of about 3×10^{-5} mA/mm. By adjusting the process sequence of boron field implantation, the high-temperature annealing process was avoided. The implanted region demonstrated high resistivity and effective field isolation was successfully achieved. In addition, a little variation of threshold voltages was observed between the circular MOSFETs with mesa isolation and B I/I isolation. The possible reason is the variation on the charges in the gate oxide layers [102].

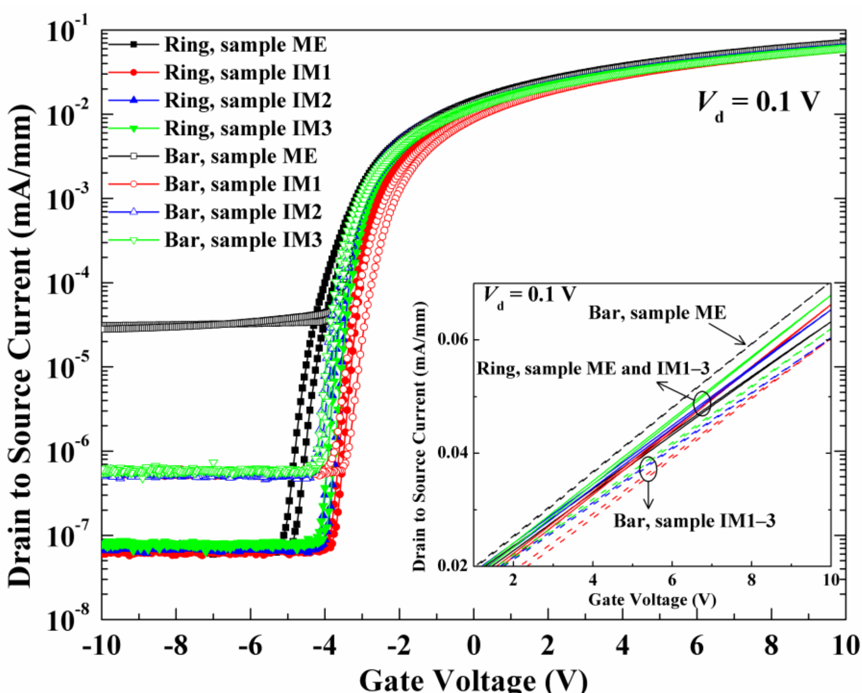


Figure 4. 13 Transfer characteristics of circular and linear R-MOSFETs on all the samples.

4. 3. 3 Characterization of GaN MOSFETs with boron ion implantation avoiding annealing process

The field-effect electron mobility μ_{FE} was obtained by the gate capacitance-transconductance method. Figure 4.14 shows the μ_{FE} values of the circular and linear R-MOSFETs on all the samples and the circular I-MOSFET on sample ME. As listed in Table 4. 3, the maximum μ_{FE} values of the linear and circular R-MOSFETs on samples IM1−3 are very close to each other, demonstrating that boron field implantation could eliminate the parasitic

MOSFET in the isolation region. The maximum μ_{FE} of the linear R-MOSFET on sample ME was 162.1 $cm^2V^{-1}s^{-1}$, which was much higher than the 134.8 $cm^2V^{-1}s^{-1}$ of the circular R-MOSFET on sample ME. The mobility was overestimated because the parasitic MOSFET in the mesa-isolated region widened the effective channel width [140]. The maximum μ_{FE} of a circular I-MOSFET on sample ME was 121.0 $cm^2V^{-1}s^{-1}$, and the decrease was attributed to a bad recess profile produced by the use of photoresist as the etching mask [98]. No degradation of μ_{FE} was observed on the circular R-MOSFETs on all the samples, demonstrating that the boron field implantation would have not deteriorated the MOSFETs.

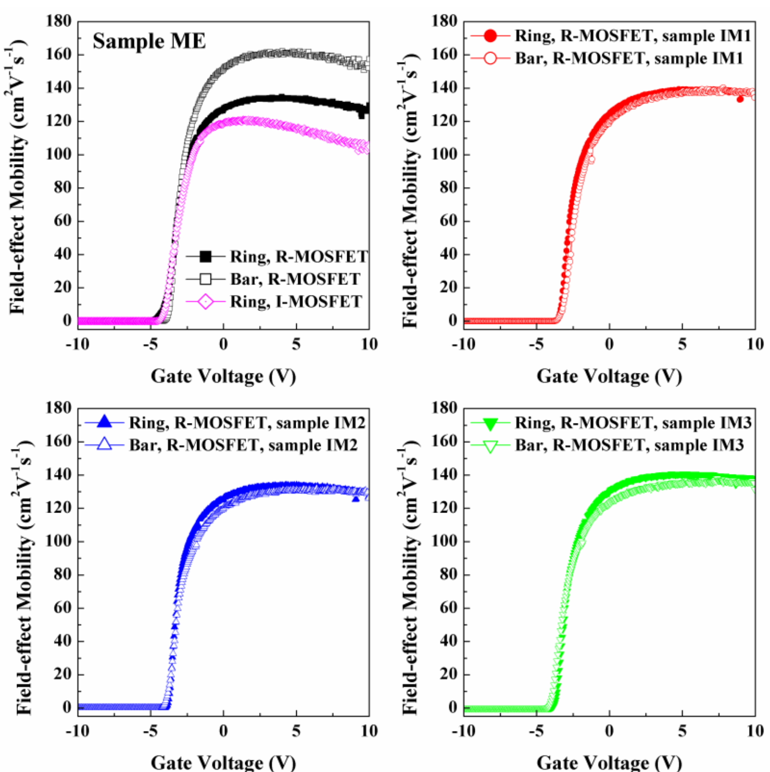


Figure 4. 14 Field-effect mobility of R-MOSFETs on all the samples and a circular I-MOSFET on sample ME.

The interface states density D_{it} at the SiO_2/u-GaN face can be calculated from the interface-related capacitance C_{it}. The oxide capacitance C_{OX} is in series, connected with a parallel connection of the semiconductor bulk capacitance C_B and C_{it} into the equivalent circuit of MOS structure. Based on the definition of subthreshold swing S

$$S = \left[\frac{\partial(\log_{10} I_{ds})}{\partial V_g} \right]^{-1} = \left(\frac{\ln 10 kT}{q} \right) \left(\frac{C_{OX} + C_B + C_{it}}{C_{OX}} \right),$$

considering that C_B is zero due to a remarkably low carrier concentration of semi-insulating u-

GaN layer, and thus C_{it} can be extracted from S. In this expression, k is the Boltzmann constant and q is the elementary charge. Table 4.3 2 lists the D_{it} of the R-MOSFETs on all the samples and the circular I-MOSFET on sample ME. The D_{it} of the linear R-MOSFET on sample IM1 was larger than that of the circular R-MOSFET because the two ends of the gate recess were connected with the implanted-region and the implantation damages were introduced into the channel and increased the D_{it}. The difference between the D_{it} values of the linear and circular R-MOSFETs on samples IM2 and IM3 was small because the implanted region was deeper than the gate recess and the implantation damages were not introduced. The isolation structure of both mesa and implantation did not introduce the implantation damages into the channel and did not influence the interface state density, whereas the isolation structure of only implantation introduced the implantation damages and resulted in a high interface state density. Therefore, the isolation structure of both mesa and implantation is advantageous to reduce the interface state density of devices. The gate recess protection from the implantation damage should be considered in future works.

Table 4. 3 Maximum field-effect mobility and interface state density of the circular MOSFETs on all the samples.

Sample	Structure	Field-effect mobility μ_{FE} ($cm^2V^{-1}s^{-1}$)		Interface state density D_{it} (10^{11} $cm^{-2}eV^{-1}$)	
		Ring	Bar	Ring	Bar
ME	R-MOSFET	134.8	162.1	7.0	–
IM1	R-MOSFET	139.3	140.3	5.3	9.0
IM2	R-MOSFET	133.9	132.2	4.2	6.5
IM3	R-MOSFET	140.9	138.2	5.2	6.0
ME	I-MOSFET	121.0	–	7.4	–

The breakdown characteristics of the mesa-isolated region and implanted regions were determined using the structure presented in Figure 4.15, with 5 μm spacing at room temperature. The breakdown voltages of 150.0, 871.0, 762.0, and 901.5 V were confirmed for the mesa-isolated region on sample ME and the implanted region on samples IM1−3. The breakdown voltage was significantly improved by boron field implantation.

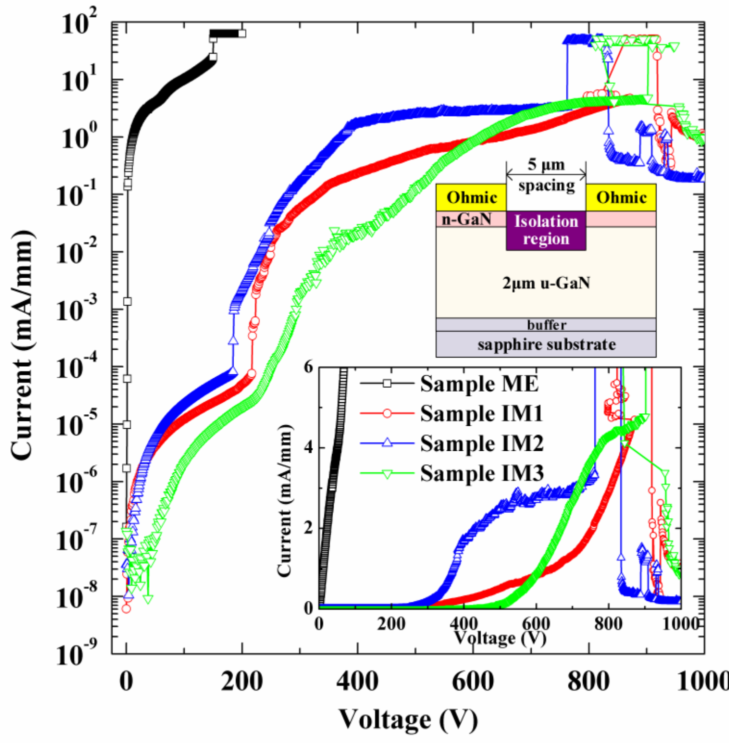


Figure 4. 15 Breakdown characteristics of the mesa-isolated region and the implanted region on all the samples.

4. 4 Summary

In this chapter, GaN MOSFETs using boron ion implantation as field isolation process were fabricated and the effectiveness of boron field implantation and influence of implantation damage on device performance were evaluated. The process of boron field implantation was developed and improved for GaN MOSFETs, the elimination of parasitic MOSFETs was confirmed by the *I*–*V* characteristics of circular MOSFETs fabricated in the isolation regions, and the isolation effectiveness of process was evaluated through the comparison of *I*–*V* characteristics between circular and linear device. The influence of implantation damage on device performance for different isolation structures were evaluated by the calculation of the field-effect electron mobility and D_{it} according to *I*–*V* and *C*–*V* tests. The process of boron field implantation was altered and subsequently conducted after high-temperature ohmic annealing process and gate oxide thermal treatment, and the implanted regions with high resistivity were achieved. The *I*–*V* characteristics indicated that the circular MOSFET fabricated in the isolation region showed an extremely low drain current of 7×10^{-8} mA/mm, demonstrating that the parasitic MOSFET in the isolation region was eliminated by boron field implantation. The comparison of *I*–*V* characteristics between circular and linear device showed that the off-state drain current of the linear MOSFET was reduced from 3×10^{-5} mA/mm of mesa isolation to 6×10^{-7} mA/mm of boron field implantation, which was only one order of magnitude higher

than the 7×10^{-8} mA/mm of the circular device. Field isolation for GaN MOSFETs succeeded using boron field implantation. The breakdown voltage of the isolation region with a 5 μm spacing was significantly improved up to 901.5 V. The calculation of the field-effect electron mobility showed that implanting did not deteriorate the mobility. The D_{it} results indicated that the isolation structure of both mesa and implantation did not influence the interface state density. This work extended field isolation technique in Si MOSFET to GaN MOSFET, provided a field implantation process that could eliminate the parasitic MOSFETs and achieve an extremely low off-state current, presented an isolation structure that could obtain field isolation and avoid the high D_{it}, and brought benefit for improving the device performance in GaN MOSFETs.

5 Conclusion and future works

5. 1 Conclusion

This thesis investigates the device isolation technologies for GaN-based FETs.

In AlGaN/GaN HFET, an effective process of O_2 plasma treatment for device isolation was investigated. Isolation current was strongly dependent on treatment temperature and the depth of etching damage. Under the conditions of O_2 plasma treatment at 300 ℃ for 15 min at 250 W, the isolation current was reduced by four orders of magnitude to 10^{-11} A and photovoltaic responses were suppressed, and the breakdown voltage of the mesa-isolated region with 5 µm spacing was improved from 171.5 V to 467.2 V. The PL results showed a decrease in the density of YL band-related defects and the occurrence of BL band-related defects. The XPS results indicated that O_2 plasma treatment can form high amounts of Ga_2O_3 than O_2 gas treatment, and the defect of O_N was also probably formed. An AlGaN/GaN HFET with an on/off drain current ratio of 1.73×10^7 was achieved through O_2 plasma treatment. O_2 plasma treatment is thus regarded as an effective method for improving device isolation. The trade-off between defects creation and reduction of leakage current is required for piratical fabrication.

GaN MOSFETs using boron ion implantation as field isolation process were fabricated and the effectiveness of boron field implantation was evaluated. The circular MOSFET fabricated on the ion-implanted region showed a drain current of 2×10^{-4} mA/mm and 6×10^{-8} mA/mm before and after adjusting the process sequence of annealing and boron field implantation, demonstrating that boron field implantation could prevent the formation of parasitic MOSFET in the isolation region. By adjusting the process sequence, the high-temperature annealing process was avoided and the implanted region presented high resistivity. The *I–V* characteristics indicated that the off-state drain current of the linear MOSFET with boron field implantation isolation was reduced to 6×10^{-7} mA/mm, which was only one order of magnitude higher than the 7×10^{-8} mA/mm of the circular MOSFET. The field isolation for GaN MOSFETs was successfully achieved by boron field implantation. The implantation damage did not deteriorate the field-effect mobility. The isolation structure of both mesa and implantation did not influence the interface state density, whereas the isolation structure of only implantation increased the interface state density because of the introduction of the implantation damages into the channel. The isolation structure of only implantation is recommended to simplify the fabrication processes; the isolation structure of mesa and implantation is recommended to minimize the interface state density.

5. 2 Future works

1. The protection of active region in AlGaN/GaN HFET is needed to avoid current collapse effect for O_2 plasma treatment.
2. The defects like O_N was induced by O_2 plasma treatment, and the elimination of the defects should be considering.
3. The thermally stability of GaN MOSFET using boron ion implantation should be evaluated.
4. The long-term influence of traps induced by boron ion implantation on interface state density should be investigated.

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Journal Paper Publication:

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