Abstract

AlGaN/GaN HFETs have become the subject of competing research due to the superior material properties of GaN. An urgent need is to reduce the leakage current in the field of high temperature and high frequency. In our previous works, AlGaN/GaN HFETs with the Schottky gates have the relatively higher reverse leakage current. For AlGaN/GaN HFETs, there is an urgent need to find p-type semiconductor gate materials and insulator gate materials with high *k* and high crystallization temperatures for their normally-off and high temperature applications. In this thesis, we discussed the synthesis and application of oxide for GaN electron devices.

NiO is a natural p-type semiconductor with stable chemical properties. We fabricated NiO films with different O_2/Ar ratios of 15%, 25%, 50%, and 65% and substrate temperature from 30 to 300 °C using magnetron reactive sputtering. The NiO films with the face-centered cubic crystalline structure are analyzed by AFM, XRD, XPS, UV-Vis transmittance spectra and circular TLM. The crystal orientation depends on the oxygen percentage. The quality of the crystallization decreases with the increasing of oxygen percentage. When the substrate temperature increased from 30 to 200 °C, the crystalline quality and stoichiometric of the NiO films were improved, resulting in higher bandgap value and resistivity. While further increasing the substrate temperature to 300 °C, the decomposition of NiO will cause the appearance of Ni metal in the film. An optimal oxygen ratio of 25% under substrate temperature of 30 ºC for growing NiO is obtained.

The electrical transport properties of the NiO/GaN heterojunction device in the temperature range from 25 to 175 ºC is investigated. Comparing with the Ni/GaN Schottky diode, the turn-on voltage of the NiO/GaN heterojunction diode is relatively higher. The NiO/GaN diode exhibited a temperature-dependent turn-on voltage with smaller reverse leakage current. The as-grown NiO exhibited cubic crystalline structure with a bandgap of 3.2 eV. It is founded that there are three types of current transport mechanisms which are strongly relates to the applied bias voltages and temperatures. On the other hand, the device exhibited considerably a stable behavior over the temperature range from 25 to 175 °C and will be favorable for widely applying in high-temperature and high-power environments.

From above the material and electrical results, we used the NiO film under 30 °C with

lowest resistivity as the gate electrode for AlGaN/GaN HFETs application. Compared with the Ni/Au-gated device, the threshold voltage of the NiO-gated device has a positive shift of approximately 1V because of the p-type conductivity as well as the conduction band offsets between NiO and GaN. The band offset at the heterojunction interface can be measured by XPS employing a well-known Kraut's method. We calculated the corresponding valence (1.25 eV) and conduction band offset (1.42 eV) using a band gap of 3.57 eV for the NiO film deposited at 30 ^{o}C. After recessing, the threshold voltage for the Ni- and NiO-gated HFETs has a positive shift. We obtained normally-off NiO-gated GaN HFETs with a threshold voltage of closing to 0 V using the recessed-gate structure. As one of the most promising insulator candidates, HfO_2 and HfO_xN_y with wide bandgap and high-k are extensive investigated. We fabricated HfO_xN_y films with different oxygen flow rates using magnetron reactive sputtering. The films are analyzed by AFM, XPS, UV-Vis diffuse reflection spectra. The growth rate decreases with the increasing of oxygen flow rate. The quantity of the hole increases with increasing oxygen flow rate. The composition of films changed from HfN to HfO_2 domination with the increasing oxygen flow rate and HfO_xN_y formed at a smaller oxygen flow rate. MOS diode fabricated with HfO_xN_y film by 1 sccm oxygen shows the smallest reverse leakage current. It indicates that the HfO_xN_y film is made due to the higher nitrogen in the reactive gases. We fabricated AlGaN/GaN HFETs using TiN/HfO_xN_y stack gate layer with 1 sccm oxygen. The threshold voltage for the Schottky contact, HfO_2 MOS, and HfO_xN_y MOS HFETs are approximately –3.0, –5.0, and –7.0 V, respectively. Compared with HfO_2 MOSHFETs, the introduction of the HfO_xN_y dielectric results in a negative shifting threshold voltage and a lower leakage current. After post deposition annealing at different temperatures, the devices using HfO_xN_y dielectric show better thermal stability at 900 ^{o}C while obvious degradation are observed for the HfO_2 MOSHFETs at 600 ^{o}C. A possible mechanism is that the existence of Hf-N bond in bulk dielectric and N at the dielectric/GaN interface can help to improve the thermal stability. The thermal stability of TiN/HfO_xN_y/AlGaN/GaN HFETs shows that the HfO_xN_y dielectric is a promising candidate for the self-aligned gate process.

Keywords: AlGaN/GaN, HFETs, NiO, HfO_xN_y

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Chapter 1 ：Introduction

§1.1. Background

With the development of technology and society, the efficient and practical use of electric energy is a hot issue that has caught people’s attention. Power electronics technology is a discipline of the realization for power conversion and control. It is a bridge and link of weak electricity controlling strong electricity. It is now widely used in various fields such as industrial and agricultural production, national defense, transportation, energy and people's livelihood. Of course, the emergence and development of power electronics depend on the continuous development of power electronics devices. In 1948, the invention of the first generation of semiconductor transistors gradually led to an electronic industrial revolution. The first semiconductor transistor was used in the field of low-power, such as computers. With the advent of the world's first transistor, the range of semiconductor transistors have been greatly expanded. Power conversion and control was developed from the rotating converter unit, the static ion converter into the inverter composed of the power semiconductor devices, which also marks the birth of power electronics technology. Transistors have played an important role in the establishment of power electronics disciplines. But the transistor is a semi-controlled device, which cannot control its pinch-off. So far, due to their relatively low cost, transistors and their derivatives have been widely used in various converters.

Due to the first generation semiconductor devices can only control its conduction through its gate and can not control its pinch-off, it was necessary to add inductors, capacitors or other auxiliary switching devices to turn off it in the DC power. But these will let increase the size of the current transformer and reduce the efficiency. The power electronic devices of the second generation represented by Giant Transistor (GTR) [1], Gate Turn-Off Thyristor (GTO) [2,3], MOSFET [4]. They can be controlled to turn on and off. The power electronics MOSFET of the second generation is a unipolar device, which is no conductivity modulation effect and increases its switching speed. And MOSFET became the most important power semiconductor devices in the high-frequency field. However, it is precisely because of no conductivity modulation effect, as the device

withstand voltage increases, on-resistance of MOSFET also increases, which will lead to have very serious conduction losses.

By the late 1980s, composite devices represented by insulated gate bipolar transistors (IGBTs) appeared [5]. IGBT is a combination of MOSFET and GTR, which is a MOSFET-driven bipolar transistor. It has advantage of both the MOSFET's high input impedance and GTR's low on-voltage drop. However, with the development of science and technology, IGBTs still can not meet the demanding requirements in various fields such as aerospace, communications and nuclear energy. People urgently need a power electronic device that can still work normally under the extreme conditions of high temperature and high radiation. Therefore, we must find more advantageous materials to develop high-power electronic devices for meeting the high temperature, high frequency, high radiation environment. Therefore, new materials such as GaAs, GaAlAs, SiC, diamond and GaN have been rapidly developed and applied [6-10].

Because of their excellent properties and thermal stability, the group III nitrides are determined to play a pivotal role in the future development of optoelectronic devices [11, 12]. Among the many group III nitrides, the gallium nitride (GaN) is seen as the preferred material of the blue and other short-wavelength optical devices (especially blue laser diodes and blue light-emitting diodes) [13-16]. And that it can meet the requirements of the semiconductor devices with high power, high temperature, high frequency and high speed, which are not available with many silicon (Si)-based semiconductor materials. Although the related properties of GaN films have been studied in the last few decades, the GaN films produced often have relatively high defect density due to the backwardness of the thin film preparation technology at that time. So that, the relevant research of the GaN material was not satisfactory. Recently, with the increase of the GaN film growth technology, high quality GaN thin film can be grown by Molecular Beam Epitaxy (MBE), Metal-organic Chemical Vapor Deposition (MOCVD) and Solid Phase Epitaxy (SPE). In some related reports, most of the GaN films were grown on the wide variety of substrates such as Si [17-22], gallium arsenide (GaAs) [23-26] and silicon carbide (SiC) [27,28]. However, it is difficult to grow high quality GaN films on these substrates because of the large lattice mismatch and the imbalance of the coefficient with thermal expansion between these substrates and the GaN films. In order to further improving the quality of GaN films, the buffer layers between GaN films and commonly used monocrystalline

substrates were grown to overcome the adverse effects of the lattice mismatch and thermal expansion coefficients between GaN layer and substrates. The buffer layers used in the experiments generally include aluminum nitride (AlN), SiC, GaAs, oxidized aluminum arsenide (AlAs) [29-32], and so on. High quality GaN films were successfully grown on the (0001) sapphire (Al_2O_3) substrates by low-pressure metal organic chemical vapor deposition (LP-MOCVD). The LP-MOCVD technology is critical to improving the quality of the GaN films due to the remission of the adverse effect with lattice mismatch (13%~16%) between GaN films and sapphire substrates [33]. Figure 1-1 shows the energy gap and lattice constants of the part of materials.

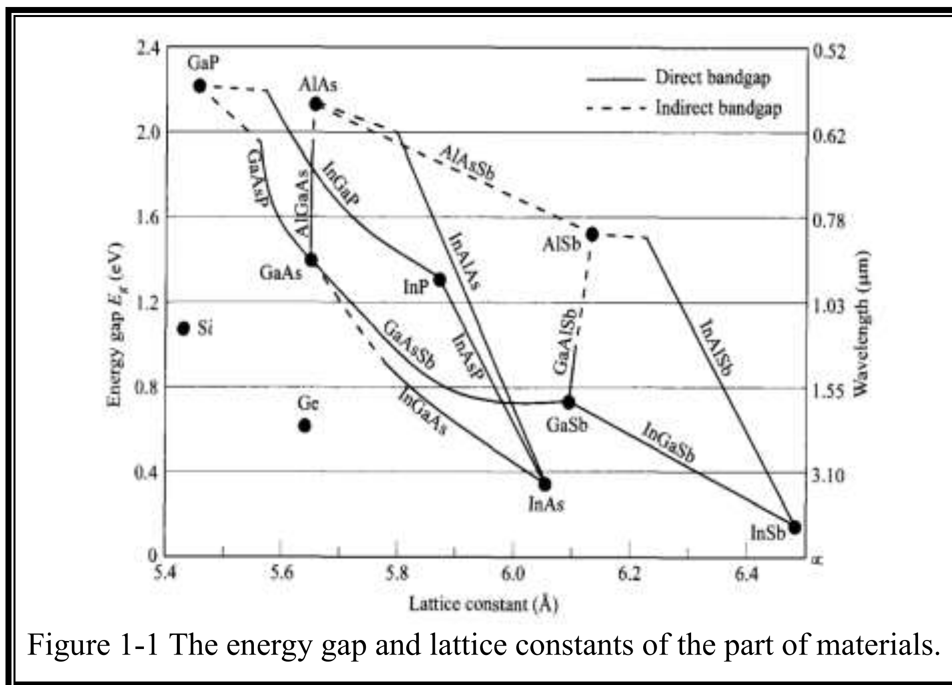

Figure 1-1 The energy gap and lattice constants of the part of materials.

§1.2. The AlGaN/GaN HFETs Technology

AlGaN/GaN heterostructure field-effect transistor (HFET) also called high electron mobility transistor (HEMT), is an important representative of GaN electronic devices. It is the focus of development and competition in the third generation semiconductor technology field. Because of its application prospects in the high temperature, high frequency, high power fields, AlGaN/GaN heterostructure becomes one of the hot spots in recent years. From the perspective of output power and frequency, AlGaN/GaN HFETs

are very suitable for high-frequency and high-power applications such as wireless communication base stations, radar and automotive electronics. In the aerospace, nuclear industry, military electronics, which require high chemical and thermal stability, AlGaN/GaN HFET is also one of the ideal candidate devices. These mainly benefits are from wide-bandgap, chemical stability and superior electrical characteristics of GaN.

Unlike SiC electronic devices, which depend on the electron mobility of the bulk materials, GaN-based materials are easy to fabricate heterostructure and can take full advantage of the superior properties of 2DEG. The AlGaN/GaN heterojunction material is one of the important representatives. It was reported that the carrier mobility can reach 2019 $cm^2/V \cdot S$ at 300K for the $Al_{0.22}Ga_{0.78}N$ heterojunction [34]. Besides, the highest mobility reached 5.17×10^4 $cm^2/V \cdot S$ for the $Al_{0.09}Ga_{0.91}N$ heterostructure at 13K [35]. Hence, AlGaN/GaN heterostructure has a more advantage than SiC in the manufacture of high frequency microwave devices. Table 1-1 shows the properties of several semiconductor materials.

GaN-based transistors, especially AlGaN/GaN HFETs have become a candidate of solid-state microwave power devices because of their performance to generate higher power densities at higher frequencies. The GaN-based material has unique properties of wide bandgap (3.4 eV of GaN to 6.2 eV of AlN), large breakdown electric field strength ($\sim 3.3\times10^6$ V / cm) and high saturation electron drift velocity ($>2\times10^7$ cm/s).

	Si	6H-SiC	GaN	GaAs
Bandgap (eV)	1.12	3.21	3.4	1.42
Lattice consta nt (nm)	0.543	0.308	0.319	0.565
Dielectric constant	11.9	10.32	10.4	12.9
Thermal conductivity (W/cmK)	1.56	4.9	1.3	0.46
Electron mobility (cm^2/Vs)	1450	400	1200 (bulk) 2000 (2DEG)	8000
Breakdown field (V/cm)	3×10^5	3×10^6	3.3×10^6	4×10^5

Table 1-2 Properties of main semiconductors.

Furthermore, the AlGaN/GaN heterostructure materials can generate 2DEG of ~10^{13} /cm^2 in the quantum well of the AlGaN/GaN heterostructure interface by polarized stress without any dopant, which much higher than the other III-V heterostructure materials system. The main reason is the strong spontaneous polarization and piezoelectric polarization effect exists in the AlGaN/GaN heterostructure materials. The higher density of 2DEG makes AlGaN/GaN HFETs have higher output current density. Coupling with the higher capability of withstand voltage, the transistors have typically higher output power density and are suitable for use in high power applications.

In summary, AlGaN/GaN HFETs have mainly four advantages.

Firstly, AlGaN/GaN HFETs have higher 2DEG density. Due to the strong polarization effect of AlGaN/GaN heterostructure, the density of 2DEG for the undoped AlGaN/GaN heterostructure can be as high as ~10^{13} /cm^2, which has one order of magnitude higher than that of the AlGaAs/GaAs heterostructure [36]. In addition, AlGaN/GaN HFETs have the superior characteristics, such as high transconductance, high saturation current and high cut-off frequency, owe to 2DEG electron mobility greatly enhancing.

Secondly, AlGaN/GaN HFETs can work at high temperature. The band gap of GaN is 3.4eV, which is three times that of Si and twice that of GaAs. AlGaN/GaN HFETs are suitable for high temperature work due to accurately controlling the free carrier

concentration in a considerable temperature range. Consequently, GaN-based devices have a higher work temperature than Si and GaAs based devices. In addition, GaN has high thermal conductivity that is three times that of GaAs, which effectively improves the heat dissipation characteristics of the devices and makes the GaN-based devices have better reliability under a high temperature environment.

Thirdly, AlGaN/GaN HFETs have well power characteristics. Because the breakdown electric field of GaN material is up to 3.3 MV/cm, AlGaN/GaN HFETs can work under high bias. In addition, the output power density of AlGaN/GaN HFETs on the SiC substrate is up to 10 W/mm, which is 20 times higher than GaAs-based devices. This reduces the size of the power device, improves the reliability of the device and reduces the fabricating cost of the device.

Finally, AlGaN/GaN HFETs have the strong anti-radiation ability. Due to the high chemical bond energy of the GaN material, the physical and chemical properties of the material is stable. It is not susceptible to external physical and chemical effects. Therefore, the devices of the GaN-based HFETs have better anti-radiation ability than GaAs-based devices. Combined with its high power density, AlGaN/GaN HFETs will be the best solid-state power devices for satellites with the comprehensive advantages of high power, small size, light weight and strong anti-radiation ability.

Therefore, AlGaN/GaN HFETs have broad application prospect in the fields of high temperature, high frequency and high power due to its superior electrical characteristics. And it has become a research hotspot in the field of microelectronic devices in recent years. Therefore, in-depth study of the basic characteristics of AlGaN/GaN HFETs is great significance for its development and real application.

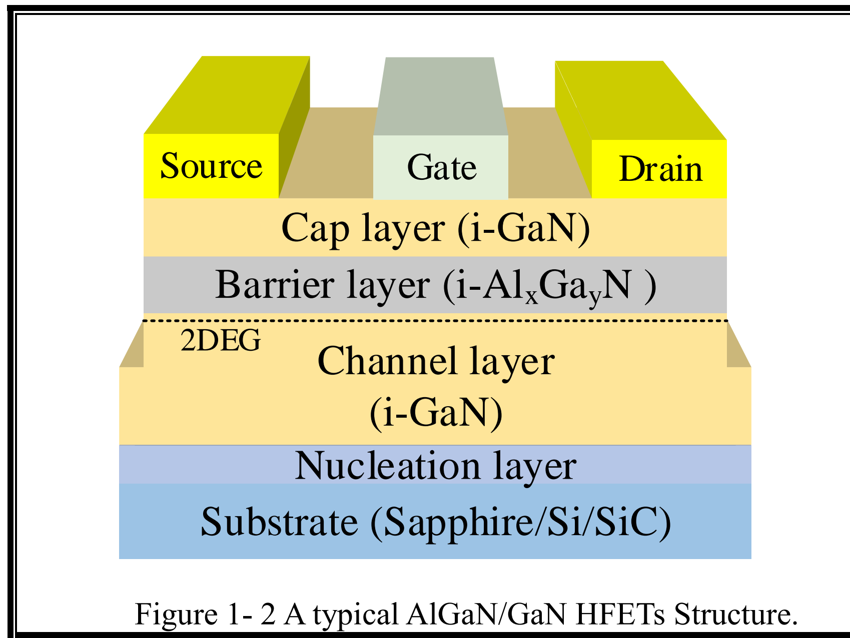

Figure 1- 2 A typical AlGaN/GaN HFETs Structure.

Figure 1-2 shows a typical AlGaN/GaN HFETs structure. MOCVD and MBE methods are usually used to grow the GaN-based HFETs epitaxial layers structure. The structure of AlGaN/GaN HFETs mainly consists five parts (from bottom to top): substrate, nucleation layer, channel layer, barrier layer, and cap layer.

Sapphire, Si and SiC are usually used as the substrate for AlGaN/GaN HFETs. Their properties are shown in Table 1-1. The lattice mismatch exists between these substrates and GaN. Where the lattice mismatch between SiC and GaN is minimal, but the manufacturing cost is relatively high.

To reduce stress and lattice mismatch from the nonnative substrate, nucleation layer is first grown on the substrates. And very thin AlN, AlGaN or GaN layer are usually used as the nucleation layer.

Channel layer (GaN in our case) is a material with the semi-insulating (SI) or high resistivity which is to ensure complete channel pinch-off, low loss at high frequencies, low cross-talk between adjacent devices and proper drain-source current saturation. On the side, the channel layer has a lower bandgap than barrier layer.

After growing the thicker channel layer, a 20 nm thickness Al_xGa_yN layer is grown as the barrier layer, which is the most critical layer in HEMT structure. The bandgap of this material depends on the aluminium mole fraction x and is higher than the channel layer [37].

Cap layer is deposited on top of the barrier layer, which is beneficial to prevent the form low resistance Ohmic contact, act as gate insulate, oxidation of barrier layer surface, etc. [38, 39] It is usually a 1-2 nm thick GaN layer.

By optical lithography and reactive sputtering technology, three metal electrodes, source (S), gate (G), and drain (D), are formed on the top cap layer. Both the source and drain terminals are ohmic contacts.

The source is typically grounded. The drain with a positive bias can control the flow of carriers in the 2DEG from the source to the drain in a direction parallel to the heterogeneous interface. The potential distribution of the heterostructure can be controlled by the gate. The structure of gate has generally the following three kinds: Schottky contact, p-n junction and metal-insulator-semiconductor (MIS).

In our previous work, Ni and TiN electrodes are normally used to develop GaN Schottky diode. TiN has lower turn-on voltage and comparable breakdown voltage comparing with Ni. However, the reverse leakage current is relative higher [40]. To suppress the reverse leakage current, new gate structure is necessary.

§1.3. The motivation of this reaserch

In the realization of GaN power switching device industrialization, there are still facing with many technical difficulties. Based on the viewpoint of safety, normally-off operation is strongly required. At present, there are three ways to fabricate the normally-off type GaN devices: junction gate structure (p-type gate), cascode structure and trench gated MOSFET. At present, the first two structures have been achieved industrialization. However, multi-chip packaging for Cascode normally-off GaN devices reduces the reliability of the device, and the p-type gated normally-off GaN devices has the small threshold voltage, the large gate leakage, the small gate voltage swing redundancy and the bad resistance to electromagnetic interference. The structure of the trench gate is expected to replace the above-mentioned methods because of its large gate voltage swing redundancy and small gate leakage current.

Because the 2DEG density has to be reduced to obtain the normally-off characteristics, we can choose the p-type oxide layer as recessed gate material.

In addition, the AlGaN/GaN HFETs are considered as the most promising materials for

high-frequency and high-power electronic devices. It is satisfactory to provide a gate contact with large Schottky barrier height (SBH) and prominent thermal stability to achieve the high-temperature performance. To achieve a high-temperature performance, it is very desirable to produce a gate contact with a large SBH and an excellent thermal stability. In the applications of high-frequency, a self-aligned gate (SAG) process comes up with minimizing the distances of source-to-gate and drain-to-gate for a smaller access resistance, in which a T-shaped Schottky gate is firstly manufactured and then applied to a mask directly for ohmic metal formation.

After that, the Schottky gate and the ohmic electrodes are treated by annealing synchronously to attain ohmic contacts. Establishing the Schottky gate is a significant method which can stand up to ohmic annealing process in order to constitute the SAG structure, due to the optimal annealing temperature for ohmic contact of the Ti-based multilayers on GaN-based materials is approximately 800 to 850 °C. Therefore, the Schottky gate must be capable of withstanding such a high temperature during the annealing process of source-drain ohmic contact. In previous studies, Ao-lab has evaluated the electrical performance of Schottky contacts fabricated by many different types of refractory metal nitrides, such as HfN, TiN, MoSiN, MoN, TaN, ZrN and WTiN on GaN deposited by reactive sputtering in Ar and N_2 mixed ambient environment. Take many factors into consideration, such as adhesion on GaN, sheet resistivity, reverse leakage current, SBH, and thermal stability of these devices, TiN is considered as one of the most suitable materials for the Schottky electrodes. It is easy to obtain by a simple method reactive sputtering with nitrogen ambient environment and shows a relatively smaller resistivity, better adhesion, and smaller leakage current of the GaN Schottky contact. To suppress the leakage current of the AlGaN/GaN HEMT with TiN gate, it is also necessary to develop a metal-insulator semiconductor (MIS) or metal-oxide-semiconductor (MOS) HEMTs using SiO_2, ZrO_2, Al_2O_3 and other oxides.

Another purpose of my research is to fabricate a kind of MIS-gate AlGaN/GaN HFET by using oxide/TiN stack structure or other dielectrics created by sputtering. By this approach, the interface between the oxide layer and the gate metal can be improved owing to the sample is kept in vacuum ambient environment. To achieve this proposal, it is necessary to find a suitable dielectric material which can stand annealing temperature at about 850°C.

§1.4. Outline of thesis

This thesis reports on the Synthesis and Application of Oxide for Gallium Nitride Electron Devices. This thesis is divided into four parts:

In Chapter 2, we deposited the NiO films under different O_2/Ar ratios and substrate temperatures, which are face-centered cubic crystalline structure. The NiO films possess direct bandgaps of 3.6, 3.2, 2.7, and 3.0 eV at O partial pressures of 15%, 25%, 50%, and 65%, respectively. The crystalline structure, composition, electrical and optical properties of the as-grown films depend on the substrate temperature. When the substrate temperature increasing, the crystalline quality and stoichiometric of NiO film were improved, resulting in higher bandgap value and resistivity. NiO film obtained at a substrate temperature of 30 °C shows the smallest resistivity, which is suitable for gate electrode for AlGaN/GaN HFETs. Besides, compared with the Ni/GaN Schottky diode, the turn-on voltage of the NiO/GaN heterojunction diode is relatively higher and shows a much smaller reverse leakage current.

In Chapter 3, we explored the temperature-dependent behavior of a NiO/GaN heterojunction diode in this work. The cubic crystalline structured NiO film exhibited p-type semiconducting behavior. The heterojunction diode showed an excellent stability over the temperature range of 25–175 °C. The turn-on voltage of the devices decreased from 2.2 to 1.5 V with increasing temperature. The device characteristics in forward bias were dominated by three types of current transport mechanisms and were found to be dependent on the applied bias voltages and temperature.

In Chapter 4, NiO film obtained at a substrate temperature of 30 °C shows the smallest resistivity and was used as gate electrode for AlGaN/GaN HFETs application. Compared with the Ni/Au-gated device, the band structure adjustment introduced by p-NiO gate was found to shift the threshold voltage positively and then cause a smaller drain current. The valence and conduction band offsets between NiO and GaN are estimated to be 1.25 eV and 1.42 eV using X-ray photoelectron spectroscopy.

After recess, the threshold voltage for the Ni- and NiO-gated HFETs has a positive shift with the smaller drain current density. With the recessed-gate structure, normally-off GaN HFETs can be obtained with a threshold voltage of closing to 0 V. Meanwhile, the

existence of p-type NiO gate layer can decrease the tunneling of electron and leakage current.

In Chapter 5, we fabricated the high-*k* material HfO_xN_y with different oxygen flow rates in the reactive sputtering ambient. It demonstrated that the surface morphologies, composition, and optical properties of the HfO_xN_y films were dependent on the oxygen flow rate in the $O_2/N_2/Ar$ mixture sputtering ambient. The synthesis conditions had been also optimized. We focus on the thermally stable HfO_xN_y was deposit as gate dielectric for $TiN/HfO_xN_y/AlGaN/GaN$ heterostructure field-effect transistors application. The obtained metal-oxide-semiconductor heterostructure field-effect transistors possessed a small hysteresis and a low leakage current by depositing HfO_2 and HfO_xN_y dielectric at different oxygen flow rates. After post deposition annealing at 900 ^oC, the device using HfO_xN_y dielectric operated normally with good pinch-off characteristics, while obvious degradation are observed for the HfO_2 gated one at 600 ^oC. This result shows that the HfO_xN_y dielectric is a promising candidate for the self-aligned gate process.

The conclusions of the dissertation and the future plans to improve the performance of the devices are given in Chapter 6.

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Chapter 2 : Synthesis and characterization of NiO

§2.1. Selection of material

In today's rapid development of science and technology, the requirements for new materials are also increasing. The traditional and single materials can no longer meet the needs of the progress of the times. Looking for new materials with excellent performance can break the inherent limitations of old materials to meet the needs of scientific and technological development. Materials such as semiconductors, metals, ceramics and polymers are now developed rapidly. In particular, the development of semiconductor materials have brought human into the information age. Without semiconductor materials, there would be not computer technology, and modern people have not a rich and colorful lives. In the human society, semiconductor materials have developed more than one century, which has gone through leapfrog development with three generations. The third-generation semiconductor materials represented by GaN and SiC are still in the developmental stage [1-4]. The third-generation semiconductor materials can more meet the requirements of the modern electronic technology with high-temperature and high-frequency performance. However, these materials have some obvious problems in the field of optoelectronic devices and microelectronic devices, such as the difficulty of commercialization for large-size substrates, excessive temperature in the preparation of materials, and the reliability and stability of p-type materials, all of which have caused people to research, develop and design new materials according to predetermined performance.

There are several p-type materials, such as p-type GaN, Cu_2O, NiO, and so on. GaN is doped with Mg to form p-type GaN at the temperature of about 1010 ^oC [5]. It has low carrier concentration of approximately $10^{17}/cm^3$. Cu_2O is a natural p-type material, which is fabricated at room temperature with low carrier concentration of approximately $10^{17}/cm^3$. But Cu_2O is instable with easily oxidizing into CuO [6]. NiO is also a natural p-type material with synthesis under room temperature. It has high carrier concentration of approximately $10^{18}/cm^3$, which can as much as possible deplete 2DEG of HFETs to form normally-off devices. So NiO is an expected material.

NiO is a 3d transition metal oxide [7-8] and a typical direct wide bandgap p-type

semiconductor. The bandgap of the NiO film is usually 3.6eV~4.0eV [9-11]. The basic physical properties in shown in Table 2-1. Due to its unique electronic structure, NiO has shown excellent application prospects in many fields such as transparent conductive films, gas sensors, UV detectors and electrochromic devices, etc. [11-18].

NiO is a p-type semiconductor with a wide range of applications, such as nonvolatile memory devices, as a functional layer material in chemical sensors, transparent conductive films, UV photodetector and electrochromic devices. NiO is a promising material applicable to nonvolatile memory devices due to its high on/off ratio and simple constituents. In recent years, the photocatalytic degradation of various kinds of organic and inorganic pollutants using semiconductor powders as photocatalysts has been extensively studied NiO can be doped into semiconductors, such as TiO_2, $InVO_4$, $NaTaO_3$, etc., as photocatalyst [19-20]. Due to its excellent performance, NiO is used to fabricate transparent p-NiO/n-ZnO heterojunction devices for ultraviolet photodetectors [21]. The p-NiO/n-ZnO heterojunction device has an average transmittance of over 80% in the visible region. The p-NiO/n-ZnO heterojunction device can detect ultraviolet light by the application of reverse bias. As a typical natural p-type semiconductor material, NiO has attracted many researchers due to its special properties and wide application.

Name	NiO
Relative density	6.6-6.8
Melting point	1984 ºC
Molecular mass	74.7 g.mal-1
Band-gap	3.6-4.0 eV
Conduction type	direct-band-gap p-type
Solubleness	insoluble in water and lye, soluble in acid, ammonia, hot perchloric acid and hot sulfuric acid, etc.

Table 2-1 The physical properties of the NiO film.

The usual stable NiO structure belongs to the Fm3m space group of cubic crystal system with the same crystal structure as NaCl. The distance between Ni^{2+} and the nearest O^{2-} is $a\times10^{-8}$ cm and the lattice constant is a=b=c=0.418 nm [22]. Figure 2-1 shows a diagram of the common NiO crystal structure. The stoichiometric ratio of Ni to O obtained by different preparation methods is different from the normal case. However, to

sum up there are basically NiO, Ni_2O_3 and Ni_3O_4 or their mixture, where it is dominated by NiO, Ni_2O_3 and their mixture. Ni_2O_3 is usually the dark brown solid, which is converted directly to NiO after high temperature treatment [23].

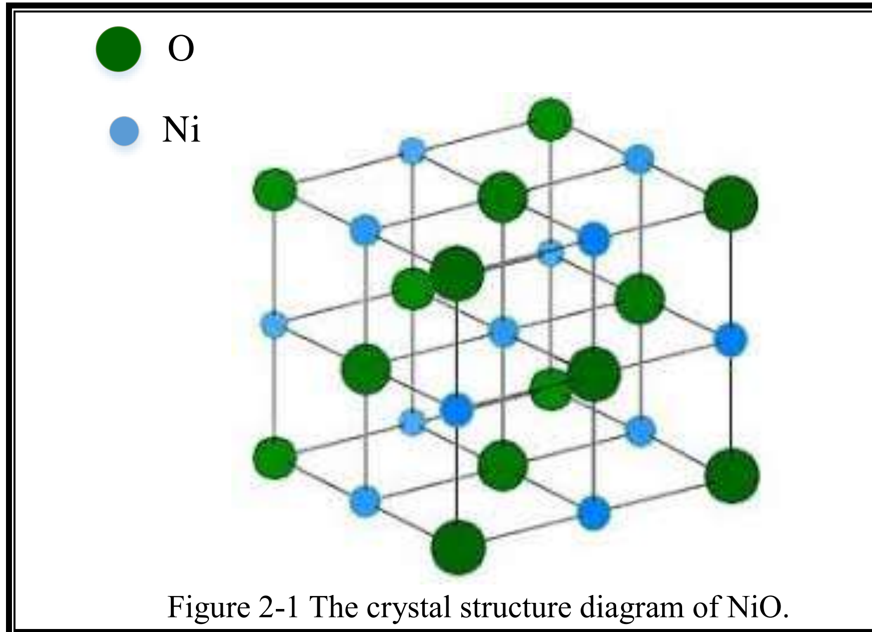

Figure 2-1 The crystal structure diagram of NiO.

NiO has the closely matched lattice constants and bandgap energy (3.6 eV) with GaN, which makes NiO as a promising candidate for applications in GaN-based heterojunction devices. Furthermore, the natural p-type NiO can reduce the amount of field crowding as guard ring at the main junction, which is an effective method obtain high breakdown voltage. In this thesis, NiO thin film was prepared by magnetron reactive sputtering on an n-GaN/sapphire substrate to form the NiO/GaN heterojunction diode.

§2.2. The synthesis of NiO

§2.2.1. The synthesis of NiO films with different oxygen ratio

In this experiment, the n-GaN layers were deposited on (0001) sapphire substrate by MOCVD. The standard photolithography and lift-off technology were utilized to form both ohmic and Schottky contacts. The cathode ohmic contact was constituted by a Ti/Al/Ti/Au (50/200/40/40 nm) multi-layer structure followed by annealing at 800 °C in N_2 atmosphere for 1 min. Before Schottky deposition, the samples were surface-cleaned

by O_2 plasma ashing and then immersed in diluted HCl ($HCl:H_2O=1:1$) solution for 5 min to remove the possible oxide layer after lithography. NiO film was deposited by reactive sputtering (RF, 75 W) in different O percentage of 15%, 25%, 50%, and 65%, using a metal target of Ni. A NiO/Ni/Au (30/10/40 nm) stack film was deposited for anode Schottky electrode. For comparison, sample with Ni/Au (30/40 nm) electrode was also deposited by RF sputtering in Ar atmosphere under a sputtering power of 150 W and a chamber pressure of 0.14 Pa. Finally, the samples were treated by post-annealing at 300 °C in N_2 atmosphere for 10 min.

§2.2.2. The synthesis of NiO films at different substrate temperatures

In order to evaluate the influence of substrate temperature on the material performance, NiO films were first formed on double-sides polished sapphire substrates using reactive sputtering. A nominal 100 nm NiO layer was deposited under different substrate temperatures of 30, 100, 200 and 300 °C, respectively, in Ar and O_2 ($Ar:O_2=15:5$ sccm) mixed ambient with a Ni target. The sputtering power was fixed at 75 W with a chamber pressure of about 0.13 Pa. The sputtering target was firstly cleaned in Ar atmosphere for 10 min with a sputtering power of 150 W. In this study, X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and UV-Vis absorption spectrum were utilized to characterize the structure, morphology, and optical properties of the as-deposited NiO films.

§2.3. The characteristics of NiO films

§2.3.1. The properties of NiO films with different oxygen ratio

NiO film (approximately 100 nm) was deposited on a polished sapphire substrate using different oxygen percentage of 15%, 25%, 50% and 65% at room temperature for the x-ray diffraction (XRD), atomic force microscope (AFM) and optical transmittance measurements.

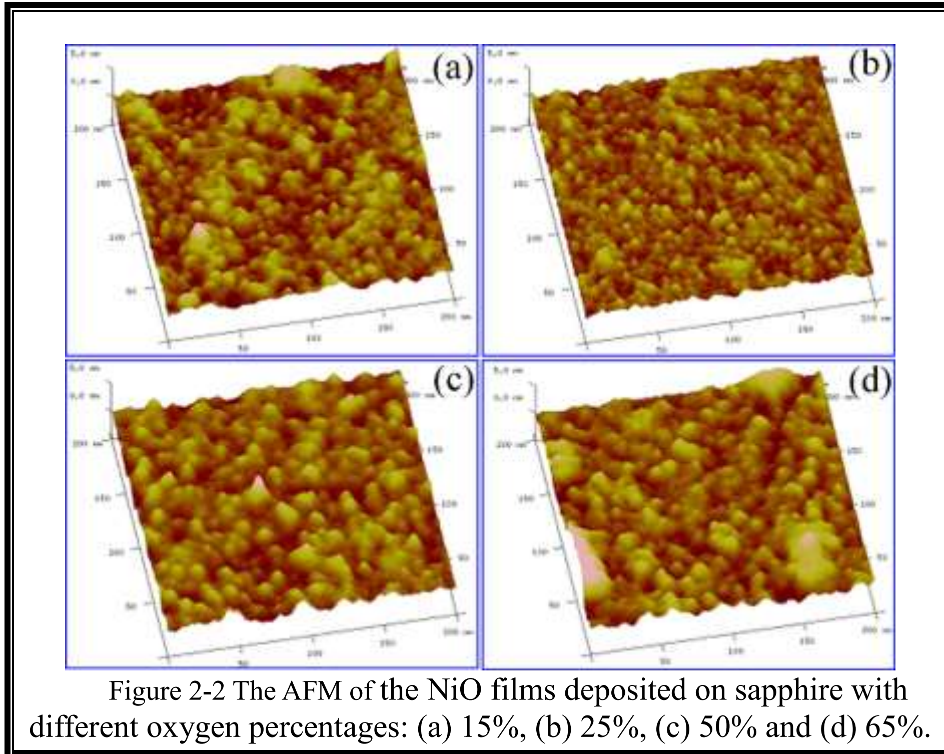

Figure 2-2 The AFM of the NiO films deposited on sapphire with different oxygen percentages: (a) 15%, (b) 25%, (c) 50% and (d) 65%.

The surface morphology and the root mean square roughness (RMS) of NiO films with different oxygen percentages are characterized using AFM (as shown in Figure 2-2) which is scanned in an area of 0.2μm×0.2 μm. With the low oxygen percentage, the surface of the samples consist with high density and small size particle (Figure 2-2 a and b). The RMS of those samples are approximately 0.35 and 0.29 nm, respectively. For the sample deposited with the oxygen percentage of 50%, the grain size increased obviously (Figure 2-2 c) and its RMS is about 0.37 nm. Finally, Figure 2-2 d showed the most rough morphology with a RMS of approximately 0.46 nm for the film with 65% oxygen percentage. Therefore, the surface of the film with 25% oxygen percentage is the most flat. The sputtered NiO on the sapphire substrate with high oxygen percentage will has the deterioration of the film quality. The oxidation of the Ni target is very weak at a relatively low oxygen percentage. The sputtered Ni atoms has enough time to diffuse and react from the target surface to substrate surface, resulting in a better surface roughness. While, the oxidization of metal target surface is much easier at a relatively high oxygen percentage, which suggest there are not enough Ni atoms to escape from the target and react with O atoms to deposit on the substrate.

Usually, the first several nanometers of film deposited by sputtering is amorphous,

which can serve as the stress buffer layer for lattice mismatch. Besides, the room temperature sputtering is also helpful to reduce the thermal stress between the film and substrate. Therefore, we think the influence of stress on the XRD measurement is relatively weak. In the XRD spectrum (Figure 2-3) for the samples with the low oxygen percentage (15% and 25%), two peaks are generally observed at around 37.5^{o} and 78.2^{o}, which are assigned to the face-centered cubic crystalline diffraction patterns of (111) and (222) respectively [24]. With the increase of the oxygen percentage (50%), the crystalline texture is changed, which a more peak of (220) is appeared at around 65.3^{o}. While for the film with the oxygen percentage of 65%, it is dominated by (111) which is also assigned to the face-centered cubic crystalline diffraction pattern. As the oxygen percentage increasing, the peaks became broad and weak, which suggested the crystalline quality is deteriorated. Using the full-width at half maximum (FWHM) of (111) peak, the mean grain size of the film is estimated by Scherrer formula as following [25]:

$$D = K\frac{\lambda}{\beta cos\theta} \quad (2\text{-}1)$$

Where D is the diameter of the grain, K=0.89 is the Scherrer constant, λ=0.154 nm is the wavelength of the X-ray, β is the FWHM of the peak and θ is the Bragg diffraction angle. From Figure 2-3 it is observed that the FWHM increases with increasing the oxygen percentages, which indicates the mean grain size of the films increases. It accord with the result of AFM. We calculated the mean grain size of the film with oxygen percentages of 25% is approximately 3.7 nm.

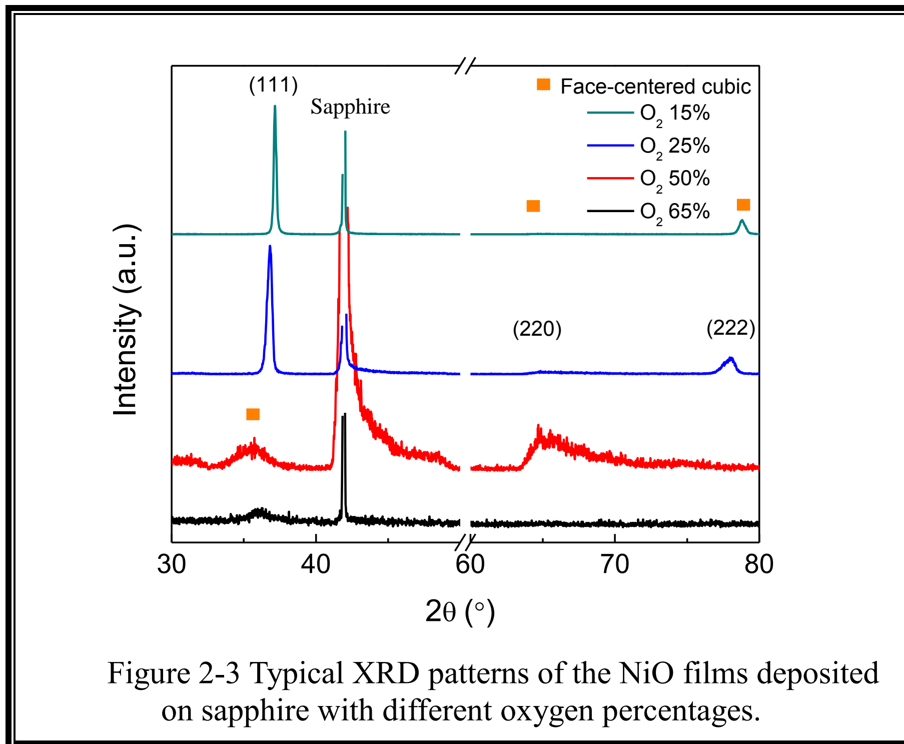

Figure 2-3 Typical XRD patterns of the NiO films deposited on sapphire with different oxygen percentages.

The optical properties of the films are characterized by UV-Visible transmission spectra. The NiO films with different oxygen percentages is grown on the double polished sapphire in order to obtain exact results by magnetron sputtering (the inset in Figure 2-4). Figure 2-4 shows optical transmittance spectra of the deposited NiO films (approximately 100 nm) at various oxygen percentages. It can be clearly observed absorption coefficient as a function of photon energy. The following equation can calculate absorption coefficient [26]:

$$T = C\exp(-\alpha t) \qquad (2\text{-}2)$$

Where T is the transmittance of the film, α is absorption coefficient, C is a constant, and t is the film thickness (approximately 100 nm). Because of the negligible reflectivity near the absorption edge, C is approximately in unity. The absorption tail of the NiO films with different oxygen ratio is shown in Table 2-3. With the oxygen ratio increasing from 15% to 50%, the absorption tail increasing from 346 nm to 459 nm, which suggests that the absorption of the film moves to the visible direction. As the oxygen content continues to increase, the absorption tail decreases to 417 nm. By applying the following Tauc model and the Davis and Mott model, the optical band gap (E_g) of the films was extracted from the absorption edge [27].

$$\alpha h\nu = \mathrm{D}(h\nu - E_g)^n \tag{2-3}$$

Where Eg is the optical band gap, D is a constant, and h is the photon energy. Here, n is 1/2 because of the direct bandgap of NiO films. The optical band gap of the film was extracted from absorption edge by applying the Tauc model, and the Davis and Mott model. By extrapolating the linear part to the zero absorption coefficients, we obtained the E_g value. As shown in Table 2-3, with increasing oxygen percentage from 15% to 50%, the band gap of the films decreases from 3.58 to 2.7 eV and increased by 2.97 eV at a higher oxygen percentage of 65%. As shown in XRD spectra, the bandgap increase for 65% oxygen is not very clear because maybe the crystalline structure is the changed, which is dominated by (111) texture. While it is shown a (111) and (220) texture for the film deposited with 50% oxygen. Meanwhile, the absorption edge for the samples with high oxygen percentage (50% and 65%) are not very clear, which can cause no exact calculation of the band gap.

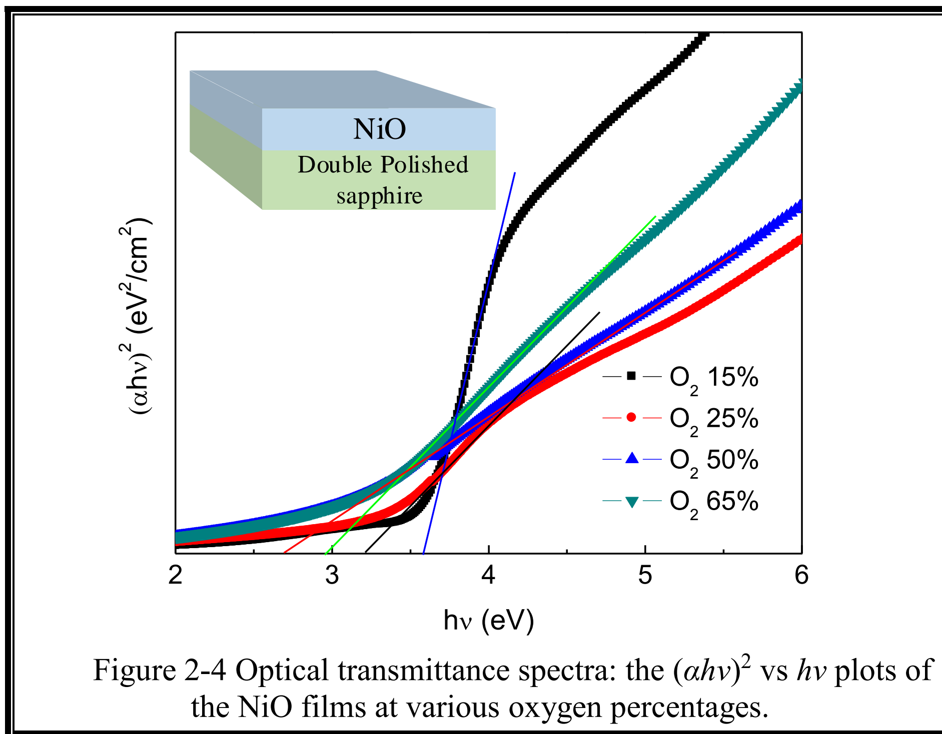

Figure 2-4 Optical transmittance spectra: the $(\alpha h\nu)^2$ vs $h\nu$ plots of the NiO films at various oxygen percentages.

Oxygen ratio	Absorption tail (nm)	Bandgap (eV)
15%	346	3.58
25%	387	3.2
50%	459	2.7
65%	417	2.97

Table 2-3 The absorption tail and bandgap of the NiO films with different oxygen percentages.

The magnetron sputtering has the potentials of large area, good uniformity, and easy to obtain stack electrode. For reactive sputtering method, the structural, electrical, and optical properties of the NiO are usually dependent on the oxygen partial pressure, power, substrate temperature, and so on [28, 29]. However, many works also suggest that the preferred orientation and crystalline quality of NiO film show a relationship with the substrate temperature [28].

§2.3.2. The properties of NiO films with different substrate temperatures

By analyzing the normalized XRD patterns of the NiO samples grown at different growth temperatures (Figure 2-5), two diffraction peaks at around 36.8°, and 78.3° dominate the spectra, which are indexed to the face-centered cubic crystalline diffraction patterns of NiO (111) and (222), respectively [30]. With the substrate temperature increasing from 30 to 200 °C, the diffraction peaks are intensified with a smaller FWHM value. Besides, the diffraction peaks show obvious movement towards higher 2-theta (2θ) values with the increasing temperature. Usually, the reaction between the Ni and O_2 was insufficient when the substrate temperature was low, the high density of interstitial oxygen and Ni vacancies in the film will cause the deterioration of crystalline quality (expansion of lattice parameter) and non-stoichiometric film. While for higher substrate temperature, atoms arriving at the substrate surface will possess higher kinetic energy, which is beneficial for the migration and reaction to obtain a better crystalline quality.

The movement towards higher 2θ values of the XRD peaks indicate an improvement in the crystalline quality of the NiO film (close to the stoichiometric status). However, the enhancement of crystalline quality (intensity and FWHM) is inconspicuous at the temperature of 300 °C because of the decomposition of NiO as shown in the following XPS measurements [31].

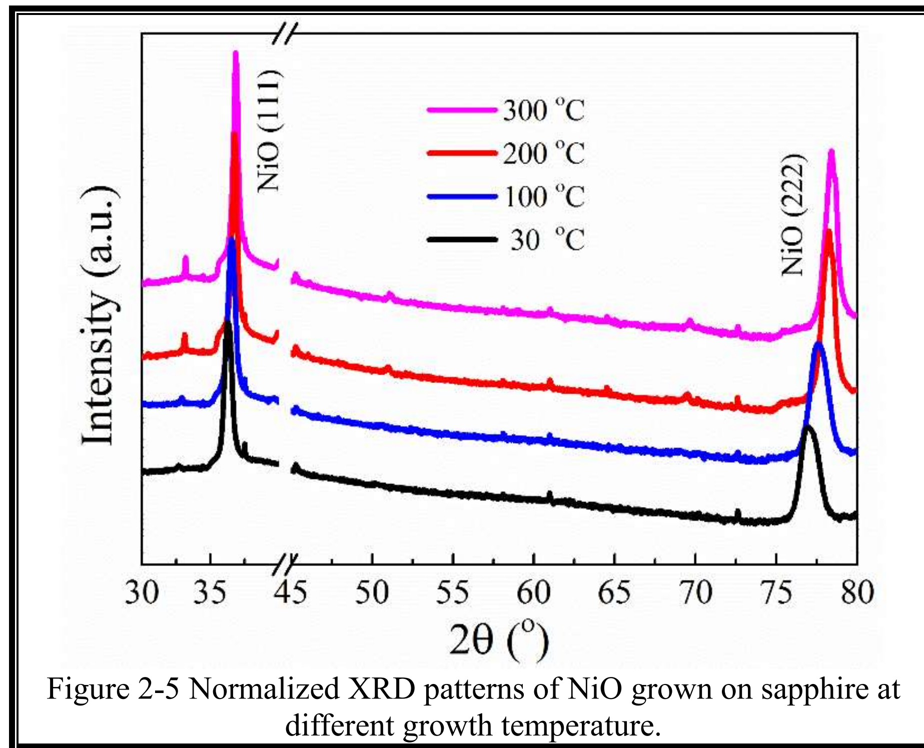

Figure 2-5 Normalized XRD patterns of NiO grown on sapphire at different growth temperature.

The composition variation of the NiO films were further identified using XPS, as plotted in Figure 2-6. $Ni2p^{3/2}$ spectrum for the sample obtained at 30 °C is composed by three peaks (fitted using Voigt line shapes and Shirley background), that is, the Ni^{2+} ($2p_{3/2}$), Ni^{3+} ($2p_{3/2}$) as well as a satellite peak at around 854.1, 855.9, and 861.3 eV, respectively. Usually, the binding energy at 854.1 and 855.9 eV are ascribed to NiO and Ni_2O_3, which represents that the films contain both NiO and Ni_2O_3 [32]. Besides, the satellite peak is ascribed to some factors such as multi-electron excitations, multiple splitting or surface plasmon loss [33]. When the substrate temperature increases to 100 and 200 °C, the positions of peaks are nearly the same as the low temperature one. However, the intensity ratio of Ni^{2+}/Ni^{3+} is enhanced with the increasing substrate temperature, which indicates that the NiO film becomes much close to the stoichiometric state with a lower Ni_2O_3

content. This is consistent with the XRD results. While for the sample obtained at a substrate temperature of 300 °C, a new peak at around 851.9 eV appears and can be assigned to Ni^0. The weak Ni^0 peak indicates the existence of Ni metal which maybe ascribes to dissociation of the NiO molecule into Ni and O [34].

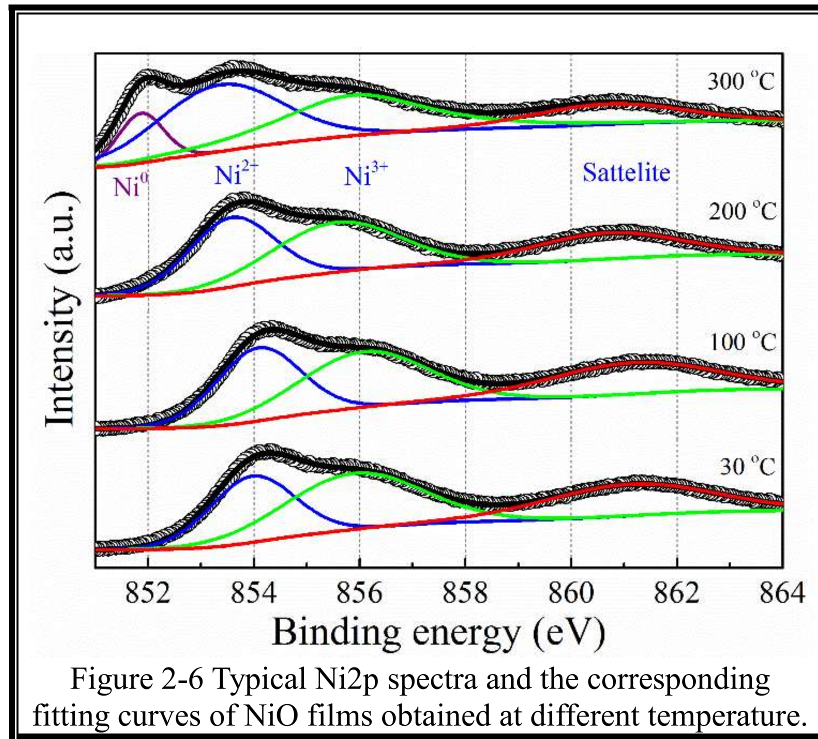

Figure 2-6 Typical Ni2p spectra and the corresponding fitting curves of NiO films obtained at different temperature.

The band gap is another key parameter to evaluate the effect of the substrate temperature on the NiO film. The transmission spectra was used to study the optical properties as shown in Figure 2-7. All samples present an obvious absorption tail near 320 nm and an optical transmittance of approximately 50% in the visible range. The optical band gap of the NiO films (inset of Figure 2-7) were obtained to be approximately 3.57, 3.62, 3.61, and 3.62 eV at 30, 100, 200, and 300 °C, respectively. It is worth noting that the absorption edges for the samples with relatively lower temperature (30 and 100 °C) are not very clear, indicating the inferior crystalline. This result is in good agreement with the structural and compositional analysis as described in the above sections.

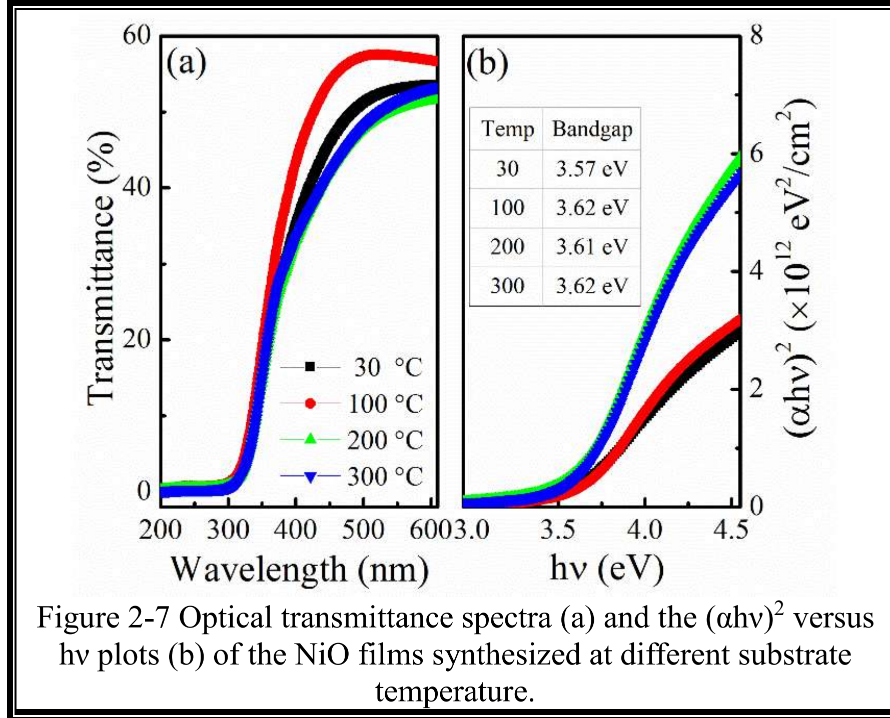

Figure 2-7 Optical transmittance spectra (a) and the $(\alpha h\nu)^2$ versus hν plots (b) of the NiO films synthesized at different substrate temperature.

§2.4. The contact of materials on n-GaN

The well-known thermionic emission TE theory analyzed the experimental current–voltage (I-V) data of Schottky contact. The TE theory predicts that the I-V characteristic is given at forward-bias as follows [35]

$$I = A_e A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right)-1\right] \tag{2-4}$$

Where A_e is the effective diode area, $A*$ is the effective Richardson constant of 26.8 $A \cdot cm^{-2} \cdot K^{-2}$ for n-type GaN, q is the electron charge, T is the absolute temperature, k is the Boltzmann constant, V is the forward-bias voltage, n is the ideality factor and Φ_b is the experimental zero-bias apparent barrier height.

When $qV \geq 3kT$, $\exp\left(\frac{qV}{nkT}\right) \geq 1$, the equation can be simplified as

$$I = A_e A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right)\exp\left(\frac{qV}{nkT}\right) \quad \text{or} \quad J = A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right)\exp\left(\frac{qV}{nkT}\right) \tag{2-5}$$

Then, $$\ln J = \frac{qV}{nkT} + \ln\left(A^* T^2\right) - \frac{q\phi_b}{kT} \tag{2-6}$$

The intercepts and slopes of the forward-bias *lnI* versus *V* plots can confirm the experimental values of the barrier height and the ideality factor for the device, respectively.

We fabricated the circular-type diodes with 30 nm Ni and NiO (25% O) electrodes on Si-doped n-GaN (3×10^{17} cm^3) to evaluate the electrical properties. The room temperature *I-V* characteristics of the Ni and NiO diodes in the logarithmic plot and the linear plot of the forward region are shown in Figure 2-8. Both of the samples showed good rectifying characteristics (Figure 2-8 a). The series resistance calculated from the slope of linear area in the forward current-voltage curves are approximately 1.9 and 9.4 Ω for Ni and NiO electrode, respectively. The Schottky barrier height (SBH) and the ideality factor of the Ni diode were approximately 0.97 eV and 1.5, respectively, when the thermionic emission theory was used. The reverse current leakage of Ni was generally higher than that calculated with an SBH of 0.97 eV. The leakage current of Ni diode increases due to the interface states at the Ni/GaN interface caused by the interaction, which led to a defect-assisted tunneling effect. The reverse leakage current of the NiO heterojunction diode was approximately one order smaller than Ni Schottky diode. The reverse saturation current and ideality factor for the NiO heterojunction diode were approximately 8.6×10^{-13} A and 3.11, respectively. The high ideal factor may be due to the interface state, which is caused by dangling bonds, surface defects, defective native oxides and contamination. Preprocessing optimization is necessary in the future. Figure 2-8 b shows the turn-on voltages at room temperature were approximately 0.71 and 1.73 V for the Ni and NiO electrodes, respectively.

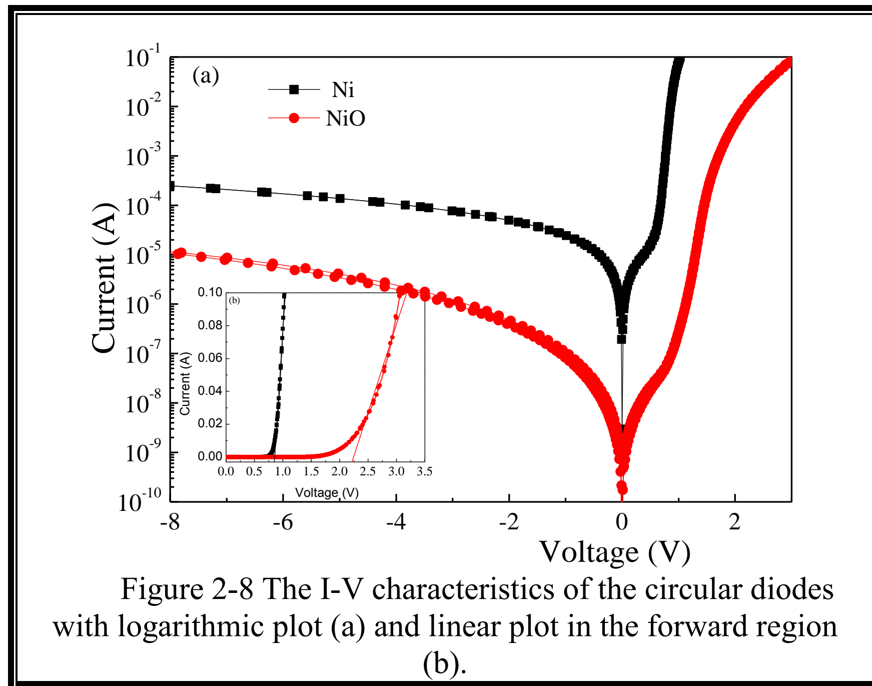

Figure 2-8 The I-V characteristics of the circular diodes with logarithmic plot (a) and linear plot in the forward region (b).

§2.5. The resistivity of NiO film

§2.5.1. The resistivity of NiO film with different oxygen ratio

Transmission Line Model (TLM) is efficient method for evaluating the quality of ohmic contact. Figure 2-9 shows a schematic diagram of the circular TLM test structure.

For obtaining an accuracy measurement, the circular TLM test patterns were fabricated in the isolated mesa. It consists of six circle metal contact pads with different inside and outside diameter. The mesa structure can make the two area non-conductive. The total resistance between two circles separated by a distance (R_2-R_1) is measured by the four point probe method and is estimated by the equation followed as:

$$R = \frac{0.03R_c}{2\pi} + \frac{R_\square}{2\pi}\ln(\frac{R_2}{R_1}) \quad (2\text{-}7)$$

Where R_c is the ohmic contact resistance, $R_\square$ is the sheet resistance. It is supposed $x = \frac{1}{2\pi}\ln(\frac{R_2}{R_1})$. By plotting R as a function of x, the data can be linearly fitted and the R_s and R_c can be calculated from the intercept and slope.

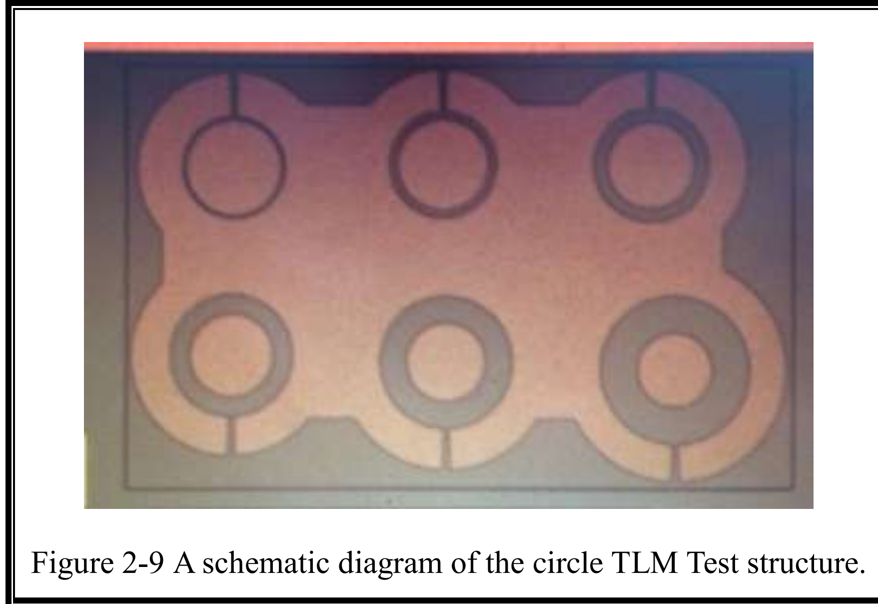

Figure 2-9 A schematic diagram of the circle TLM Test structure.

A Ni/Au (10/40 nm) stack film was deposited on NiO/sapphire with a circular TLM patterns to obtain the ohmic contact resistance (Rc) and sheet resistance of NiO film. Circular TLM was chosen for its simplicity since no separate mesa isolation etching was needed. Figure 2-10 a shows the I–V characteristics recorded on the TLM patterns with an interval of 5, 10, 15, 20, 25, and 30 μm, respectively. The linear curves suggest the good ohmic contact behavior was formed between the Ni/Au metal stack and NiO. R_c of 1.22×10^6 Ωμm and $R_\square$ of 2.73×10^6 /□ were obtained from the plot of the corresponding resistance versus the interval (Figure 2-10 b). We had studied the room temperature electrical properties of NiO film, using Hall measurement in van der Pauw arrangement. The NiO thin film exhibited p-type semiconducting behavior. Hall mobility is about 0.85 $cm^2 V^{-1} s^{-1}$. The estimated values of electrical resistivity was approximately 6.3 Ωcm, in addition, the concentration of holes was near 1.16×10^{18} cm^3 [36].

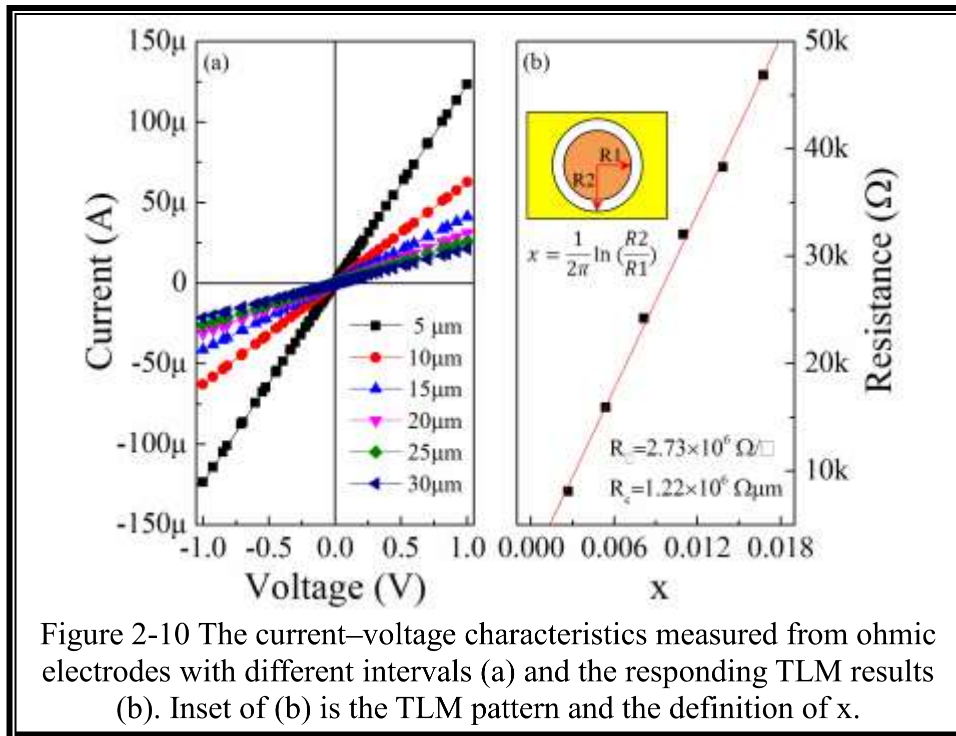

Figure 2-10 The current–voltage characteristics measured from ohmic electrodes with different intervals (a) and the responding TLM results (b). Inset of (b) is the TLM pattern and the definition of x.

§2.5.2. The resistivity of NiO film with different substrate temperature

The sheet resistivity of NiO films synthesized at different substrate temperatures were measured by a circular TLM patterns due to the simplicity of no separate mesa isolation is needed. Ni/Au (70/30 nm) stack electrodes were deposited on NiO/sapphire to evaluate the electrical characteristics of NiO films at different substrate temperatures. Typical I-V curves recorded on different samples (Figure 2-11) shows obvious linear characteristics, representing that good ohmic contact behavior was formed between the NiO films and Ni/Au metal stack. When the substrate temperature increased from 30 to 200 °C, the resistivity of films increases significantly from approximately 7 Ωcm to 114.41 Ωcm. The origination of p-type conductivity in non-stoichiometric NiO film was ascribed to the replacement of one Ni^{2+} vacancy by two Ni^{3+} ions [37]. Based on the XRD and XPS results, the intensity ratio between Ni^{2+}/Ni^{3+} is enhanced with the increasing substrate temperature. Then, the nickel vacancy density (hole concentration) decreased in the samples grown at higher substrate temperatures, resulting in higher resistivity. However, the resistance decreases to approximately 78.42 Ωcm at temperature of 300 °C because of the appearance of NiO phase. The existence of Ni metal can provide better conductivity although the electron will partially compensate the hole concentration as reported in our

previous work.

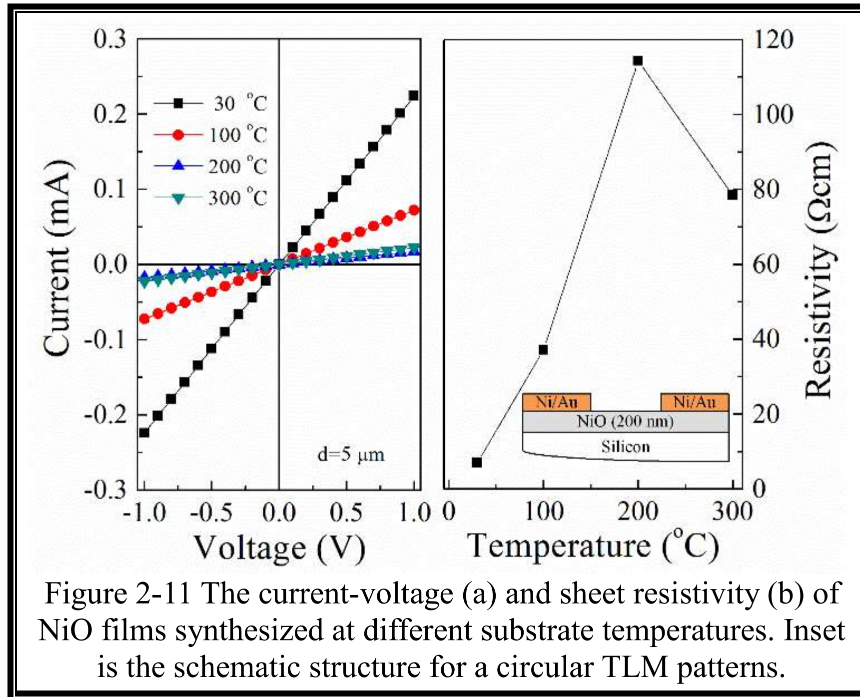

Figure 2-11 The current-voltage (a) and sheet resistivity (b) of NiO films synthesized at different substrate temperatures. Inset is the schematic structure for a circular TLM patterns.

§2.6. Conclusion

NiO films were deposited under different O_2/Ar ratios and substrate temperatures, which are face-centered cubic crystalline structure. The NiO films possess direct bandgaps of 3.6, 3.2, 2.7, and 3.0 eV at O partial pressures of 15%, 25%, 50%, and 65%, respectively. When the substrate temperature increased from 30 °C to 200 °C, the crystalline quality and stoichiometric of NiO film were improved, resulting in higher bandgap value and resistivity. While further increasing the substrate temperature to 300 °C, the decomposition of NiO will cause the appearance of Ni metal in the film.

Compared with the Ni/GaN Schottky diode, the turn-on voltage of the NiO/GaN heterojunction diode is relatively higher and shows a more smaller reverse leakage current. Combined the XRD and XPS results, the intensity ratio between Ni^{2+}/Ni^{3+} is enhanced with the increasing substrate temperature. The NiO film has a higher resistivity at higher substrate temperatures due to nickel vacancy density (hole concentration) decreased.

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Chapter 3 : Temperature–dependent electrical transport characteristics of a NiO/GaN heterojunction diode

§3.1. GaN-based heterojunction diode

Over the years, gallium nitride (GaN) material has attracted considerable attentions because of their superior properties, such as high breakdown voltage, high switching frequency, and good thermal stability [1, 2]. The realization of high conductivity p-type GaN epitaxial film is critical for the achievement of high performance GaN-based electronic devices and photodetectors [3-6]. For instance, p-type GaN cap layer has been proposed to deplete the 2DEG carriers in the AlGaN/GaN interface in order to achieve enhanced-mode heterostructure field-effect transistors (HFETs) [7]. Besides, high quality p-type GaN is also necessary for obtaining high efficiency GaN light-emitting diodes (LEDs) [8]. But, high resistivity and complex fabrication techniques of p-GaN retard the application of GaN [9]. On the other hand, nickel oxide (NiO) shows excellent chemical stability and behaves as a natural p-type semiconductor [10]. It has a closely matched lattice constant and bandgap energy with GaN, which makes p-NiO/n-GaN heterojunction to be a possible candidate for blue-UV LEDs and microwave power rectification. Furthermore, the natural p-type NiO can serve as guard ring structure to reduce the amount of field crowding at the main junction, which is regarded as an attractive method to obtain high breakdown voltage [11].

We previously fabricated NiO/GaN heterojunction diodes using magnetron reactive sputtering. Compared with Ni/GaN Schottky diodes, the heterojunction diode showed lower leakage current (approximately one order low) and kept good rectification property even worked at 175 °C. However, it mainly focuses on the optimization of deposit condition and thermal stability evaluation of the NiO/GaN heterojunction structure. In fact, the ideality factor of the NiO/GaN diodes are relatively high due to the interface states, which origin from dangling bonds, surface defect, ultrathin interfacial layer of defective native oxides and contamination. The rather imperfect interface between the NiO film and GaN substrate can cause the increase of leakage current and the decrease of breakdown voltage. Furthermore, the mechanism of the obtained temperature dependent

characteristics is not discussed in detail. A better understand of the electrical transport characteristics of the NiO/GaN heterojunction structure is necessary to improve the device characteristics.

Herein, the ohmic contact resistance and sheet resistance of Ni/Au/NiO film fabricated using magnetron reactive sputtering technique is obtained. The conduction and valence band offset for p-NiO/n-GaN heterojunction are also estimated from the schematic of energy band diagram. On the basis of the above results, the temperature dependent electrical transport behavior of NiO/GaN heterojunction structure is explored in detail to pave way for potential application in high-temperature and high-power environments.

§3.2. Fabrication of the NiO/GaN heterojunction diode

The commercial n-GaN wafers used in this experiment were grown on (0001) sapphire substrate by MOCVD. The vertical structure of wafer consists of a buffer layer (about 300 nm), a Si-doped (impurity density over 4×10^{18} cm^{-3}, 3.5 μm) GaN layer, and a Si-doped (3×10^{17} cm^{-3}, 0.4 μm) Schottky contact layer from bottom to top. We decided to use a circular-shaped Schottky pattern with a diameter of 166 μm to keep a uniform current between ohmic contact and Schottky contact. In order to simplify the process, the ohmic contact was placed on the same side of the Schottky contact with a distance of 15 μm.

Both of the ohmic contact and Schottky contact was formed by a standardized lift-off technology. The cathode ohmic contact was constituted utilizing a Ti/Al/Ti/Au (50/200/40/40 nm) multi-layer structure followed by annealing at 800 °C in N_2 atmosphere for 1 min. Before the Schottky deposition process, the samples were surface-cleaned by O_2 plasma ashing and then immersed in diluted HCl (HCl:H_2O=1:1) solution for 5 min to remove the possible oxide layer after lithography process. The NiO film was deposited by reactive sputtering (RF, 75 W) in Ar and O_2 (15:5 sccm) mixed ambient under a chamber pressure of 0.14 Pa, using a sputtering target of Ni. The anode Schottky electrode was formed using a NiO/Ni/Au (30/10/40 nm) stack film. As a comparison, the sample with Ni/Au (30/40 nm) electrode was also deposited by RF sputtering in Ar atmosphere under a sputtering power of 150 W and a chamber pressure of 0.14 Pa.

Ultimately, the sample was treated by post-annealing at 300 °C for 10 min. For a better evaluation of the effect of temperature, the current-voltage (I-V) characteristics of the sample were recorded at 25 °C, 75 °C, 125 °C, and 175 °C, respectively.

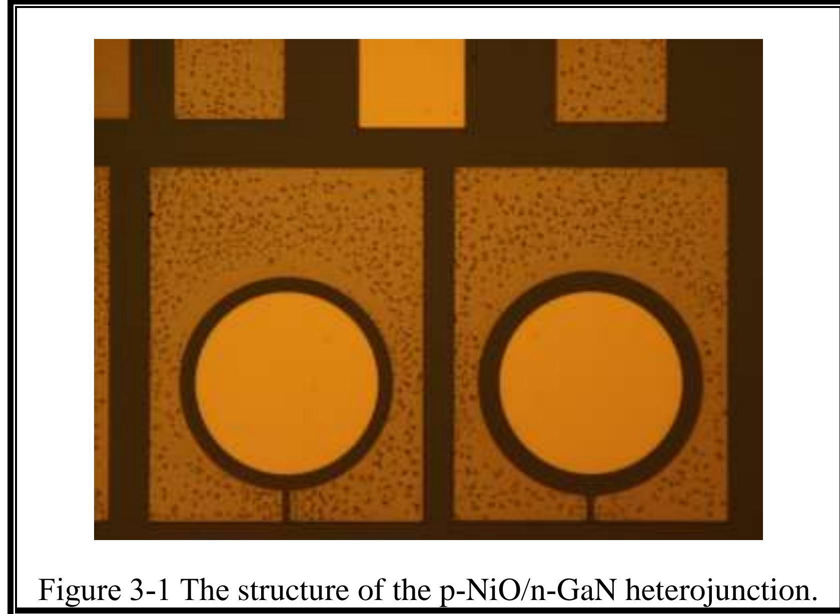

Figure 3-1 The structure of the p-NiO/n-GaN heterojunction.

§3.3. The characterization of a NiO/GaN heterojunction diode

Based on the results of UV-vis absorption spectrum and Hall measurement, the schematic of energy band diagram for a p-NiO/n-GaN heterojunction (inset of Figure 3-1) is depicted in Figure 3-1. The conduction band offset (ΔE_c) for the fabricated diode structure is:

$$\Delta E_c = \chi_{GaN} - \chi_{NiO} = 2.80 \text{ eV} \tag{3-1}$$

Where, χ is the electron affinity which is reported to be 4.2eV for GaN and 1.4eV for NiO. Using ΔE_c, the valence band offset (ΔE_v) is estimated as:

$$\Delta E_v = E_{gGaN} - E_{gNiO} + \Delta E_c = 3.0 \text{ eV} \tag{3-2}$$

Where, E_{gGaN} and E_{gNiO} are the band gaps of GaN (3.4 eV) and NiO thin films (3.2 eV), respectively. High band offset (barrier height) of NiO electrodes against GaN is beneficial to suppress leakage current and improve the reverse breakdown voltage (approximately 60 V for the NiO/GaN heterojunction).

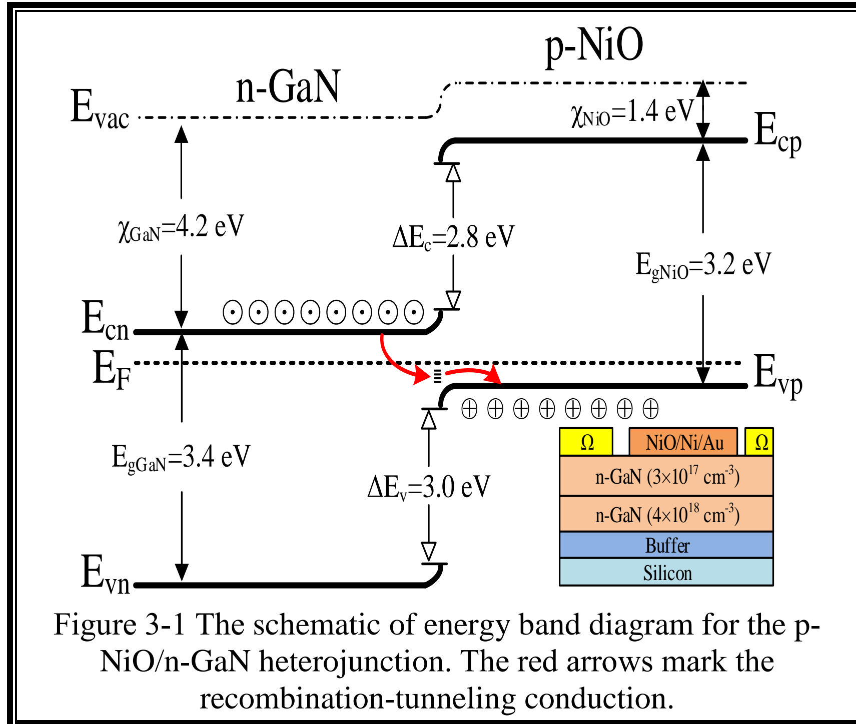

Figure 3-1 The schematic of energy band diagram for the p-NiO/n-GaN heterojunction. The red arrows mark the recombination-tunneling conduction.

The typical I-V characteristics of the NiO/GaN heterojunction at 25, 75, 125, and 175 °C are shown in Figure 3-2. The device showed typical rectification characteristics at all temperatures. The turn-on voltage at the room temperature, which is extracted by linear fitting the forward region, is about 2.24 V. It shifts to about 1.5V when the measurement temperature increased to 175 °C. Under forward bias, the energy band of GaN close to the GaN/NiO interface would upward bend, and the ΔE_c is enough to accumulate electrons at the GaN side. While the holes in the valence band of the NiO layer could be injected into the GaN side at a relatively low driving voltage. Therefore, the negative shift of turn-on voltages at higher temperature was mainly ascribed to the decrease in the barrier width due to the thermal diffusion of hole. Taking into account of temperature effect, the I-V characteristics of heterojunction are fitted by the following equation:

$$I=Is\,[exp(qV/nkT)-1] \quad (3\text{-}3)$$

where I_S is the reverse saturation current, V is the applied voltage, q is the electronic charge, k is the Boltzmann constant, T is the absolute temperature, and n is the ideality factor. The n values at different temperatures are obtained from the slope of the lnI-V plot (top inset of Figure 3-2). They are approximately 3.11, 3.04, 2.92 and 3.11 at 25, 75, 125,

and 175 ºC, respectively. In general, the n=1 is related to the characteristic of ideal p-n junction, while the higher (n>1) means the deviation from ideal p-n junction due to the presence of defect states in the NiO film. The decrease of n at higher temperatures results from the more carriers by thermally excited and the enhanced tunneling through the barrier and generation-recombination process occurring in the depletion region. Based on Eq.(3), we can obtain the I_s of the device from the intercept of $lnI–V$ curves. The Is are about 8.59×10^{-13}, 3.72×10^{-11}, 6.17×10^{-10} and 2.34×10^{-8} at 25, 75, 125, and 175 ºC, respectively. For a heterojunction, $ln(I_S/T)$ is expected to show a linear dependence on 1/T (bottom inset of Figure 3-2). Calculated from the slope of $ln(I_s)$ versus $1/kT$ plot, the activation energy (ΔE) is about 0.73eV for the NiO/GaN heterojunction.

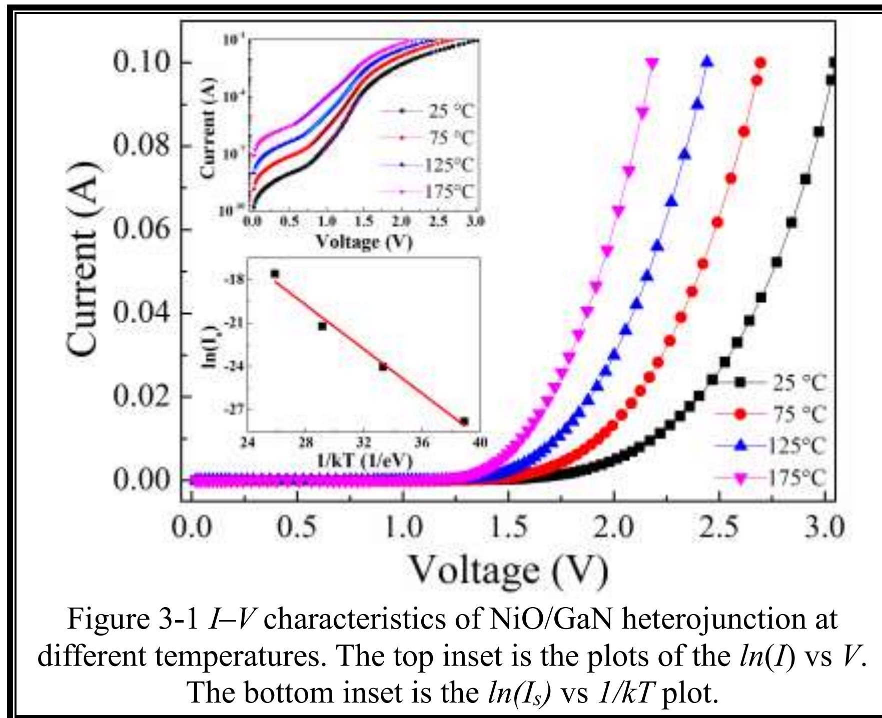

Figure 3-1 $I–V$ characteristics of NiO/GaN heterojunction at different temperatures. The top inset is the plots of the $ln(I)$ vs V. The bottom inset is the $ln(I_s)$ vs $1/kT$ plot.

Theoretically, the $lnI–V$ curve should be a straight line for the ideal NiO/GaN heterojunction. But three regions with obvious inflection points can be clearly observed in top inset of Figure 3-2, implying the existence of other mechanisms. In order to examine the conduction mechanism of p-n heterojunction at various temperatures, log-log plots of forward biased current-voltage characteristics were shown in Figure 3-3. The plots also exhibit three distinct regions depending on the applied bias voltage. By contrast, the two curvilinear regions in inset of Figure 3-2 became straight line. Therefore, other

than the exponent law, power laws are assumed to dominate these two regions. At all temperatures, the device current in low forward voltages (＜0.8V, region I) follows as power law of $I \sim V^{\alpha}$, where α are 1.31±0.04, 1.22±0.03, 1.15±0.03 and 1.07±0.02 at 25, 75, 125, and 175 ºC, respectively. Hence, the transport mechanism in the device is dominated by tunneling at region I. The exponents approach to 1 at higher temperatures because of higher density of free carrier can contribute to the conduction, resulting in the improvement of ohmic behavior. In region II (between 0.8 and 2V), it is dominated by an diffusion conduction mechanism of $I \sim exp(\beta V)$. The fitted constant β are 5.51±0.08, 4.74±0.06, 4.29±0.04 and 3.56±0.02V-1 at 25, 75, 125, and 175 ºC, respectively, which are larger than that for an ideal vacuum diode (1.5). This deviation occurs due to the electrons tunneling from the conduction band of GaN into the recombination centers provided by the interface states and subsequently recombining with holes in the valence band of NiO. Therefore, the decrease of β means that the recombination-tunneling current transport was suppressed at a relatively higher temperature, implying the diode at high temperature become more close to diffusion conduction as the ideal vacuum diode. At higher voltages (>2 V, region III), the current behaves as power law of $I \sim V^{m}$, where m ($=Tc/T+1$) is the exponent parameter, Tc is a characteristic temperature constant of the trap distribution. It can be fitted into $I \sim V^{6.85\pm0.07}$, $I \sim V^{6.67\pm0.05}$, $I \sim V^{6.36\pm0.04}$, and $I \sim V^{6.13\pm0.09}$ at 25, 75, 125, and 175 ºC, respectively. The decrease of value m with increasing temperature is expected for space-charge-limited current (SCLC) conduction observed in wide band gap semiconductors. However, the value of m are larger than 2 implying that the dominant conduction mechanism in this region is trap charge limited SCLC with an exponent distribution of traps. The decrease of m value with increasing temperature means the effect of trap became weak and tended to being a trap-free SCLC conduction. The plot of (m-1) versus 1000/T can be fitted into a straight line and the Tc obtained from the slope of the straight line is about 648 K. The corresponding characteristic trap energy E_t according to the relation of $E_t=kTc$ is found to be 55.9meV. For a comparison, the log-log current-voltage plot of the Ni/GaN Schottky diode only shows two regions. The current in low forward voltages (＜0.5V, region *I*) is dominated by tunneling, and in region II (between 0.5 and 1V), it follows an exponential relation of $I \sim exp(\beta V)$ due to the recombination-tunneling mechanism.

The breakdown voltage (VBK) of Ni and NiO diodes on 1μm thick drift layer with an impurity density of about $10^{17}cm^{-3}$ are about 92 and 57V, respectively. The decreases of breakdown voltage attribute to the rather imperfect interface between the NiO and GaN.

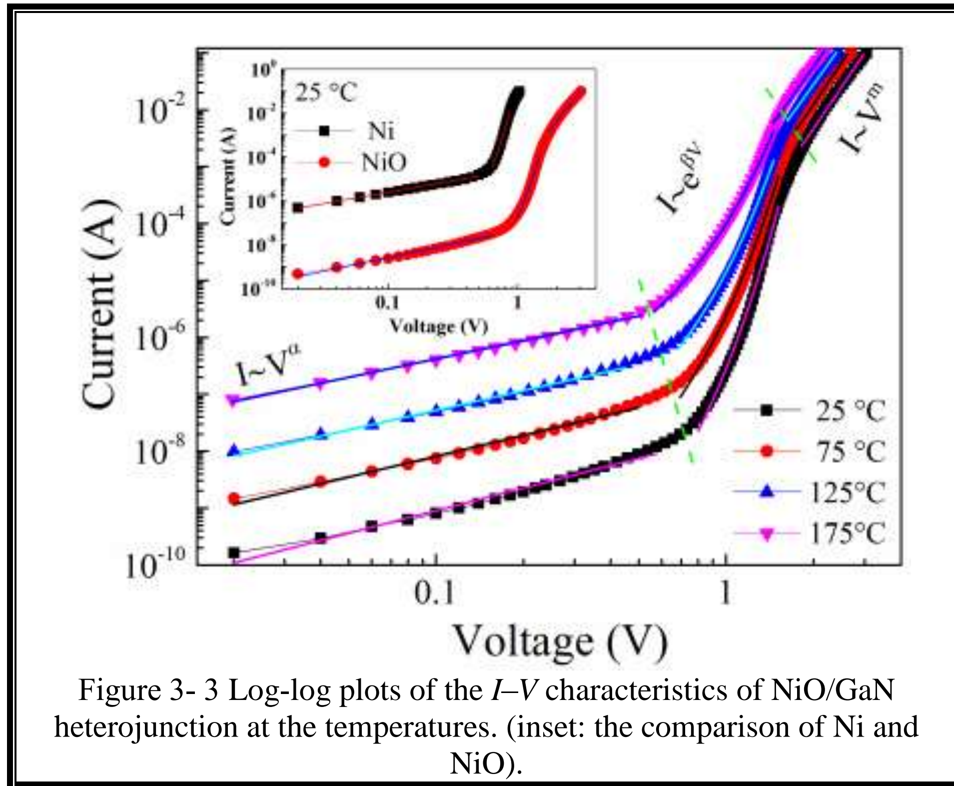

Figure 3- 3 Log-log plots of the *I–V* characteristics of NiO/GaN heterojunction at the temperatures. (inset: the comparison of Ni and NiO).

§3.4. Conclusion

In conclusion, we have investigated the electrical properties of the NiO/GaN heterojunction device in the temperature range 25-175 ºC. The as-grown NiO exhibited cubic crystalline structure with a bandgap of 3.2 eV. The NiO/GaN diode exhibited a temperature-dependent turn-on voltage. Compared with the Ni/GaN Schottky diode, the turn-on voltage of the NiO/GaN heterojunction diode is relatively higher and shows a more obvious negative shift with increasing temperature. The three types of current transport mechanism are found to be strongly related to the applied bias voltages and temperatures. On the other hand, the device exhibited considerably a stable behavior over the temperature range of 25-175 °C and will be favorable for wildly applying in high-temperature and high-power environments.

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Chapter 4：Normally-off AlGaN/GaN HFETs with NiO gate

§4.1. Normally-off (or E-mode) AlGaN/GaN HFETs

The AlGaN/GaN HFETs are generally normally-on devices with negative threshold voltage which need extra gate voltage to turn off the channel. Therefore, it must have a more complicate circuit design and high consumption. Normally-off AlGaN/GaN HFETs are preferable for power switching applications because they meet the requirement of a safe operation, low consumption and a simple gate drive configuration [1]. The strong piezoelectric polarization effect in the AlGaN/GaN structure can induce high density, high electron mobility and high saturation velocity [2]. This high density 2DEG is difficult to be depleted by the zero-biased Schottky gate voltage, which resulting in typical normally-on operation. Many methods have been developed to partially or completely deplete the 2DEG channel in order to realize normally-off HFETs, such as recessed-gate structure, fluorine processing, thin AlGaN barrier, p-type gate, and so on [3-6]. Among the above methods, the p-type gate device is a promising candidate owing to the characteristics of high mobility and the considerable threshold value.

The p-GaN (or p-AlGaN) layer under the gate contact region lifts up the band diagram, resulting in the depletion of the 2DEG channel [7]. Based on this technique, the only commercially available "real" normally-off HFETs to date are achieved. However, one of the challenges for this processing is the selective removal of the p-GaN layer in access region by plasma etch, since it is rather difficult to avoid under-etching or over-etching [8]. Furthermore, the plasma-induced damage of the AlGaN surface can lead to a degradation of the properties of device. For this reason, the scientific community explores some new approaches, such as the selective epitaxial growth of p-GaN in localized regions [9] or the hydrogen surface treatment to passivate the Mg-acceptors in the access region [10].

As another interesting approach, p-type semiconductor materials (NiO, Cu_2O, etc.) that can be synthesized in localized regions at low temperature are attracting many attentions [11-12]. Many works also suggest that the preferred orientation and crystalline quality of NiO film show a relationship with the substrate temperature [13]. In this chapper,

AlGaN/GaN HFETs with NiO gate electrode (synthesized at 30 °C) are fabricated, showing positively threshold voltage shift compared with Ni/Au gate. The mechanism of the threshold voltage tuning is also investigated.

§4.2. The fabrication of NiO-gated AlGaN/GaN HFETs

For device fabrication, AlGaN/GaN HFETs grown by MOCVD on a sapphire substrate were used in this experiment. In the HFETs fabrication process, firstly, an etching depth of 100 nm was made by inductively coupled plasma (ICP) to obtain MESA isolation. The ohmic contact metals were then constituted by a Ti/Al/Ti/Au (50/200/40/40 nm) multi-layer structure followed with annealing at 900 °C in N_2 atmosphere for 80 s. After lithography of gate pattern, the samples were subjected to O_2 plasma ashing to make the surface clean, and in order to remove the native oxide layer, immersed into diluted HCl ($HCl:H_2O=1:1$) for over 5min. A NiO gate electrode of about 100 nm was deposited at the substrate temperature of 30 °C. Then, a cap layer of Ni/Au (70/30 nm) was deposited on the NiO layer in Ar ambient to reduce the gate resistance (as shown in Figure 4-1). The electrical properties of the devices were evaluated systemically.

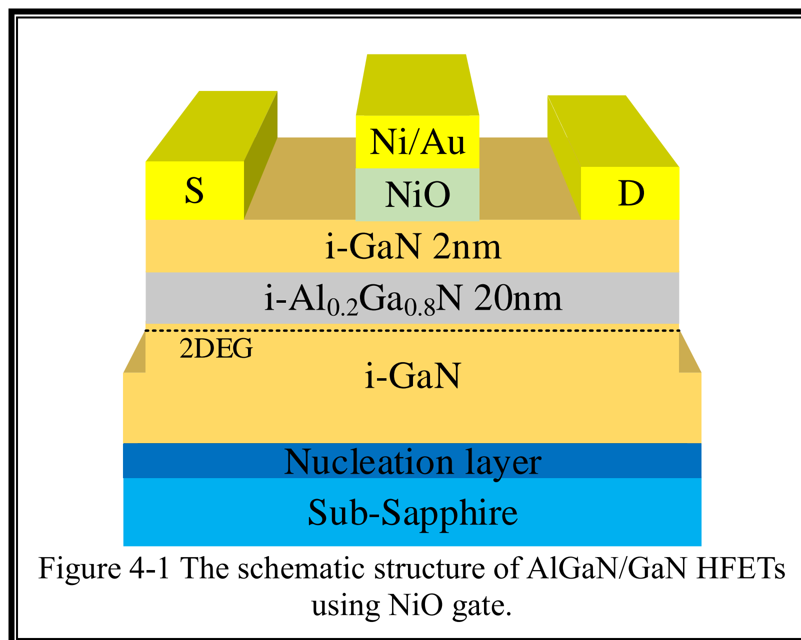

Figure 4-1 The schematic structure of AlGaN/GaN HFETs using NiO gate.

§4.3. The characteristics of NiO-gated AlGaN/GaN HFETs

The NiO film deposited under 30 °C has the smallest resistivity and enough bandgap is regarded as a suitable gate electrode for the HFETs application. Compared with the Ni/Au-gated device, the threshold voltage of the NiO-gated device shifts positively from approximately -3.6 to -2.8V, as shown in the transfer characteristics (Figure 4-3 a). Similar with the common p-GaN gated normally-off device, the p-type conductivity as well as the conduction band offset between NiO and GaN can effectively lift up the potential, which leads to depletion of the two-dimensional electron gas (2DEG) and positive shift of the threshold voltage. Besides, the existence of depletion layer can decrease the tunneling of electron and leakage current (not shown). The corresponding output characteristic shows that the NiO-gated HFETs operate very well (Figure 4-3 b). However, the NiO-gated HFETs show a relatively lower output drain current which may be mainly attributed to the higher threshold voltage. Figure 4-2 shows the actual test device.

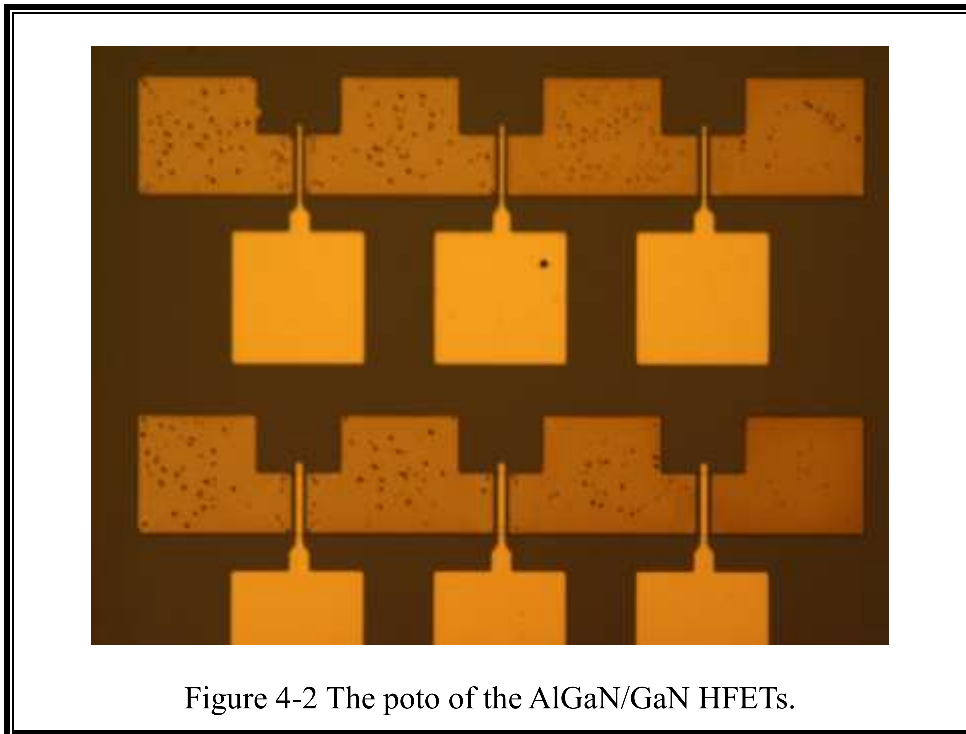

Figure 4-2 The poto of the AlGaN/GaN HFETs.

The corresponding gate leakage characteristic of the square-type device is shown in Figure 4-4. Both reverse leakage current and forward current decrease with introducing

of NiO. As compared with the HFETs, the reverse leakage current of the NiO is approximately 1.5 order lower due to the decrease of defect density for assisting the carrier tunneling.

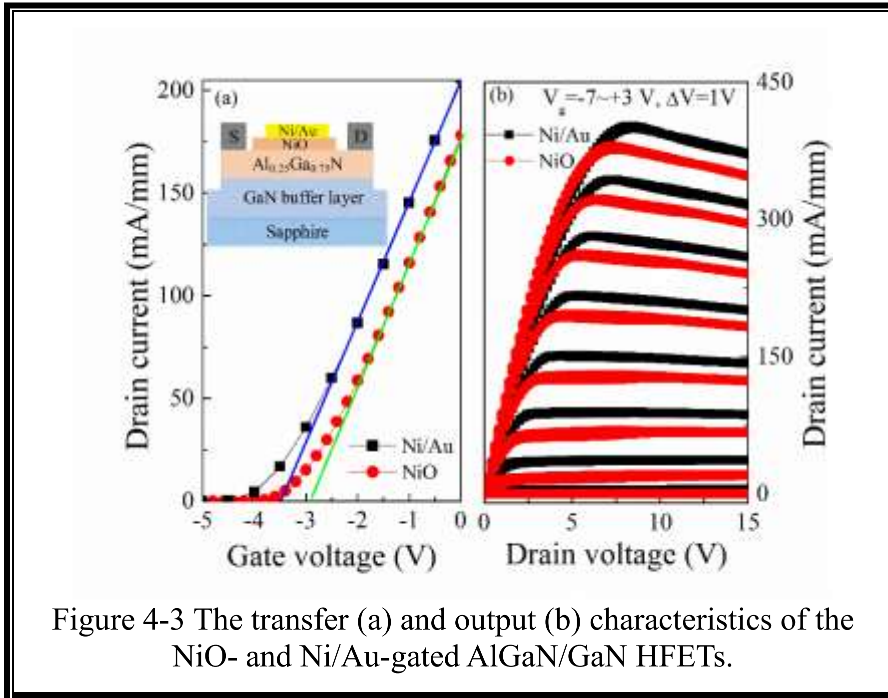

Figure 4-3 The transfer (a) and output (b) characteristics of the NiO- and Ni/Au-gated AlGaN/GaN HFETs.

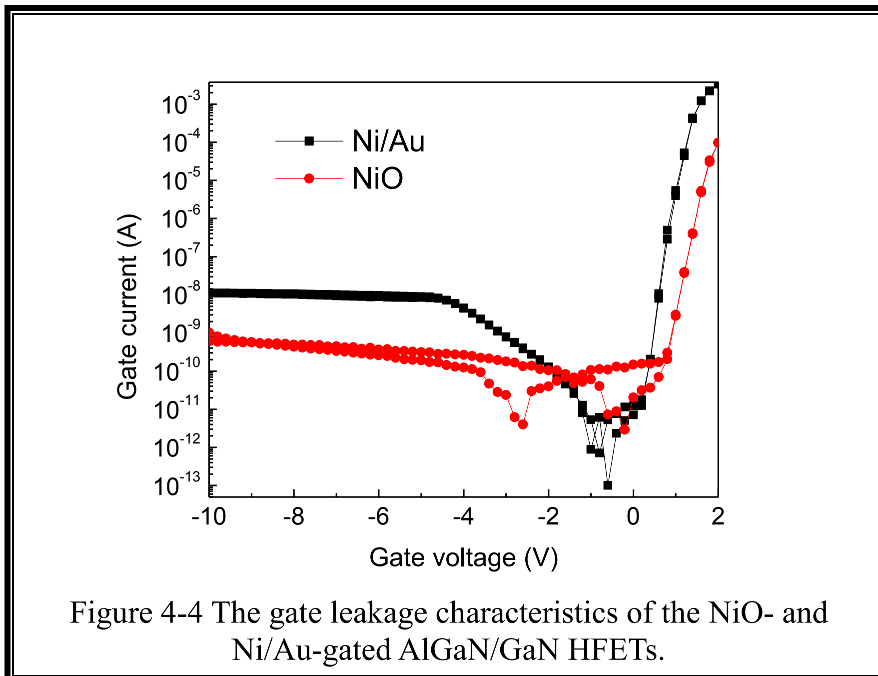

Figure 4-4 The gate leakage characteristics of the NiO- and Ni/Au-gated AlGaN/GaN HFETs.

In order to obtain the band offset at the NiO / GaN interface, we prepared three samples, where GaN on sapphire substrate (Figure 4-5 a) with a buffer layer, a heavily

doped GaN channel layer ($10^{18}/cm^3$) and a lightly doped GaN layer ($10^{15}/cm^3$) was grown by MOCVD. To remove the dirty of surface and the native surface oxide layer the GaN samples were dipped into H_2SO_4:H_2O_2 (4:1) solutions for 10 min first and then into diluted HCl (HCl:H_2O=1:1) for over 5 min. To measure the band offsets, 5 nm (sample b) and 100 nm (sample c) NiO fims were deposited on GaN surface by magnetron sputtering.

The band offset comes from the band structure difference of the semiconductor material, which forms the heterojunction. Under the assumption that with or without the over-layer deposition, it is intact for the energy difference between the valence band edge and core level peak of the substrate, XPS is well employed to determine the band offset at the heterojunction interface [14, 15]. Although the valance band offset at the two material interfaces can be calculated from the difference between VBMs, there is an error due to the lack of consideration of the usual interface dipoles [16].

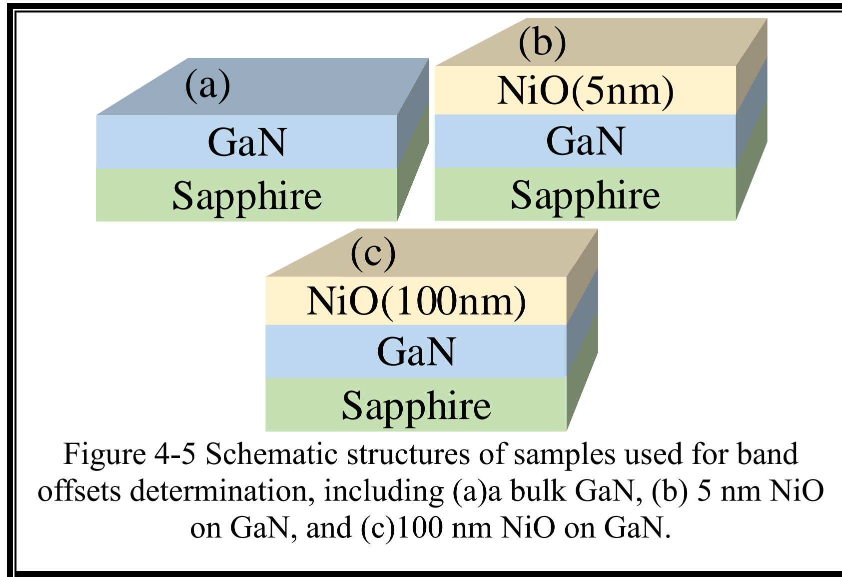

Figure 4-5 Schematic structures of samples used for band offsets determination, including (a)a bulk GaN, (b) 5 nm NiO on GaN, and (c)100 nm NiO on GaN.

The band offsets at the NiO/GaN interface can be measured by XPS employing a well-known Kraut's method [17, 18]. This method can be depicted as the following equation:

$$\Delta E_V = \left(E_{Ni2p}^{NiO} - E_{VBM}^{NiO}\right) - \left(E_{Ga3d}^{GaN} - E_{VBM}^{GaN}\right) - \Delta E_{CL} \quad (4\text{-}1)$$

where $\left(E_{Ni2p}^{NiO} - E_{VBM}^{NiO}\right)$ is the energy difference between Ni2p and valence band maximum (VBM) of the bulk NiO material, $\left(E_{Ga3d}^{GaN} - E_{VBM}^{GaN}\right)$ is the energy difference

between Ga3d and VBM of the bulk GaN material, $\Delta E_{CL} = (E_{Ni2p}^{NiO} - E_{Ga3d}^{GaN})$ is the energy difference between Ni2p and Ga3d core levels in the NiO/GaN heterojunction. Then, the conduction band offset (CBO, ΔE_c) of NiO/GaN heterojunction can be estimated by:

$$\Delta E_c = \Delta E_V + E_g^{NiO} - E_g^{GaN}. \quad (4\text{-}2)$$

Where E_g^{NiO} and E_g^{GaN} are the band gap for NiO and GaN, respectively.

The energy of the core level (CL) and the VBM for the NiO are shown in Figure 4-6. The CL spectrum of Ni $2p^{3/2}$ consists of three components located at 855.12, 857.11, and 862.14 eV, which are attributed to the Ni^{2+}, Ni^{3+}, and satellite bonds. It is worth noting that the peak location shows slight difference compared with the data shown above, which may be ascribed to the discrepancy between different apparatus. The VBM value determined from the linear extrapolation of leading edge of the valence band is 1.34 eV. The energy difference between Ni2p core level and VBM is then calculated to be 853.78 eV.

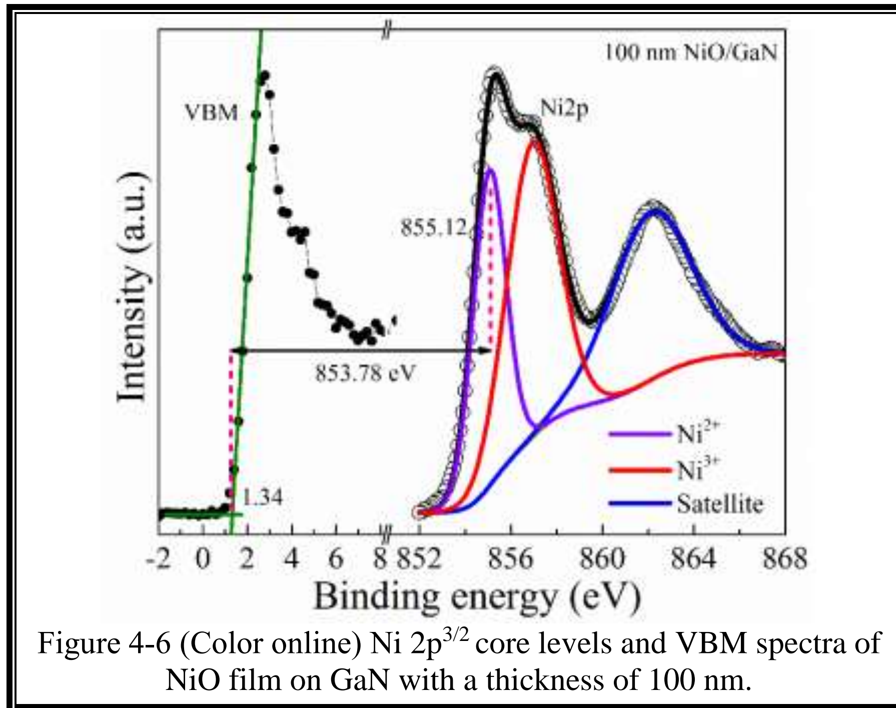

Figure 4-6 (Color online) Ni $2p^{3/2}$ core levels and VBM spectra of NiO film on GaN with a thickness of 100 nm.

The CL spectrum of Ga3d as well as the VBM for GaN material is shown Figure 4-7. Three peaks can be observed, including N2s (at around 17.48 eV), Ga-N (at around 20.96

eV) and Ga-O (at around 21.92 eV) bonding. Combining the VBM value of approximately 3.82 eV, the energy difference between Ga3d core level and VBM is then determined to be 17.14 eV. Furthermore, The CL energy difference between Ga3d and Ni2p is deduced on the sample with a thin layer of NiO (approximately 5 nm) deposited on GaN, as shown in Figure 4-8. The Ga 3d peak presents obvious change, which is dominated by the native Ga-O at 22.51 eV and O2s contribution from NiO at 26.32 eV. This observation indicates that the thickness of the NiO layer is slightly thick for XPS measurement [19]. The CL energy positions of Ga3d and Ni2p are fitted to approximately 20.22 eV for Ga-N and approximately 855.61 eV for Ni^{2+}, respectively. Therefore, the corresponding energy difference can be calculated as 835.39 eV.

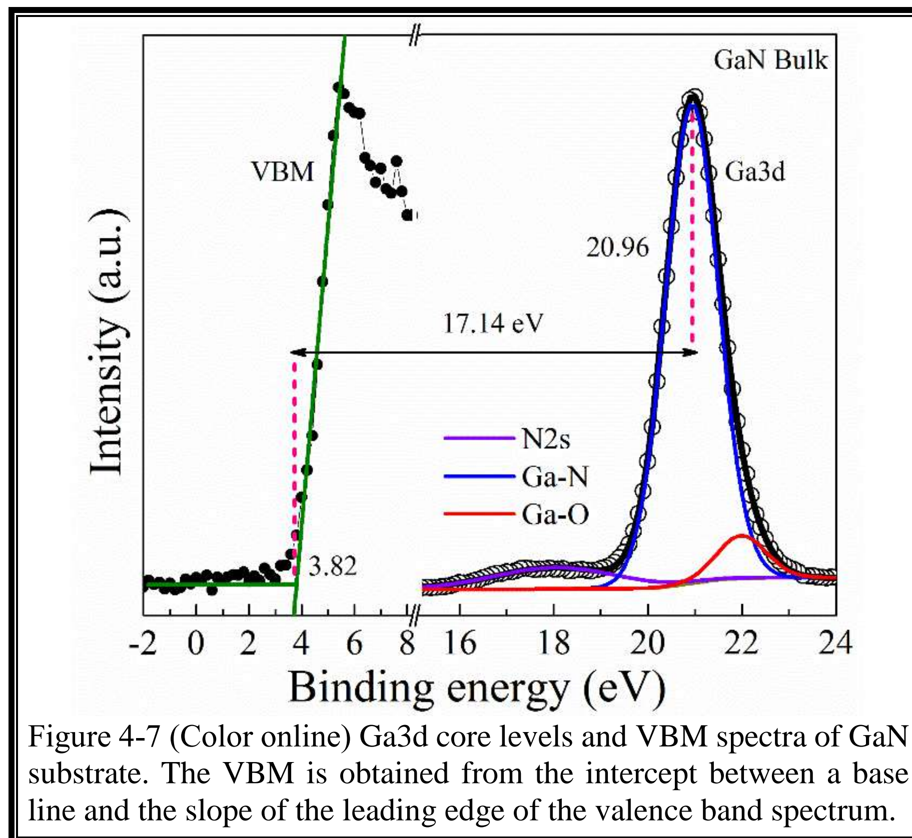

Figure 4-7 (Color online) Ga3d core levels and VBM spectra of GaN substrate. The VBM is obtained from the intercept between a base line and the slope of the leading edge of the valence band spectrum.

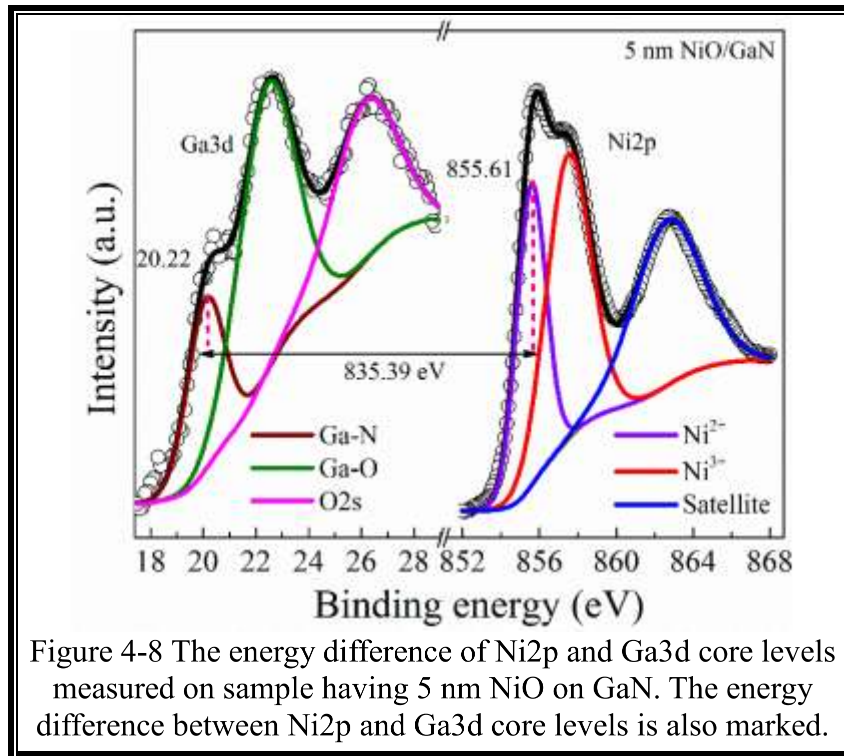

Figure 4-8 The energy difference of Ni2p and Ga3d core levels measured on sample having 5 nm NiO on GaN. The energy difference between Ni2p and Ga3d core levels is also marked.

The peak positions of VBMs and core levels are shown in Table 1. Based on those data, the valence band offset is calculated to be 1.25 eV and the corresponding conduction band offset can be estimated as 1.42 eV using a band gap of 3.57 eV for the NiO film deposited at 30 °C. Figure 4-9 shows the schematic diagram of the band alignment.

		GaN bulk	NiO (5 nm)	NiO (100nm)
Ga3d	Ga-N	20.96 eV	20.22 eV	855.12 eV
VBM	--	3.82 eV	--	1.34 eV
Ni2p	Ni-O	--	855.61 eV	--

Table 1 The peak positions of VBMs and core levels used to calculate the VBO of NiO/GaN heterojunction.

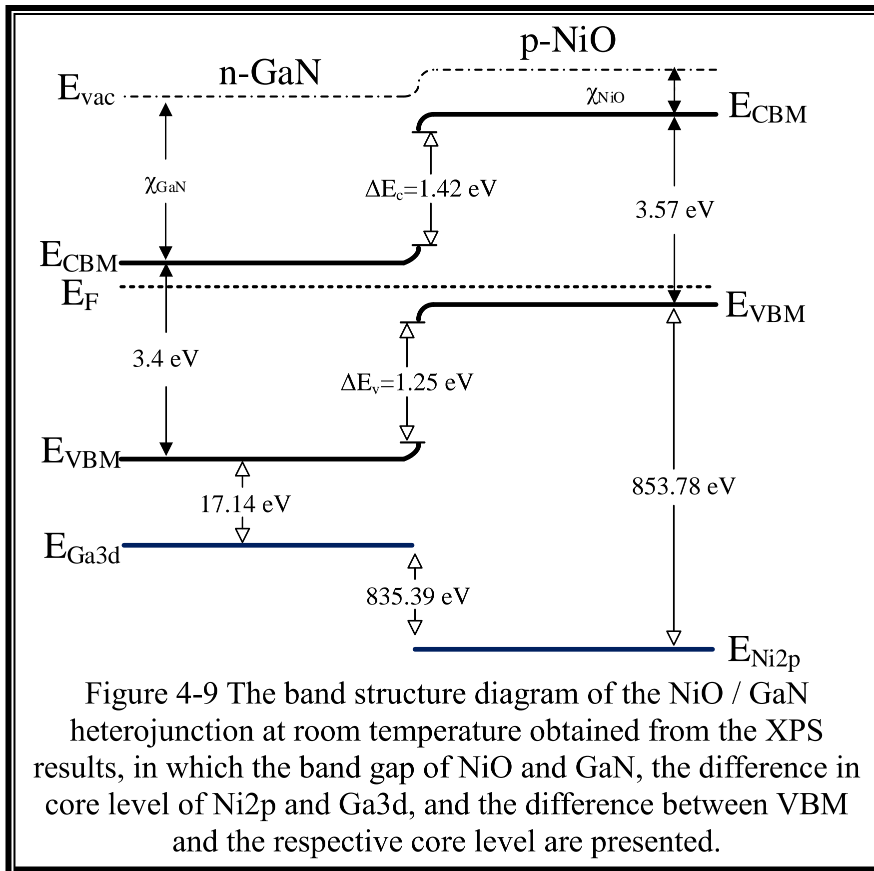

Figure 4-9 The band structure diagram of the NiO / GaN heterojunction at room temperature obtained from the XPS results, in which the band gap of NiO and GaN, the difference in core level of Ni2p and Ga3d, and the difference between VBM and the respective core level are presented.

§4.4. The fabrication of NiO-gated normally-off AlGaN/GaN HFETs

The AlGaN/GaN HFETs wafer used here were grown by MOCVD on Si substrate. For the MESA isolation, the AlGaN/GaN HFETs wafer was etched by ICP with an etching depth of 100 nm. After cleaning by remover, acetone and methyl alcohol, gate area was recessed (the residual barrier thickness was approximately 8 nm) using $SiCl_4$-based dry etching, with the ICP/bias power is of 100 W/20 W. The Ti/Al/Ti/Au (50/200/40/40 nm) stack was evaporated for forming the ohmic contact metals and was annealed at 900 °C for 80 s in an N_2 ambient environment. Before sputtering, the samples were immersed in diluted HCl ($HCl:H_2O$=1:1) for about 5min to remove the native oxide layer. At the substrate temperature of 30°C, a NiO gate electrode of about 100 nm was deposited and then Ni/Au (70/30 nm) was deposited on the NiO layer in Ar ambient to reduce the gate resistance (as shown in Figure 4-10 a). As comparison, a Ni/Au (about 100 nm) gated AlGaN/GaN HFET with recess structure was deposited (as shown in Figure 4-10 b). Figure 4-11 shows the whole device fabrication.

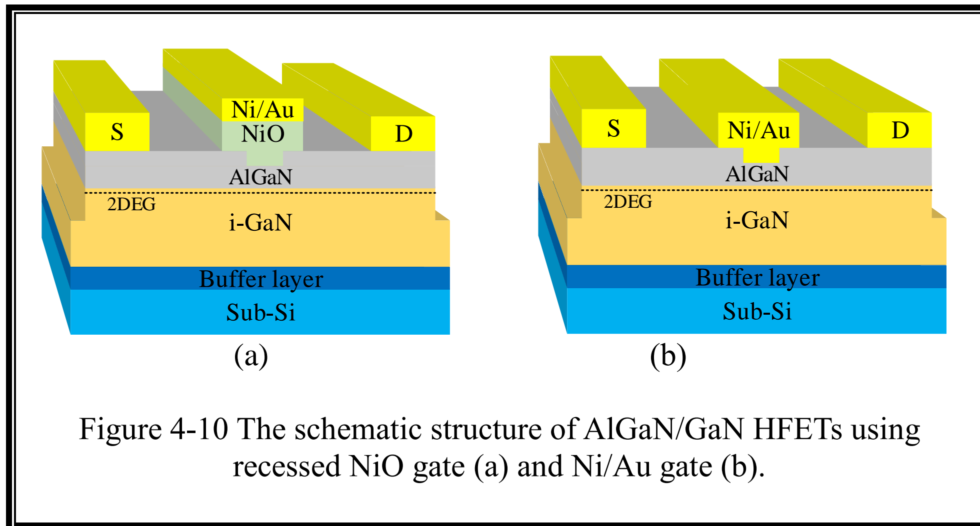

Figure 4-10 The schematic structure of AlGaN/GaN HFETs using recessed NiO gate (a) and Ni/Au gate (b).

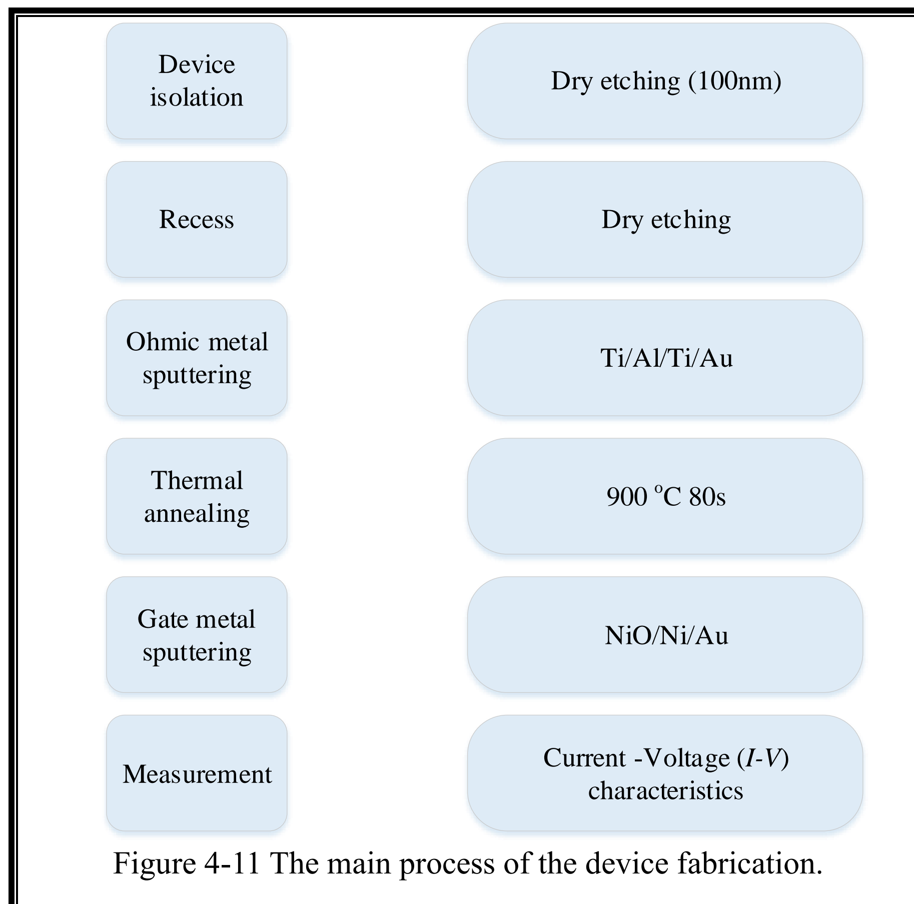

Figure 4-11 The main process of the device fabrication.

§4.5. The characteristics of NiO-gated normally-off AlGaN/GaN HFETs

The output curves of recessed-gate devices with Ni and NiO as gate electrode are shown in Figure 4-12. Both the Ni- and NiO-gated HFETs can operate well with the swept gate voltage from -7 to 3 V. The maximum drain current density of NiO-gated HFET is smaller than that of Ni-gated one, which is consistent with the transfer curve. With recessing, the maximum drain current density of NiO-gated HFETs decreases due to the increase of the resistivity.

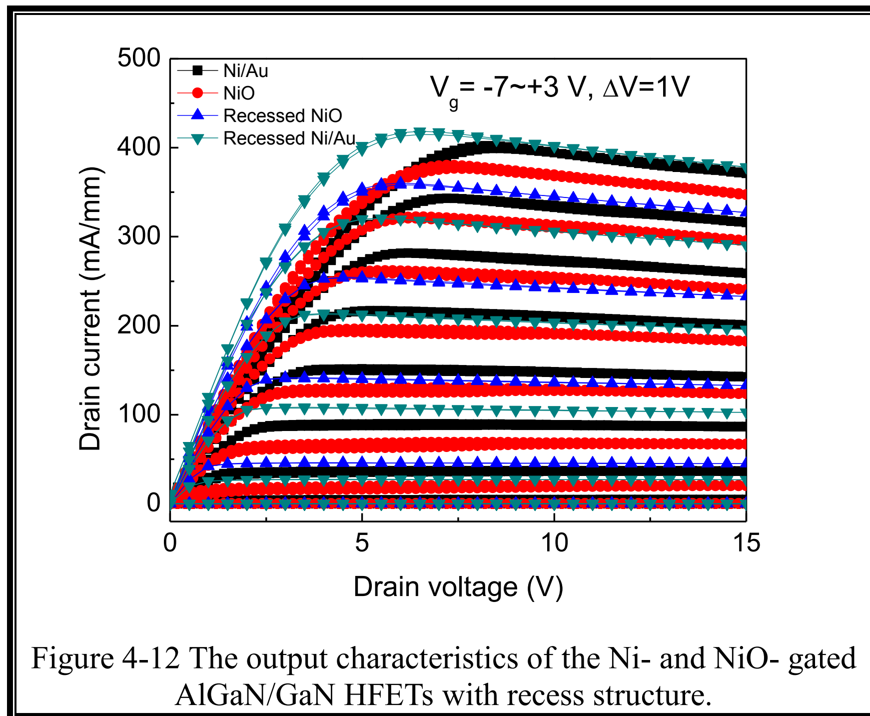

Figure 4-12 The output characteristics of the Ni- and NiO- gated AlGaN/GaN HFETs with recess structure.

Figure 4-13 shows a schematic diagram of the rectangular TLM test structure. TLM is a commonly used method of evaluating electrical characteristics and the quality of ohmic contact.

The rectangular TLM test patterns were fabricated in the mesa-isolated area for obtaining an accuracy measurement. It consists of rectangular metal contact pads (the length L= 100 μm and width W=150 μm) with spacing between them are d=5, 10, 15, 20, 25μm, respectively. The mesa structure can eliminate the lateral current flows from one contact to the other contact, and limits the current flow direction which perpendicular to

the edge of the metal contacts within a mesa. The total resistance between two neighbouring pads separated by a distance d is measured by the four point probe method and is estimated with the following equation：

$$R = \frac{\rho_s d}{W} + \frac{2R_C}{W} \tag{4-3}$$

Where ρ_s is the sheet resistance which between the two pads, R_C is the ohmic contact resistance between the metal and semiconductor material. All the voltages in the horizontal direction drop because of ρ_s. While the voltage drop in the vertical direction perpendicular to the current plane is due to *Rc*. By plotting *R* as a function of *d*, the data can be linearly fitted and the ρ_s and *Rc* can be calculated from the slope and intercept.

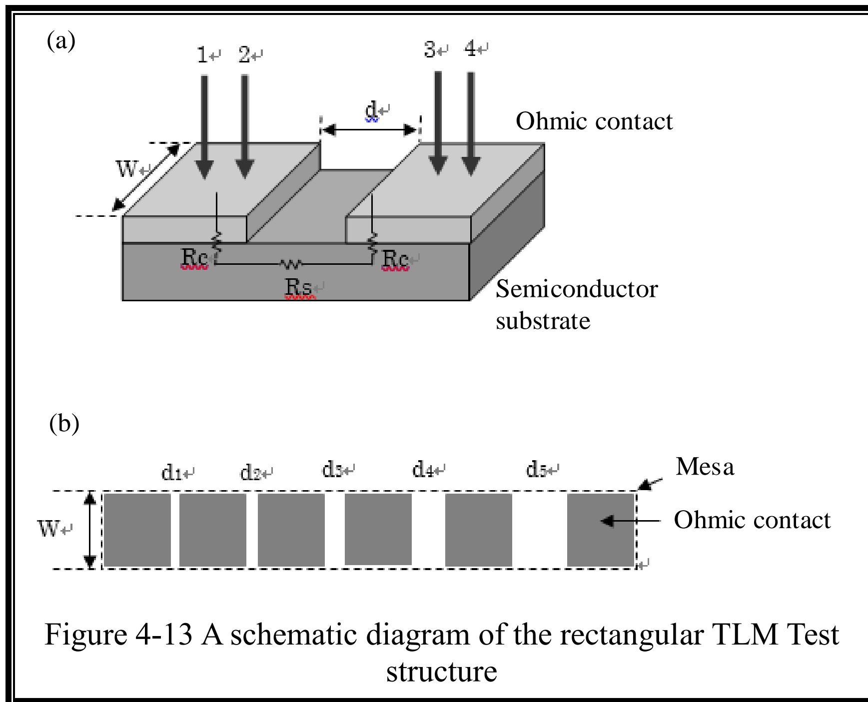

Figure 4-13 A schematic diagram of the rectangular TLM Test structure

We use a square TLM pattern for the samples to calculate the contact resistance and sheet resistance before and after recessing. The contact resistance is 1.43 Ωmm with the sheet resistance of 415.26 Ω/□ for the NiO- gated devices, respectively.

Figure 4-14 shows the transfer (a) and transconductance (b) characteristics of the HFETs with Ni and NiO gate electrodes. The conventional Ni-gated HFETs showed a threshold voltage of approximately -3.6 V at Vg=10 V (Figure 4-14 (a)). While for NiO-

gated HFETs, the threshold voltage positively shifts to approximately -4 V. The threshold voltage has a positive shift due to the p-type conductivity as well as the conduction band offset between NiO and GaN, which can effectively lift up the potential to result in depletion of the 2DEG. However, the relatively higher threshold voltage as well as the slight decrease of transconductance (Figure 4-14 (b)) of the NiO gate result in smaller drain current density. After recess, the threshold voltage for the Ni- and NiO-gated HFETs positively shifted to approximately 2.5 V and 3V, respectively. The threshold voltage of the recessed NiO-gate HFETs is close to about 0 V. So far, the threshold of NiO- gated HFET can not reach above 0V. The possible reason is that the ICP etching rate is uncertain and the depth of etching is relatively shallow, resulting in poor control of the depth of trenching.

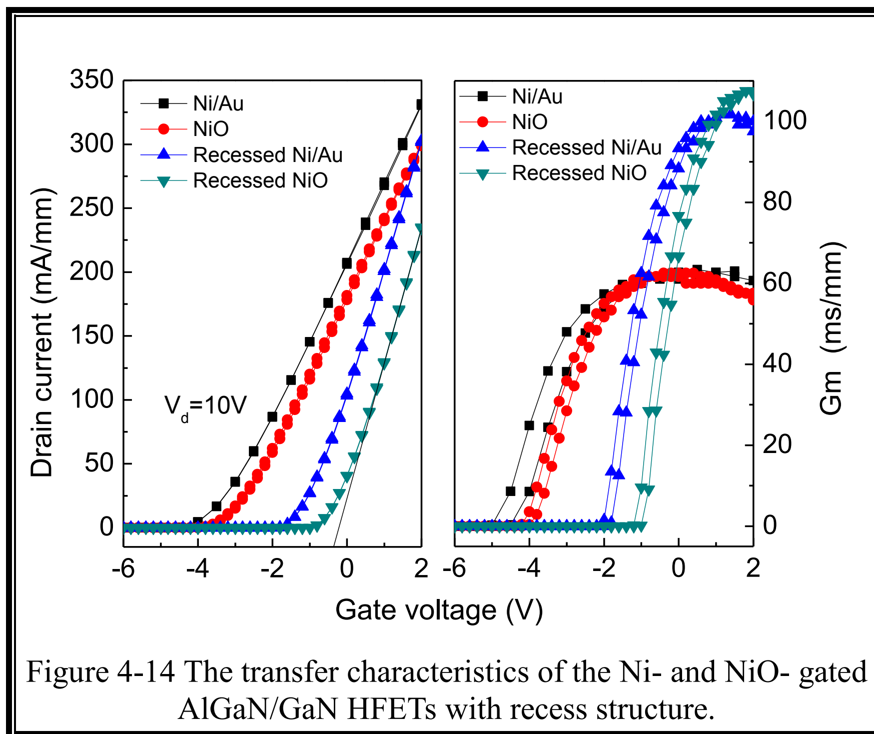

Figure 4-14 The transfer characteristics of the Ni- and NiO- gated AlGaN/GaN HFETs with recess structure.

Figure 4-15 shows the gate leakage characteristics of the Ni- and NiO-gated AlGaN/GaN HFETs with recess structure. The gate leakage current of NiO-gated AlGaN/GaN HFETs decreases nearly one order of magnitude in reverse bias and approximately three orders of magnitude in forward comparing with Ni-gated AlGaN/GaN HFETs. It indicates that the existence of depletion layer can decrease the

tunneling of electron and leakage current for p-type gate electrode. For the Ni- gated HFETs, the reverse leakage is almost no obvious changes with larger value and the forward current is slightly decrease after recessing. While for the NiO-gated HFETs, both the reverse leakage current and the forward current have a slight reduce after recessing. It suggests that the recessing has a slight effect on reducing leakage current.

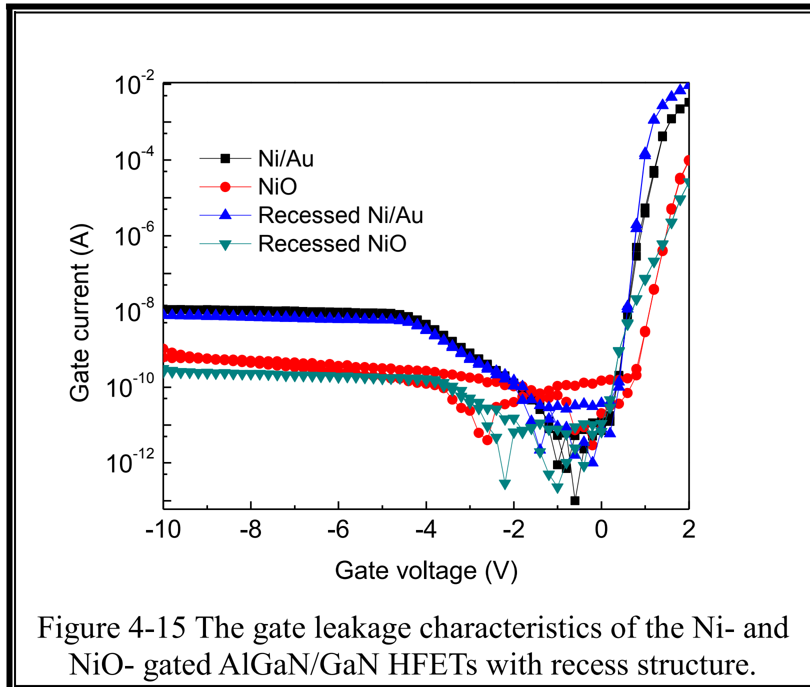

Figure 4-15 The gate leakage characteristics of the Ni- and NiO- gated AlGaN/GaN HFETs with recess structure.

§4.6. Conclusion

Combining the material and electric results, the NiO film under 30 °C with lowest resistivity is used as the gate electrode for HFETs application. Compared with the Ni/Au-gated device, the threshold voltage of the NiO-gated device shifts positively from approximately -3.6 to -2.8 V because of the p-type conductivity as well as the conduction band offsets between NiO and GaN. The band offset at the heterojunction interface can be measured by XPS employing a well-known Kraut's method. The corresponding valence and conduction band offset is calculated to be 1.25 and 1.42 eV using a band gap of 3.57 eV for the NiO film.

After recess, the threshold voltage for the Ni- and NiO-gated HFETs has a positive shift with the smaller drain current density. With the recessed-gate structure, normally-off GaN

HFETs can be obtained with a threshold voltage of closing to 0 V. Meanwhile, the existence of p-type NiO gate layer can decrease the tunneling of electron and leakage current.

§4.7. Reference

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Chapter 5：Metal-oxide-semiconductor AlGaN/GaN HFETs using TiN/HfO_xN_y stack gate layer

§5.1. Selection of material

Another way for reducing the leakage current is to use a gate with MIS structure. The insulator is generally oxide. Since the successful of MOSFET, it has been rapid development and become the most important devices of the advanced integrated circuits, such as the microprocessor and memory, etc. It dominates the development of integrated circuits and microchip fate due to the MOSFET can easily reduce the device size, and occupy a smaller space than the bipolar transistor in the same design specifications. Therefore, the greatest benefit of developing the complementary metal-oxide-semiconductor transistor (CMOS) planar technology is that it is suitable for mass production to result in the low cost [1-5]. Most of the commercial digital processing units currently use the CMOS technology. With the advance of the CMOS technology, the applications of the CMOS technology have been extended from digital circuits to analog/mixed-signal and radio frequency (RF) circuits, and has an significant role in the field of high-speed analog circuits dominated traditionally by bipolar, GaAs and SiGe devices [6-8].

The shrinkage of the device gate-length size in integrated circuits since 1970 is shown in Figure 5-1 [9]. The dimension has been steadily decreasing by more than three orders of magnitude and will continue to reduce in the future. The driving force behind shrinking device dimensions is the need for circuit performance and integration level. The number of components on each integrated circuit chip has been increasing exponentially. It is expected to slow down for the growth rate due to increasing technical difficulty and manufacturing cost.

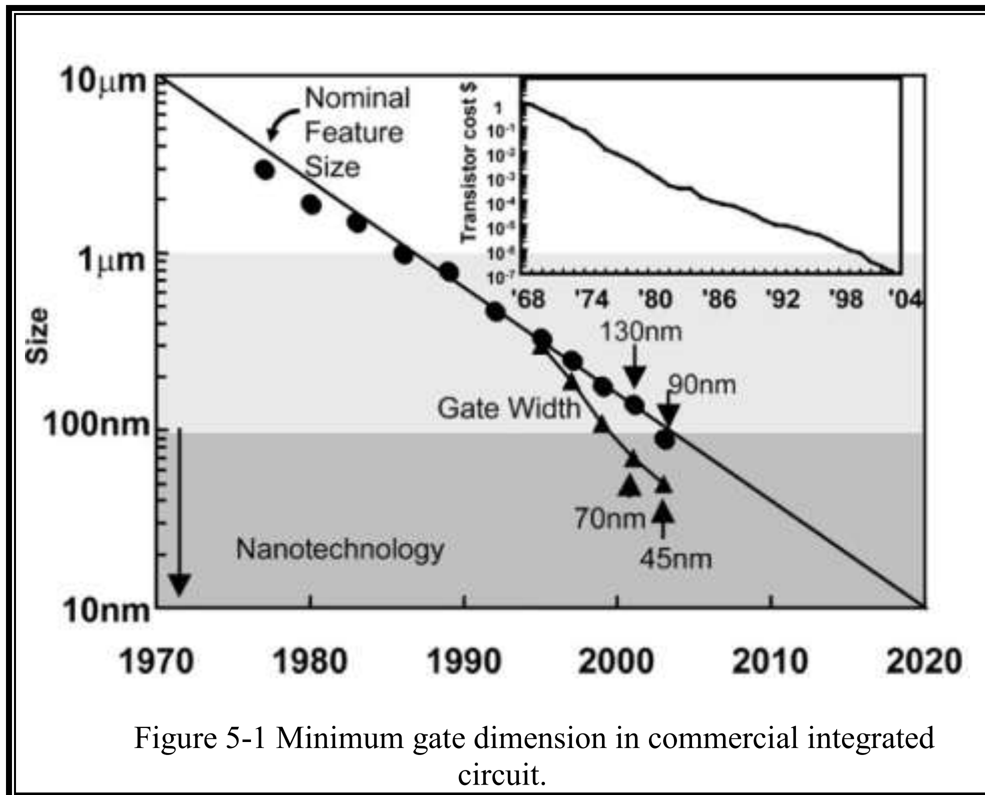

Figure 5-1 Minimum gate dimension in commercial integrated circuit.

As MOSFETs device scaling, we need to redesign the device to keep long channel behavior as far as possible. With the decrease of channel length, the depletion width of source and drain is equivalent to the length of channel, and the tunneling between drain and source is unavoidable, which demands higher doping of the channel lead to enhance the threshold voltage. For the sake of controlling the threshold voltage reasonably, we need a thinner oxide. The device performance optimizes using certain scaling rules.

Even if we use the optimal scaling rules, the deviation of long channel characteristics is inevitable as the channel length decreases. The two-dimensional potential distribution and the strong electric field in the channel region cause these deviations, namely the short-channel effect, causing the gradual channel approximation no longer to hold. This two-dimensional potential distribution creates many undesired electrical properties. With increasing the electric fields, the mobility of the channel depends on fields, and the final velocity is saturated. With increasing the electric fields further, the number of carriers has multiplied in the vicinity of the drain, creating a substrate current and parasitic bipolar transistor action. The strong electric field also causes the injection of hot carriers into the oxide, resulting in oxide charging, subsequent threshold voltage shift and

transconductance degradation.

In order to avoid the short channel-effect, the ideal scaling rule is to scale down all the dimensions and voltages of the long channel MOSFET. The same internal electric field can be obtained [10]. Table 5-1 and Figure 5-2 show the constant-field scaling [9]. This method provides a simple image for the miniaturization of device. The dimensions of the channel length and width, junction depth and oxide thickness, reduces by the same scaling factor *k*. The doping concentration increases by *k*, and voltages decreases to 1/*k*. So the junction depletion width decreases to 1/*k* or so.

However, there are several factors which impede the ideal scaling rule. It is worth noting that there are two ways to reduce the size of the device. Firstly, three-dimensional MOSFETs with ultra-thin body regions effectively eliminate most of the punch-through conductive paths and relax the need for channel doping. Secondly, people are always seeking gate dielectrics with high dielectric constant (*k*), which relaxes the need for the geometric thickness of dielectrics, reduces the tunnel field and improves defect density. These two techniques can contribute to prevent short-channel effects in devices with particularly small channel length.

Parameter	Scaling factor: Constant-$\mathcal{E}$	Scaling factor: Actual	Limitation
L	$1/\kappa$	/	/
$\mathcal{E}$	1	> 1	/
d	$1/\kappa$	$> 1/\kappa$	Tunneling, defects
r_j	$1/\kappa$	$> 1/\kappa$	Resistance
V_T	$1/\kappa$	$\gg 1/\kappa$	Off current
V_D	$1/\kappa$	$\gg 1/\kappa$	System, V_T
N_A	κ	$< \kappa$	Junction breakdown

Table 5-1 MOSFET Scaling [9].

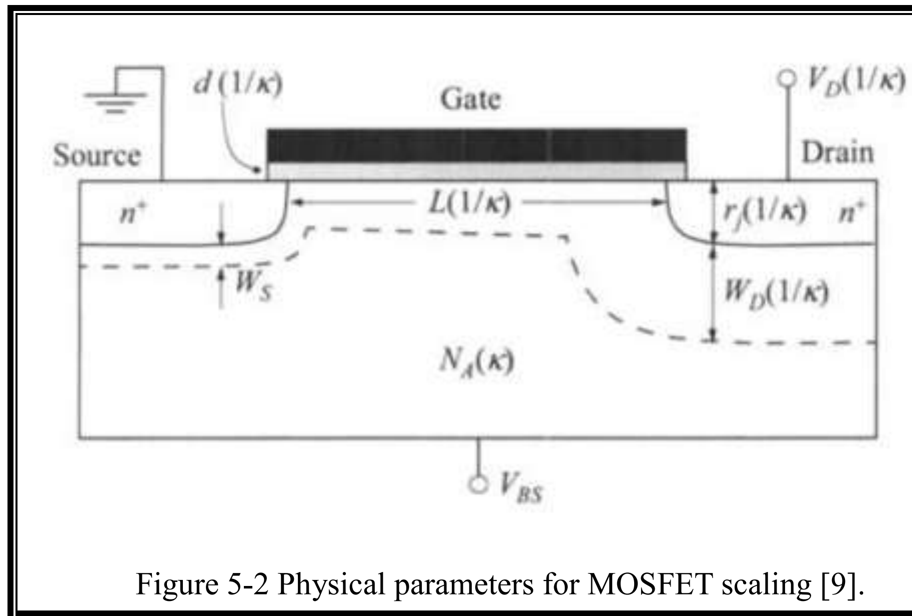

Figure 5-2 Physical parameters for MOSFET scaling [9].

AlGaN/GaN HFETs have attracted many attentions for power and microwave applications due to the high mobility of the 2DEG [11,12]. To achieve high-gain millimeter-wave power amplification, the key challenge is to increase the maximum cut-off frequency (f_T). Self-aligned gate (SAG) structure is an effective method to reduce the access resistance of AlGaN/GaN HFETs, which is beneficial for achieving high f_T [13]. In the SAG structure, the Schottky gate serves as the mask for ohmic electrode deposition and anneals simultaneously with the ohmic electrodes. A high annealing temperature (commonly above 700 ºC) is needed for the widely used Ti/Al-based multilayers on AlGaN/GaN HFETs to obtain ohmic contact, which usually causes a high gate leakage current of the Schottky contact and degrades the noise handling capacity [14]. One of the solutions is to develop a low temperature ohmic process (below 600 ºC) with the assistance of ICP treatment, but it is difficult to control the etching depth and uniformity [15,16]. Figure 5-3 (a) shows the conventional HFET fabrication process. It needs to be annealed at a relatively high temperature to form an ohmic contact first. After forming the ohmic contact, gate electrode is deposited, which reduces the minimal source-to-gate and drain-to-gate distance and let it very difficult achieve a little access resistance. In a SAG process (Figure 5-3 (b)), the fabrication of a T-shaped Schottky gate is carried out first, which is used directly as a mask of the ohmic metal formation.

On another hand, MOS HFETs with gate dielectric are help to decrease the gate leakage

current. To meet the SAG process requirement, the dielectric should withstand the high annealing temperature. Besides, to scaling-down the gate length as well as the dielectric thickness for higher frequency, it usually adopt high dielectric constant (high-*k*) gate dielectric to suppress the serve leakage current problem [17-19].

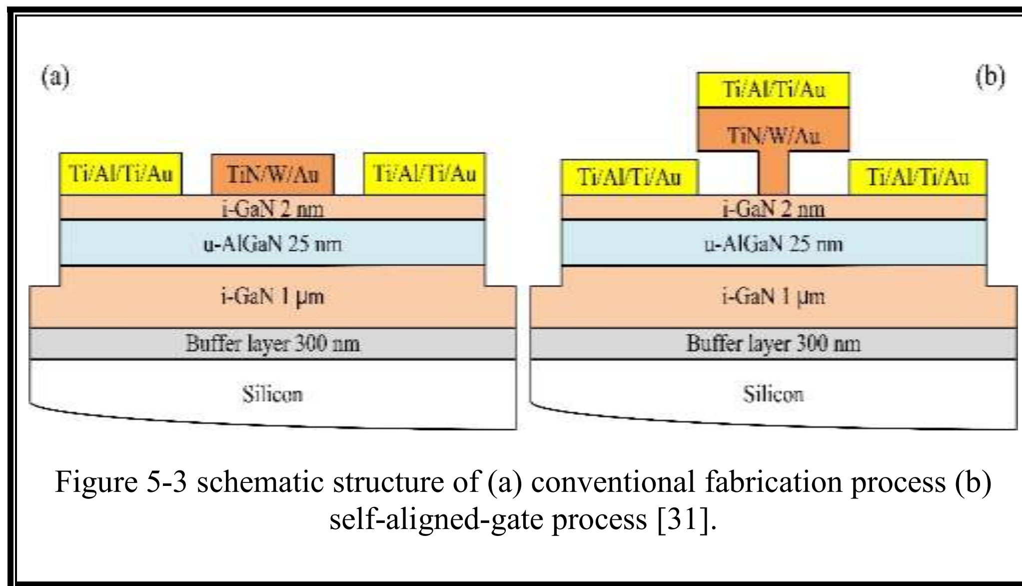

Figure 5-3 schematic structure of (a) conventional fabrication process (b) self-aligned-gate process [31].

However, high-k materials need to remain amorphous after device fabrication. The materials will produce large amounts of grain boundary after crystallization. Oxygen or dopants can easily diffuse into a gate dielectric and an even channel region in silicon substrate by grain boundaries in fully or partially crystallized gate dielectric resulting from a high-temperature process which can be the fast pathways for atomic diffusion. This will result in formation of a low-k interfacial layer at a high-k/Si, threshold voltage (Vth) instability, and long-term dielectric reliability degradations on account of defect generation [17]. However, the crystallization temperatures of most binary oxides are much less than 800 ^oC.

Among various gate dielectrics, hafnium oxide (HfO_2) possesses high-*k*, wide bandgap, and acceptable band offsets (ΔE_V=2.1 eV and ΔE_C=0.3 eV), is extensively investigated as one of the most promising candidates [20-22]. However, the crystallization temperature of the HfO_2 film is usually close to 500 ^oC, which means that the microcrystalline structure appears after ohmic annealing at high temperature [23]. Then, oxygen or dopants from the environment can easily diffuse into the gate dielectric via grain boundaries,

leading to the increasing leakage current, threshold voltage (V_{th}) instability, and long-term dielectric reliability degradation [24].

Recently, many studies focused on the hafnium oxynitride film (HfO_xN_y) by incorporating nitrogen atom into HfO_2. The existence of Hf-N bond in the bulk and N at the dielectric/GaN interface could act as a crystallization inhibitor, which produce the distortion for the equilibrium of the lattice, disordered states and improvement of the thermal stability (crystallization temperatures of 800–950 ºC) [25-27]. Because of oxygen shows a stronger reactivity to Hf than nitrogen, we should carefully control the oxygen flow rate to guarantee the excellent properties of HfO_xN_y dielectric [28]. Therefore, it is worthwhile to further study electrical and material characterizations of HfO_xN_y film. Herein, we try to obtain HfO_xN_y film by optimizing the oxygen percentage in the N_2/Ar mixture sputtering ambient. Then, we also explore the thermal stability of the TiN/ HfO_xN_y gate stack structure. The physical properties of the HfO_2 and HfO_xN_y films are shown in Table 5-2.

name	HfO_2	HfO_xN_y
dielectric constant	24	21
bandgap	5.6 eV	5.7 eV
crystallization temperatures	500 ºC	800-950 ºC

Table 5-2 The physical properties of the HfO_2 and HfO_xN_y films.

§5.2. The synthesis of HfO_xN_y

§5.2.1. The synthesis of HfO_xN_y films

HfO_xN_y films were first formed on double-sides polished sapphire substrates using reactive sputtering. A 50nm thickness HfO_xN_y was deposited by reactive sputtering in Ar, N_2, and O_2 mixed ambient (Ar:N:O=15:15:x) using a Hf target. Atomic force microscope (AFM), X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and UV-Vis diffuse reflectance spectrophotometer (UV-Vis DRS) were used to characterize the structure, morphology, and optical properties of the as-deposited HfO_xN_y films.

In this experiment, the epitaxial layers of the n-GaN were deposited on a sapphire substrate by metal organic chemical vapor deposition (MOCVD). The ohmic contact metals were constituted by a Ti/Al/Ti/Au (50/200/40/40 nm) multi-layer structure and treated by annealing at 850 °C in N_2 atmosphere for 3 min. After gate pattern lithography, the samples were subjected to O_2 plasma ashing for surface cleaning and then immersed in diluted HCl (HCl:H_2O=1:1) for over 5 min to remove the native oxide layer. A 50nm thicknesss HfO_xN_y layer was grown by reactive sputtering in Ar, N_2, and O_2 mixed ambient (Ar:N:O=15:15:x) using a Hf target. Then the TiN films (about 50nm) were constituted by DC magnetron reactive sputtering in Ar and N_2 ambient (Ar:N_2= 15:3 sccm) under a chamber pressure of 0.14 Pa, using a Ti target with a purity of 99.99% on the HfO_xN_y layer directly. Then a cap layer of Ti/Au (10/40 nm) was deposited in Ar atmosphere on a TiN layer to reduce the gate resistance. Finally, post-annealing at 300 °C was conducted for 10 min.

§5.2.2. The characteristics of films

First, HfO_xN_y films are deposited on sapphire substrates to evaluate the effect of oxygen flow rate on the structure and properties. The surface morphology and the growth rate of HfO_xN_y films are characterized using atomic force microscope. When introduce a low flow rate of oxygen (0 and 1 sccm), the surface of the samples consist with high density and small size particle (Figure 5-4 a and b). The root mean square roughness (RMS) of those samples are approximately 0.12 and 0.13 nm, respectively. The particle size increased obviously for the sample deposited with a medium oxygen (3 sccm) (Figure 5-4 c), but the surface is still flat with a RMS of approximately 0.12 nm. Finally, the film obtained with 5 sccm oxygen showed the most rough morphology with a RMS of approximately 0.29 nm. Besides, obvious pits appeared on the surface, implying the growth mode changed seriously. We calculate the average sputtering rates from dividing the total film thickness by the deposition times. The rates were approximately 0.83, 0.66, 0.56, and 0.42 nm/min with the oxygen flow rate of 0, 1, 3, and 5 sccm, respectively. When introducing oxygen into the chamber, a decrease of the sputtering yield as well as the oxidation of the Hf target surface will cause the decrease of sputtering rate. At a relatively low oxygen flow rate, the oxidation of the Hf target is very weak. The sputtered

Hf atoms on the substrate surface has enough time to diffuse and react under a lower sputtering rate, resulting in a better surface roughness. While at a relatively high oxygen flow rate, the oxidization of metal target surface is much easier by oxygen because of the high bonding energy between oxygen and hafnium. Therefore, the sputtered HfO_2 on the substrate is relatively difficult to diffuse, which will deteriorate the film quality and cause the pit defect.

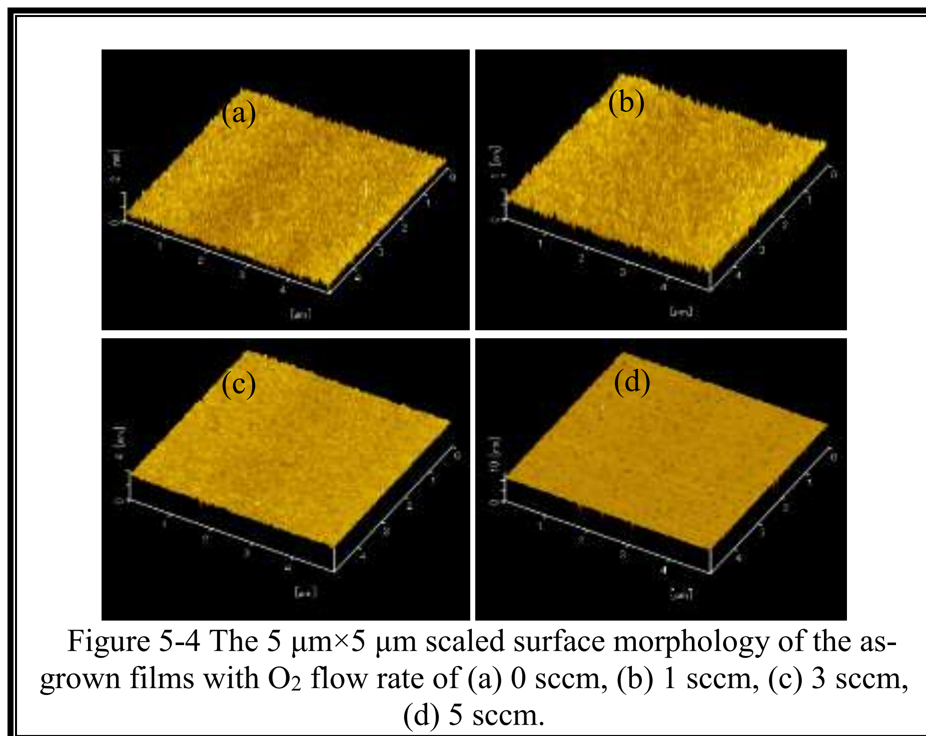

Figure 5-4 The 5 μm×5 μm scaled surface morphology of the as-grown films with O_2 flow rate of (a) 0 sccm, (b) 1 sccm, (c) 3 sccm, (d) 5 sccm.

Figure 5-5 compares the X-ray photoelectron spectroscopy (XPS) of HfO_xN_y films deposit at different oxygen flow rates. The Hf4f core level (CL) spectrum of the sample without oxygen can be fitted into Hf-$4f^{5/2}$ and Hf-$4f^{7/2}$ located at 14.3 and 15.7 eV, respectively, which agree well with the reported values for HfN. Furthermore, the N–Hf peak at 396.7 eV in N1s CL spectrum and no detectable peak in O1s CL spectrum also confirm the above result. While for the sample deposit with 1 sccm oxygen, the Hf-4f CL spectrum has three obvious peaks at 15.7 eV, 17.2 eV, and 18.9 eV. The first peak as well as the weak peak in N1s CL spectrum demonstrate the existence of the Hf-N bonding [29].The latter two peaks separated by 1.6 eV originates from Hf bounded to oxygen. Besides, a major peak appear around 530 eV in the O1s CL spectrum after the introduction

of oxygen. Based on those results, the as grown film has transformed from HfN into HfO_xN_y because of the small oxygen flow rate. Finally, two peaks at 17.2 eV and 18.9 eV dominate the Hf-4f CL spectrum, an enhanced peak at 530 eV dominates the O1s CL spectrum as well as no detectable peak in N1s CL spectrum for the sample obtained with 5 sccm oxygen flow rate. This indicate that HfO_2 become the dominate phase because of the higher bonding energy between oxygen and hafnium.

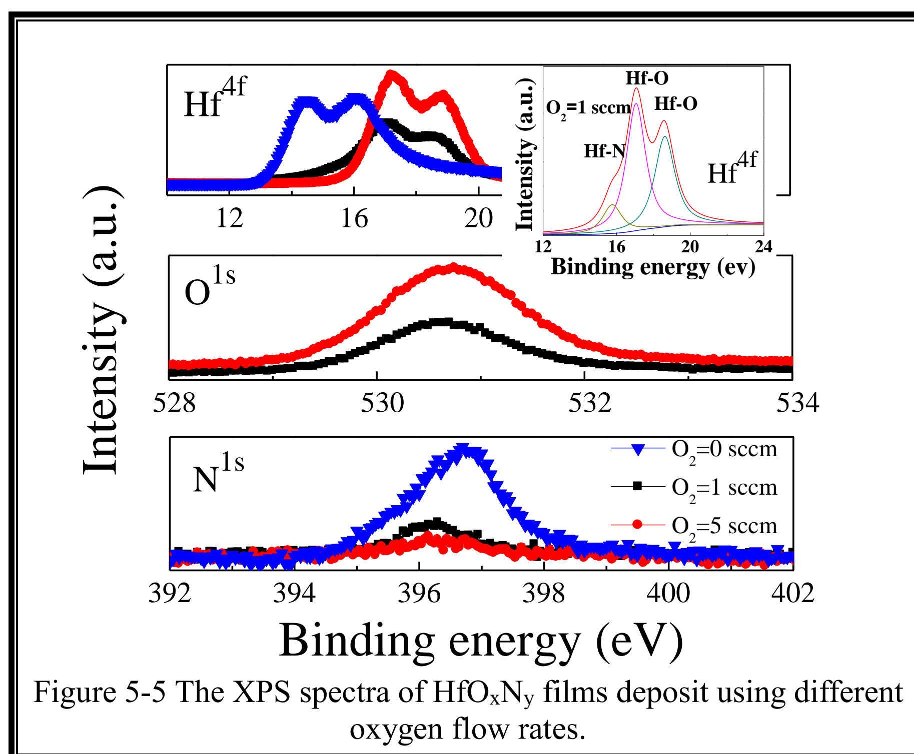

Figure 5-5 The XPS spectra of HfO_xN_y films deposit using different oxygen flow rates.

UV-vis diffuse reflectance spectrophotometer (UV-vis DRS) was used to study the optical absorption properties of the HfO_xN_y films. The optical absorbance decreased significantly with the increasing oxygen flow rate. Then, the absorbance (A) of samples are calculated as following:

$$A = -\lg(R) \tag{5-1}$$

Where R is the measured reflectance. Figure 5-6 shows that all films exhibit an absorption tail near 230 nm and no absorption in the visible region. By applying the following Tauc model and the Davis and Mott model, we obtained the optical band gap

(E_g) of the films from the absorption edge [30].

$$\alpha hv = D(hv - E_g)^n \tag{5-2}$$

where α is absorption coefficient, hv is the photon energy, D is a constant, and E_g is the optical band gap. Here, the value calculated using the absorbance instead of the absorption coefficient without no obvious effect on the band gap value. We obtained the E_g value from extrapolating the linear part to the zero absorption coefficients. As shown in the inset of Figure 5-6, the band gap of the films decrease from 5.55 eV to 5.19 eV with increasing oxygen flow rate from 1 to 5 sccm. One possible reason is that oxygen incorporation will lead to the deterioration of crystalline structure.

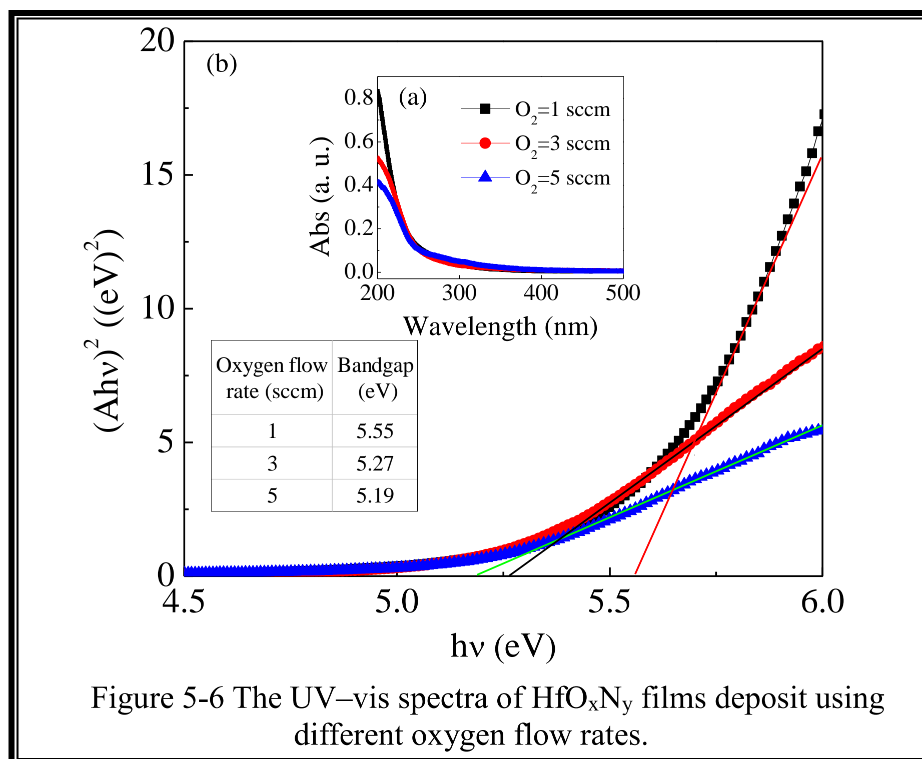

Figure 5-6 The UV–vis spectra of HfO_xN_y films deposit using different oxygen flow rates.

§5.2.3. Characteristics of MOS diode using HfO_xN_y

MOS structures were fabricated on n-GaN (1×10^{17} cm^{-3} dopant density, 0.1 μm thick, sapphire substrate) using different O_2 reactive sputtering gas (oxygen percentage) to evaluate the properties. Capacitance-voltage (Figure 5-7) characteristic at the high

frequency (1 MHz) of the sample with a TiN/HfO_xN_y film gate presents clear accumulation and depletion regimes. The corresponding C-V curves of the capacitor with HfO_xN_y film by 5 sccm oxygen, the flat-band voltage is shifted to a negative value in comparison with 1 and 3 sccm oxygen films, indicating a formation of positive charges. By scanning dc bias during C-V measurements, the dispersion is at spillover region at the higher voltage which is related to the capacitance variation at HfO_xN_y /AlGaN interface. Finally, MOS diode fabricated with HfO_xN_y film by 1 sccm oxygen shows the smallest reverse leakage current, which means that the increase of oxygen flow rate rises the leakage current of the devices. Combing those material properties, HfO_xN_y film deposit using 1 sccm oxygen is choose for device fabrication.

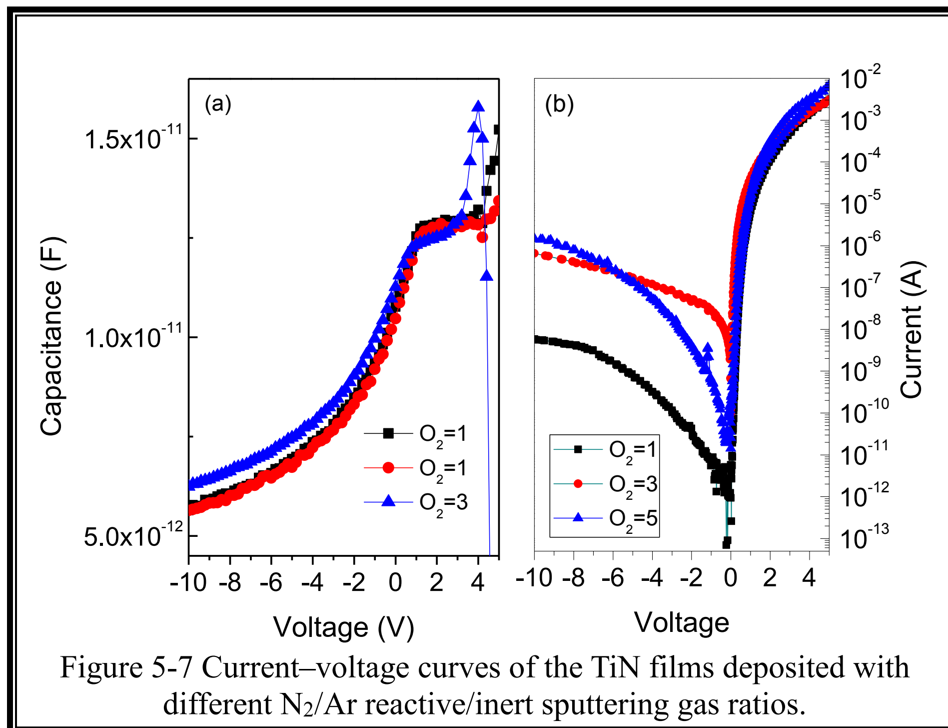

Figure 5-7 Current–voltage curves of the TiN films deposited with different N_2/Ar reactive/inert sputtering gas ratios.

§5.3. Thermal stability studies of Metal-oxide-semiconductor AlGaN/GaN HFETs using TiN/HfO_xN_y stack gate layer

§5.3.1. The fabrication of TiN/HfO_xN_y/AlGaN/GaN HFETs

The epitaxial layers used in this experiment are AlGaN/GaN HFETs grown on a

sapphire substrate by MOCVD. The device fabrication process started with inductively coupled plasma (ICP) isolation with an etching depth of 100 nm. Ti/Al/Ti/Au (50/200/40/40 nm) multi-layer structure was used to form ohmic contact by annealing at 850 °C for 3 min in an N_2 ambient environment. The samples were immerged into diluted HCl (HCl:H_2O=1:1) for over 5 min to get rid of the native oxide layer after gate pattern lithography. An HfO_xN_y layer with a nominal thickness of 50 nm was produced by reactive sputtering in an N_2, O_2 and Ar mixture ambient environment (Hf target) (Ar:N:O=15:15:1). A relatively smaller oxygen flow rate was choose because of the hafnium metal is easy to be oxidized. To investigate the thermal stability, the HfO_xN_y layer was annealing in N_2 ambient at 400, 600, 800, 900 and 1000 ^{o}C for 1min, respectively. The TiN gate electrode (about 50 nm) with a cap layer of Ti/Au (10/40 nm) were formed by DC magnetron reactive sputtering (as shown in Figure 5-8). The chamber pressure was maintained at 2×10^{-5} Pa. The sputtering target was firstly cleaned by a pre-sputtering in Ar atmosphere for 10 min under a sputtering power of 150 W. During the process of sputtering, the sputtering power was fixed at 75 W under a chamber pressure of approximately 0.18 Pa. The substrate was placed on a water cooling holder, which is 15 cm above the sputtering target. Finally, post-deposition anneal was conducted in an N_2 ambient at 300 °C for 10min to improve the contact.

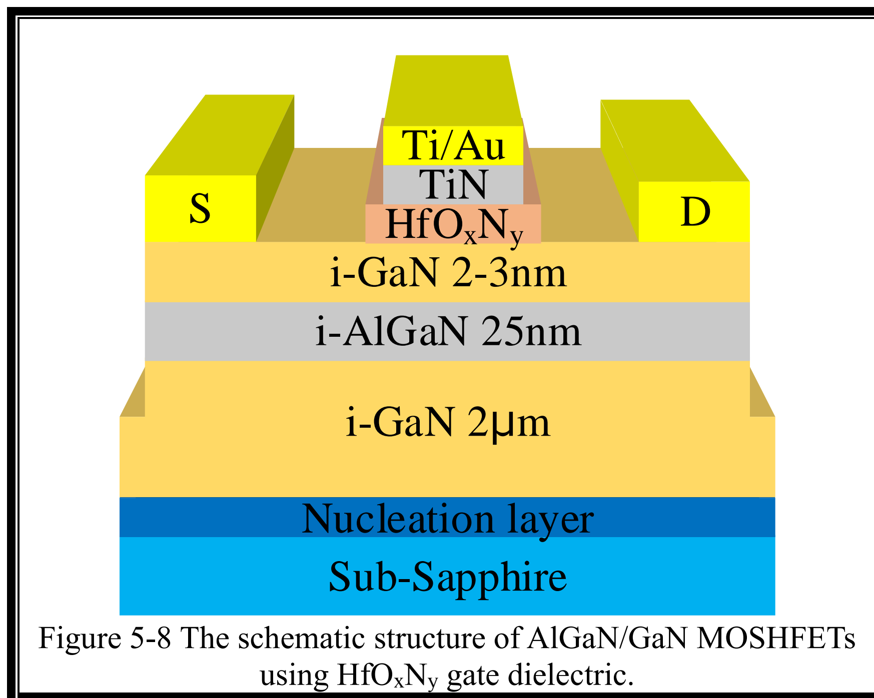

Figure 5-8 The schematic structure of AlGaN/GaN MOSHFETs using HfO_xN_y gate dielectric.

§5.3.2. The characteristics of TiN-gated and MOSHFETs devices

Figure5-9 shows the output and gate leakage characteristics of the devices with and without HfO_xN_y dielectric (gate length is 100 μm and gate width is 200 μm). The gate voltage swepts from -10 to 1 V with a step of 1 V. All of the devices operate well with the saturation current exhibiting a negative conductance at large drain voltage due to the self-heating and the decreased electron mobility (Figure 5-9 a). The maximum drain current density of MOSHFETs is larger than that of TiN-gated one because of the negative shift of V_{th}. As shown in Figure 5-10 a, the V_{th} for the Shottky contact, HfO_2 MOS, and HfO_xN_y MOS HFETs are approximately –3.0, –5.0, and –7.0 V, respectively. The corresponding gate current-voltage (I_g-V_g) characteristics of the square-type device also shows that the TiN gated HFETs has a reverse leakage current of about 10^{-6} A (Figure 5-9 b). Then, the gate leakage current decreases nearly four orders of magnitude in reverse bias and approximately five to six orders of magnitude in forward by introducing the HfO_2 and HfO_xN_y dielectric. Furthermore, the HfO_xN_y MOSHFETs has much lower forward current compared with the HfO_2 MOSHFETs, which suggested the HfO_xN_y film is more suitable for the gate dielectric material. However, the transconductance (Gm) of the MOSHFETs are slightly smaller than the Schottky-gated device, owing to the increase of

distance between the gate electrode and channel (Figure5-10 b).

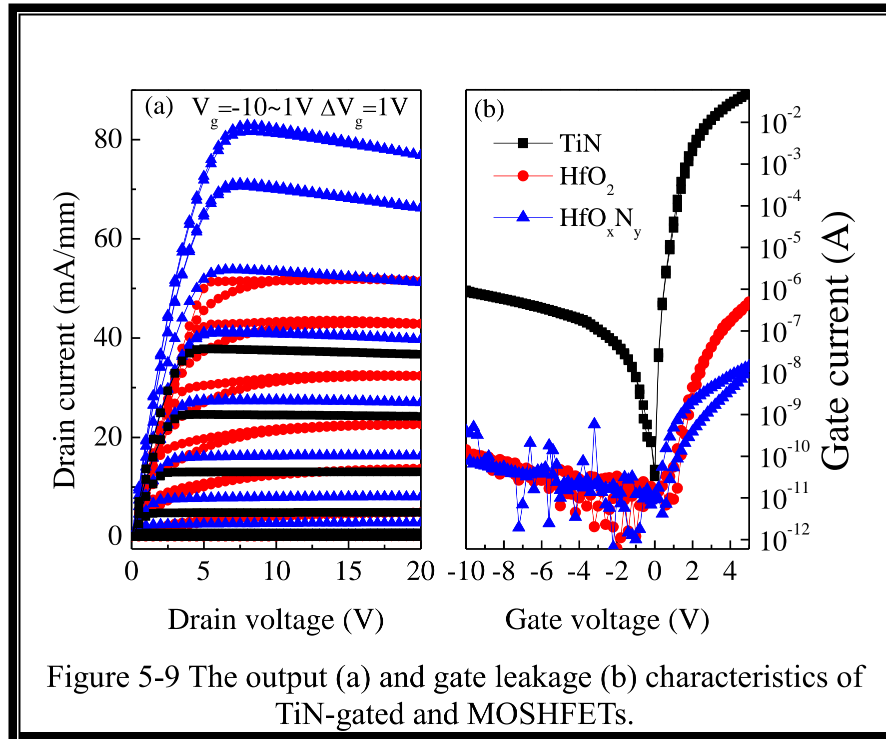

Figure 5-9 The output (a) and gate leakage (b) characteristics of TiN-gated and MOSHFETs.

The following equation estimates the permittivity of the oxide:

$$\frac{1}{C_{MOSHFET}} = \frac{1}{C_{HFET}} + \frac{1}{C_{oxide}} \tag{5-3}$$

Where $C_{MOSHFET}$, C_{HFET}, and C_{oxide} are the zero-bias capacitance of the MOSHFET, oxide layer, and HFET, respectively. The following equation calculates the capacitance of the oxide layer:

$$C_{oxide} = \frac{\varepsilon_o \varepsilon_{oxide} S}{d_{oxide}} \tag{5-4}$$

Where S is the capacitor area, ε_0 is the vacuum permittivity, *doxide* is the nominal oxide thickness. The permittivity of the oxide estimated from the capacitance-voltage curves on FATFETs (S =1.2 × 10^{-4} cm^2, *doxide*=50 nm) are approximately 12.1 and 10.5 for HfO_xN_y and HfO_2, respectively. Those values are relatively smaller than the theoretical value. The possible reasons are that the crystalline quality is not so good for the sputtered oxide and the real oxide thickness maybe thicker than the nominal one.

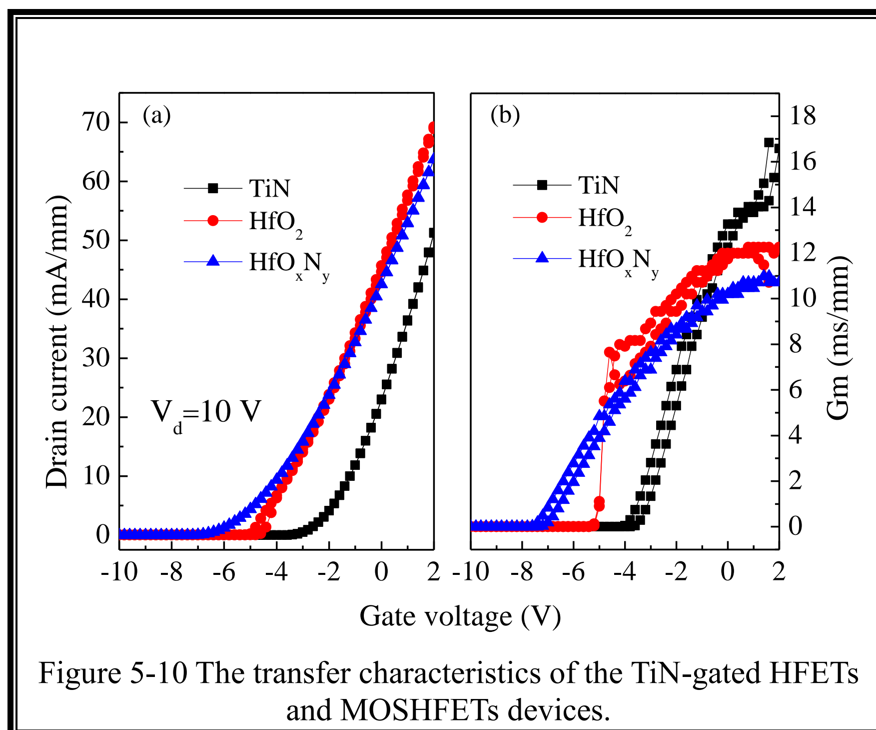

Figure 5-10 The transfer characteristics of the TiN-gated HFETs and MOSHFETs devices.

§5.3.3 The characteristics of TiN/HfO_xN_y/AlGaN/GaN HFETs with annealing

To evaluate the thermal stability of the HfO_xN_y and HfO_2 MOSHFETs, we measured the I-V characteristics of the devices after post deposition annealing at different temperatures (Figure5-11). Figure 5-11 a shows a typical output characterization of the HfO_xN_y device annealed at 900 °C. The device operates well with the output current is comparable with that of the non-annealed one. Figure 5-11 (b) shows the corresponding I_g-V_g characteristics at different annealing temperatures. The forward leakage increases gradually with the increasing annealing temperature from 400 to 900 °C, while the reverse leakage is nearly 10^{-9} A and increases obviously only at 900 °C, which illustrates that HfO_xN_y dielectric has a very good thermal stability. Further increased the annealing temperature to 1000 °C, the pinch-off characteristic of the device deteriorated with large leakage current. As a comparison, the output characterization of HfO_2 MOSHFETs device after annealing at 600 °C presents obvious leakage current, as shown in Figure 5-12. The leakage current of HfO_2 MOSHFETs deteriorated seriously after annealing at 400 °C, which is a little higher than that of the HfO_xN_y-gated MOSHFETs at an annealing temperature of 800 °C (as shown in Figure 5-12 b). A possible reason is that the crystallization temperature of HfO_xN_y film is enhance from approximately 500 °C (HfO_2)

to approximately 900 °C, resulting in a better thermal stability [13,17].

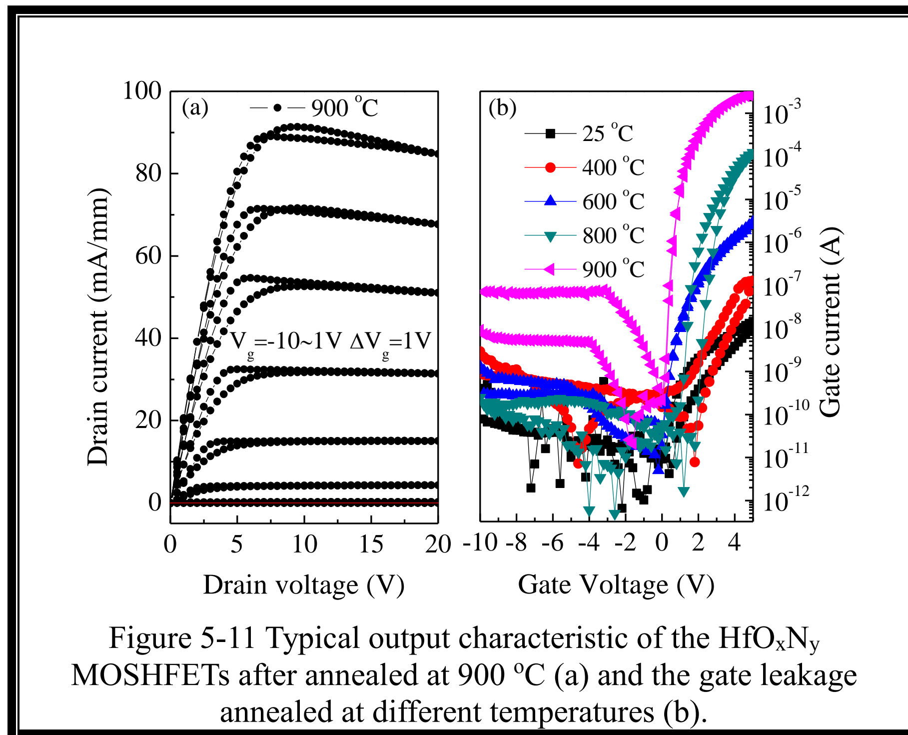

Figure 5-11 Typical output characteristic of the HfO_xN_y MOSHFETs after annealed at 900 °C (a) and the gate leakage annealed at different temperatures (b).

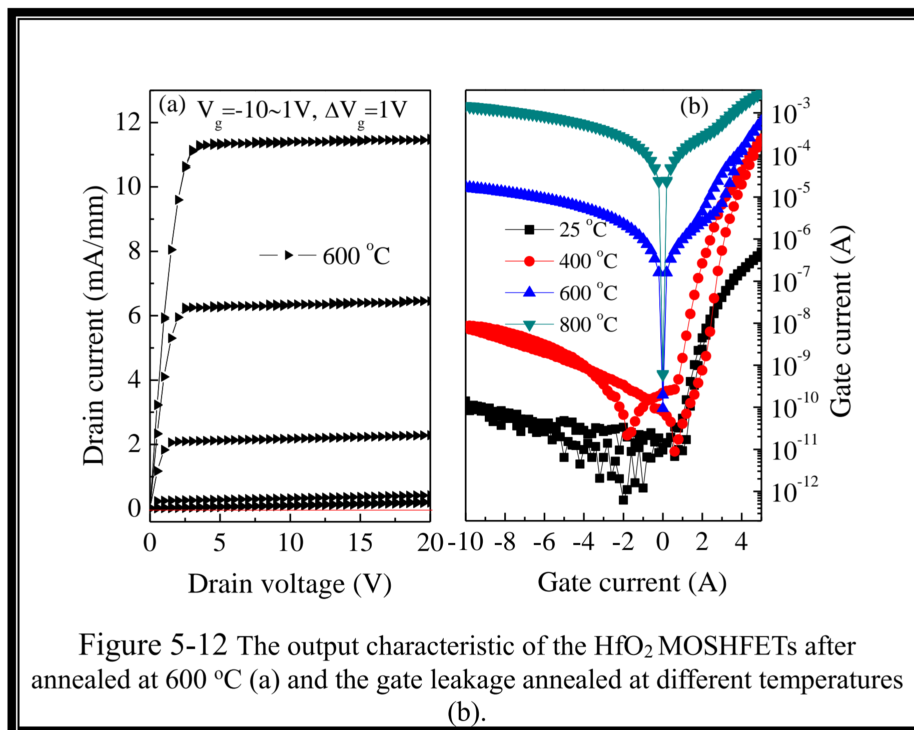

Figure 5-12 The output characteristic of the HfO_2 MOSHFETs after annealed at 600 °C (a) and the gate leakage annealed at different temperatures (b).

§5.4. Conclusion

To improve the performances of the resulting MOS-HEMTs, the wide bandgap oxide layer was deposited to form a gate dielectric stack. HfO_2 and HfO_xN_y with wide bandgap and high-k are extensive investigated as one of the most promising candidates.

The high-*k* material HfO_xN_y was fabricated with different oxygen flow rates in the reactive sputtering ambient. The synthesis conditions had been optimized by AFM, XRD, XPS and the electronic characteristic. MOS diodes using high-k HfO_xN_y films were deposited under different O_2 flow rate. The reverse leakage current of the MOS diode fabricated with HfO_xN_y film by 1 sccm oxygen is approximately two order lower than HfO_xN_y film by 3 and 5 sccm.

We fabricated TiN/HfO_xN_y/AlGaN/GaN MOSHFETs with different oxygen flow rates in the reactive sputtering ambient. The composition of films changed from HfN to HfO_2 domination with the increasing oxygen flow rate and HfO_xN_y formed at a medium oxygen flow rate. Compared with HfO_2 MOSHFETs, the introduction of the HfO_xN_y dielectric results in a negative shifting threshold voltage and a lower leakage current. After post deposition annealing at different temperatures, the devices using HfO_xN_y dielectric show good thermal stability at 900 ^oC while obvious degradation are observed for the HfO_2 MOSHFETs at 600 ^oC. A possible mechanism is that the existence of Hf-N bond in bulk dielectric and N at the dielectric/GaN interface can help to improve the thermal stability.

§5.5. Reference

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Chapter 6: Conclusions and future works

§6.1. Summary and conclusions

Due to the superior material properties of GaN, AlGaN/GaN HFETs have become the subject of competing research. In the field of high temperature and high frequency, an urgent need is to reduce the leakage current. For MOSFETs, there is an urgent need to find materials with high *k* and high crystallization temperatures for their high temperature applications. In this thesis, we discussed the synthesis and application of oxide for GaN electron devices, and the details as follows:

NiO is a natural p-type semiconductor with stable chemical properties. Firstly, we fabricated NiO films with different O_2/Ar ratios of 15%, 25%, 50%, and 65%. The NiO films with the face-centered cubic crystalline structure are analyzed by AFM, XRD, XPS and UV-Vis transmittance spectra. An optimal oxygen ratio for growing NiO is obtained.

And then we evaluated the effect of the substrate temperature on the properties of the NiO films using magnetron reactive sputtering. All NiO samples can be indexed as (111) oriented face-centered cubic crystalline. When the substrate temperature increased from 30 to 200 °C, the crystalline quality and stoichiometric of the NiO film were improved, resulting in higher bandgap value and resistivity. While further increasing the substrate temperature to 300 °C, the decomposition of NiO will cause the appearance of Ni metal in the film. The NiO film under 30 °C has a lowest resistivity.

Next, we have investigated the electrical properties of the NiO/GaN heterojunction device in the temperature range 25-175 ºC. The turn-on voltage of the NiO/GaN heterojunction diode is relatively higher, comparing with the Ni/GaN Schottky diode. The NiO/GaN diode shows the more smaller reverse leakage current with exhibiting a temperature-dependent turn-on voltage. The as-grown NiO exhibited cubic crystalline structure with a bandgap of 3.2 eV. The three types of current transport mechanism are found to be strongly related to the applied bias voltages and temperatures. On the other hand, the device exhibited considerably a stable behavior over the temperature range of

25-175 °C and will be favorable for wildly applying in high-temperature and high-power environments.

Combining the material and electric results, the NiO film under 30 °C with lowest resistivity is used as the gate electrode for HFETs application. Compared with the Ni/Au-gated device, the threshold voltage of the NiO-gated device has a positive shift of approximately 1V because of the p-type conductivity as well as the conduction band offsets between NiO and GaN. The band offset at the heterojunction interface can be measured by XPS employing a well-known Kraut's method. The corresponding valence and conduction band offset is calculated to be 1.25 and 1.42 eV using a band gap of 3.57 eV for the NiO film. For the normally-off AlGaN/GaN HFETs, we fabricated NiO gate with recess structure, the threshold voltage for the Ni- and NiO-gated HFETs has a positive shift after recessing. Normally-off GaN HFETs can be obtained with a threshold voltage of closing to 0 V with the recessed-gate structure.

HfO_2 and HfO_xN_y with wide bandgap and high-k are extensive investigated as one of the most promising candidates. Finally, we fabricated TiN/HfO_xN_y/AlGaN/GaN MOSHFETs with different oxygen flow rates in the reactive sputtering ambient. The composition of films changed from HfN to HfO_2 domination with the increasing oxygen flow rate and HfO_xN_y formed at a medium oxygen flow rate. Compared with HfO_2 MOSHFETs, the introduction of the HfO_xN_y dielectric results in a negative shifting threshold voltage and a lower leakage current. After post deposition annealing at different temperatures, the devices using HfO_xN_y dielectric show good thermal stability at 900 ºC while obvious degradation are observed for the HfO_2 MOSHFETs at 600 ºC. A possible mechanism is that the existence of Hf-N bond in bulk dielectric and N at the dielectric/GaN interface can help to improve the thermal stability.

§6.2. Suggestion for future works

As shown in chapter 4, the tunneling of electron and leakage current decreases with the existence of p-type NiO gate layer. After recess, it has a positive shift with the smaller drain current density for the threshold voltage of the Ni- and NiO-gated HFETs. However, with the recessed-gate structure, the threshold voltage of normally-off GaN HFETs is only close to 0 V because of the uncontrollable rate for ICP. Therefore, we need to further

optimize the condition of the normally-off HFETs.

The reverse leakage current of the devices can effectively decrease for the MOSHFETs. However, the crystallization of materials caused the higher reverse leakage through the grain boundaries of oxide layer at a high temperature. Finding other oxide materials with resisting high temperature to decrease the leakage current for self-align gate devices is necessary.

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