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論　文　内　容　要　旨

報告番号	甲　先　第　329　号	氏　名	片山　貴文
学位論文題目	Key Extension Technologies for Future Video Coding (次世代動画像符号化技術向け拡張方式の要素技術に関する研究)		

内容要旨

H.265/HEVC is the new next generation video compression standards, which is developed by the ITU-T video coding experts group (VCEG) together with the ISO/IEC moving picture experts group (MPEG). The final drafting version of H.265/HEVC is released in 2013. Afterwards, the standard is continually extended to support more new advanced video applications which include high resolution, scalable or multi-view video applications. As evaluated by many researchers, the H.265/HEVC standard can achieve much more coding efficiency compared with the previous video compression tools. However, the complexities of corresponding algorithms have increased the difficulty of implementation. Especially, for high-resolution video, multi-view video applications, simulcast etc, software coding require a very high computational complexity. Therefore, when the real-time processing is required, application specified hardware has been acknowledged as a good way of implementation for the H.265/HEVC encoding. Moreover, because various contents are increased to satisfy the requirement of the consumer, the importance of the extension technique become very high. This paper studies on the key technology for the future video coding. As shown in following contents, the main research contents include two parts.

(1) Scalable extension

Recently, various video streams needed to be generated because of increasing of multi-cast service and terminal devices. One approach to full this requirement is coding the video streams in all available formats (simulcast coding) and transmitting them separately. As well know, this approach requires more bandwidth. The other approach has been developed as a scalable video coding (SVC) tool, which enables the video coding system to deliver different versions of the same video content within the same bit-stream. Compared to simulcast coding, SVC requires less bandwidth. Furthermore, many consumer electronic devices are developed for a various display, processing, and transmission capabilities. Therefore, scalable coding plays the role of an important tool.

(2) Future extension

Various extension technologies of HEVC were examined from 2014 to

2016 in order to satisfy consumers' demands. Also, since the precision of image recognition by an artificial intelligence(AI) has greatly improved in 2016, to apply the AI to image processing was expected. Therefore, it is necessary to propose a new coding technique using AI for super-resolution such as 8K. One of our research aim is to develop the preprocessing software architecture of AI for greatly improving a coding efficiency.

Our research target is the complexity reduction of the extension model of HEVC and implement its hardware architecture. We consider that the diverse terminal device, 3D view (VR), and the device including the AI require the complexity reduction and the improvement of the coding efficiency according to extension technology because the target of the future video coding is super-resolution(8K). The main research contents consist of a conventional extension model and next future model. The main research results are as following:

(1) Scalable extension

Our research focus is on developing a complexity reduction scheme for spatial scalable SHVC encoder. The proposed algorithm uses fast coding unit(CU) depth decision (FCDD), fast mode decision (FMD), and early termination process (ETP). The performance of the proposed algorithm was tested over a representative set of video sequences and was compared to the unmodified SHVC encoder as well as two of the art complexity reduction schemes and combinations. Performance evaluations show that our proposed algorithms reduce encoding time on average 61.88% and increases BD-rate about 0.9%, compared with SHM 11.0. Moreover, to confirm a validity of the proposed FCDD algorithm, the hardware architecture is designed targeting on the FCDD algorithm. Synthesis results show that the hardware cost is about 1.8K gates and achieve the scalable working clock frequency in the case of FPGA (Cyclone V) implementation.

(2) Future extension

We proposed the preprocessing AI software architecture for HEVC and the future coding technique. The new encoding model reduce the computation complexity significantly, and the CNN structure is simple. Specifically, CNN investigates the textures of a CU, and then determines the optimal CU configuration. As compared to the reference software HM16.7, the conservative configuration of our algorithm saved 66.7% encoding time and 70.1% complexity reduction, at the cost of 1.8% BD-rate increment.

In conclusion, our research has greatly contributed to the next generation video coding standard by the proposed various low complexity algorithms and hardware implementation.