Study on Normally-off AlGaN/GaN Heterostructure Field-Effect Transistors with P-GaN Cap Layer

P-GaN キャップ層を有するノーマリオフ型 AlGaN/GaN ヘテロ構造電界効果トランジスタに関する研究

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Abstract

With respect to Silicon-based material, GaN has abundant merits for the application of low power consumption due to its 3.4 eV energy bandgap (1.1 eV for Si). Owing to the unique properties of 2DEG in AlGaN/GaN heterosturcture, GaN-based HFETs have become one of the most attractive research region. However, to alleviate the drawback of normally-on operation in conventional AlGaN/GaN HFETs and satisfy safety requirement, the normally-off HFETs is proposed and become the researching hot point. In this thesis, there are four parts will be introduced, they are 1) device and process design of normally-off AlGaN/GaN HFETs on AlGaN/GaN heterostructure; 2) study on the feature of blocking layer in normally-off HFETs, and the influence of blocking layer on device performance; 3) the normally-off HFETs with MIS gate is proposed for improving device threshold voltage and performance, the impact of varied SiN_x thickness on performance is analyzed; and 4) the feasibility of self-aligned gate (SAG) with gate first process is confirmed, the superiority of SAG is deduced by analyzing the device characteristics. Moreover, the optimized normally-off SAG device is fabricated. And gate-first process is redesigned.

In chapter 2, the basic structure and fabrication process, test methods for p-GaN gate HFETs were described in details. Based on the process of conventional HFETs, the fabrication process of HFETs with p-GaN cap layer is developed and demonstrated in details. Meanwhile, the mechanism of normally-off operation by p-GaN is analyzed. Moreover, the fabrication process included cleaning, mesa etching, ohmic contact, gate contact. In particular, the ohmic contact and gate contact were discussed. The field-effect electron mobility could be calculated by a method of gate capacitance-transconductance ($C\text{-}G_m$).

In chapter 3, the normally-off operation in the p-GaN gate HFETs with i-GaN blocking layer is confirmed. The performance of the p-GaN gate HFETs are extracted by I-V measurement, including the threshold voltage, gate leakage current and ohmic contact by TLM model. As comparison, the normally-on HFETs on access region is also fabricated, and the device characteristics is investigated. A phenomenon is appeared that device performance such as threshold voltage, drain current and ohmic contact has a great relationship with blocking layer thickness. The possible reason is the Mg^+ diffusion

during the p-GaN growth, that the Mg^+ as p-type doping can decrease the 2DEG concentration. The Mg element content was analyzed by secondary ion mass spectroscopy (SIMS). The Mg concentration in 2DEG channel is decreasing by raising i-GaN blocking layer thickness. On the other hand, field-effect mobility device is extracted in devices with varied blocking layer thickness by C-G_m method, which has the proportional relation with Mg content. Besides, the most optimal i-GaN layer thickness was figured out according on normally-off/on devices characteristics.

In chapter 4, Due to the higher threshold voltage requirement in practical application, to raise threshold voltage furtherly is investigated. Refer to regular MOS structure, a dielectric layer is considered to be used in normally-off device. Therefore, MIS-HFETs with p-GaN layer is fabricated, where the SiN_x is as dielectric layer. The fabrication process is demonstrated with different SiN_x thickness. Due to the dielectric layer, threshold voltage has a great increasing, and the gate leakage current is significant decreasing which is compared with a MOS device. The reason of positive shifting threshold voltage is that the existence of the dielectric layer is increasing the turn-on resistance, which can be observed from the on-state resistance of device. Besides, different devices have the similar mobility value, it indicates that the SiN_x thickness has no influence on device mobility. However, several drawbacks are existing, so the optimized structure is required.

In chapter 5, the normally-off SAG MIS-HFETs with p-GaN layer is fabricated, it confirms that this SAG structure with gate-first process is feasible for the MIS-HFETs, this structure can induce a more stable device performance. Compared to the conventional MIS-HFETs with p-GaN layer, the lower channel resistance is observed in SAG device. At the same time, it also leads a little low threshold voltage but higher output performance. For enhance the device performance, a SiN_x of 50 nm is adopted as dielectric layer. Higher output performance is confirmed. Device performance are extracted by I-V and C-V characteristics curves. Further, the interface state between p-GaN and dielectric layer is deduced with the SS curve. And the influence of hydrogen during the SiN_x growth on p-GaN hole concentration is analyzed as well as.

Key words: AlGaN/GaN heterostructure, normally-off, blocking layer, gate-first, metal-insulator-semiconductor.

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Chapter 1：Introduction

§1.1 Background

The power electronics technology is an important role in modern society. Nowadays, the relative high scale energy used by industrial production and living is from the electric source. So how to improve the usage efficiency of the electric energy is the necessary projection to promote human society development. In power electronics devices, the highly efficient electronics device is desired from the electronics switcher or rectifiers. For achieving the more efficient electronics conversion, many requirements are raised such as the less conduction loss, operation in high temperature, high performance electrical conductivity and so on. By the state of art, these Si-based devises almost reach the material limitation which had been researched for more than half century. For satisfying the practical requirements, the Gallium Nitride (GaN) is to be developed which has the most promising as third-generation semiconductor material. Due to GaN's high breakdown voltage, wide bandgap, ruggedness, efficiency and thermal management capabilities, the GaN-based device possess the widely application prospect. As shown in figure 1-1, the GaN-based device has the more abroad power density range and more widely frequency region from low to high frequency than Si-based device, which is compared to SiC-based device.

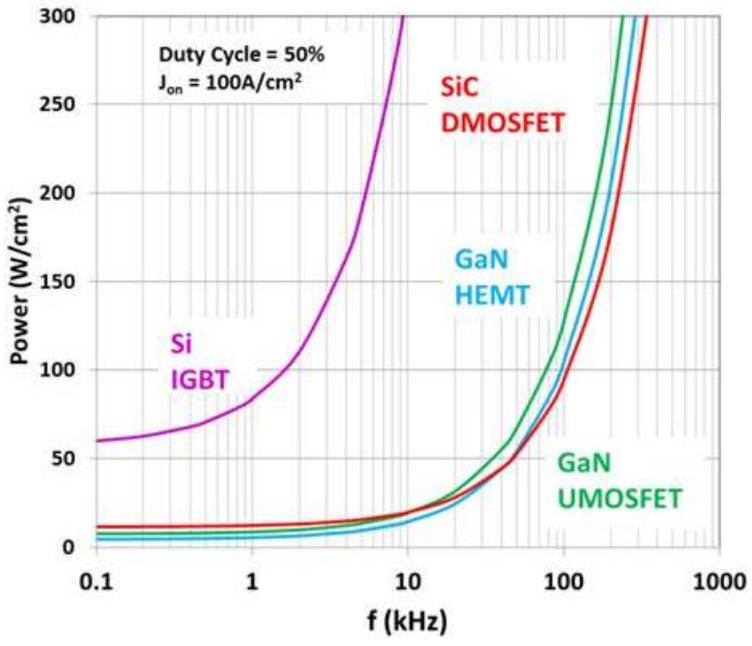


Figure 1- 1 The applications of GaN devices in power electronics field.

§1.2 The properties of GaN-based materials

§1.2.1 Crystal structure of GaN

GaN as III-N based semiconductors has three kinds of crystal structures, wurtzite, zincblende and rock-salt [1-2]. The crystal structure is mainly dominated by its iconicity. Both covalent bond and ionic bond exist in the crystal of a compound semiconductor. The more ionic composition in the crystal lead the stronger iconicity the crystal, and it's easier to form a wurtzite structure. Due to the strong iconicity of the nitride semiconductors, hence the wurtzite structure is most common GaN crystal structure and also the most stable structure at room temperature and 1 atm. In general, the GaN is in form of hexagonal wurtzite structure. Besides, the zinc-blende structure is metastable structure and just existing in certain condition. In normal condition, III-V nitride material are more stable and representative in wurtzite structure [3].

GaN epitaxial layer of wurtzite structure is grown on c-orientation substrates which generally transfer their hexagonal symmetry to GaN, such as (0001) sapphire or (0001) 6H-SiC. The GaN epitaxial layer of zincblende structure can be grown on substrates of cubic structure, such as (001) GaAs, (001) 3C-SiC or (001) Si substrate. In this thesis, GaN samples implemented in all the experiments are under wurtzite structure.

Both of zincblende and wurtzite structure have tetrahedral coordination: each atom is surrounded by four equidistant nearest neighbors which lie at the corners of a regular tetrahedron. The main difference between these two close-packed structures is the layer stacking sequence: for the zincblende structure, the stacking sequence of (1111) layers is ABCABCABC... along the <111> direction; for the wurtzite structure, the stacking sequence of (0001) layers is ABABAB... along the <0001> direction.

Figure1-2 shows the wurtzite and zincblende lattice structure of GaN. The wurtzite structure has a hexagonal unit cell and consists of two interpenetrating hexagonal close-packed (hcp) sub-lattice, which constituted by gallium and nitrogen atoms respectively. Each sub-lattice are shifted against each other along the c-orientation (i.e. [0001] direction) by the distance u= (3/8) c=0.375c.The zincblende lattice consists of two interpenetrating face-centered cubic (fcc) sub-lattice. One sub-lattice is gallium and the other is nitrogen, each sub-lattice are shifted against each other along the body diagonal of cubic cell by 1/4 of the width of the unit cell (Figure 1-2b).

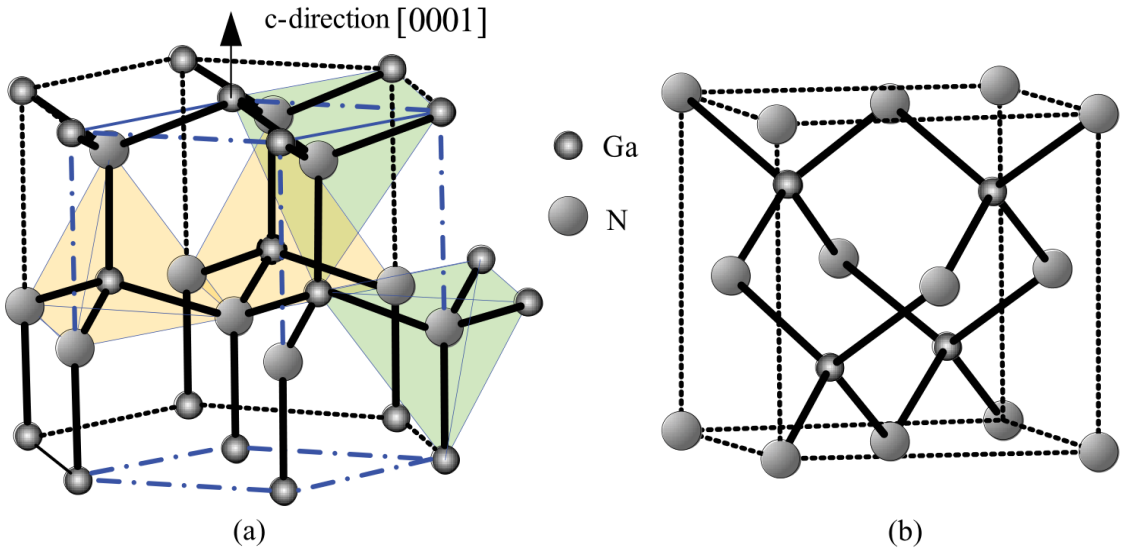


Figure 1- 2 Illustration of (a) wurtzite structure and (b) zincblende lattice [19].

§1.2.2 Material properties of GaN

The bandgap of GaN (wurtzite structure) is 3.4 eV, it's three times than Si of 1.1 eV [4-6]. It determines that the GaN-based has higher breakdown voltage and could operation at higher temperature ambient than Si-based [7-8]. The high electron velocity characteristics make GaN devices operate at high frequency as well. Besides, the GaN as wide bandgap material has also an importance role in optoelectronics field, such as luminescent device and optoelectronics detectors [9-11]. Table 1.1 summarized the material properties of GaN and other semiconductor.

Table 1.1 Material properties of GaN and other semiconductors [12]

Material properties	GaN	GaN	Si	GaAs	4H-SiC
Crystal structure	Wurtzite	Zincblend	Diamond	Zincblend	Hexagon
E_g (300K)	3.39	3.2	1.12	1.42	3.23
E_B (MV/cm)	5	5	0.25-0.8	0.3-0.9	3-5
μ_n ($cm^2v^{-1}s^{-1}$)	≤1000	≤1000	1450	8000	≤900
μ_p ($cm^2v^{-1}s^{-1}$)	≤200	≤350	500	400	≤120
V_s (10^7cm/s)	2.5	2.5	1	0.7	1.9
n_i (cm^{-3}) 300K	3.85×10^{-10}	1.04×10^{-8}	9.65×10^{9}	2.1×10^{6}	8.2×10^{-9}

E_g: bandgap, E_B: breakdown field, μ_n : electron mobility, μ_p : hole mobility, V_s : saturation electron velocity, n_i : intrinsic carrier concentration.

The unique feature of the GaN-based semiconductor is the two dimensional electron gas (2DEG) in a quantum well at the interface of the heterostructure [13]. The heterostructure is generally presented between intrinsic GaN (i-GaN) and GaN alloy. Aluminum gallium nitride (AlGaN) is the most commonly alloy that its bandgap is function of Al mole fraction in $Al_xGa_{1-x}N$. Different with 2DEG in AlGaAs/GaAs heterosturture, which the 2DEG is formed by the doping in AlGaAs and GaAs [14]. Due to their piezoelectric polarization and spontaneous polarization as shown in Fig. 1-3, AlGaN/GaN heterostructure possess high density 2DEG up to 1×10^{13} cm^{-2} without intentional doping [15]. The band structure is modulated by the polarization effects while the quantum well of GaN side deep and narrow This makes it possible to realize a low on-state resistance (R_{on}) as its transistor characteristic. The 2DEG lead the AlGaN/GaN heterostructure device has the high electron mobility and lead the good ohmic contact [16].

Now, AlGaN/GaN heterostructure field-effect transistors (HFETs) have become one of the most promising solid-state microwave power devices because of their ability to generate higher power densities at higher frequencies [17-22]. On the other hand, high-frequency GaN HFET is an essential component for power amplifiers systems, which need high-output-power and high-efficiency performance [23-26]. Thanks to its high-output-power performance, GaN HFET can achieve 110W or higher with just a single device, making high-efficiency and power-saving power amplification possible [27].

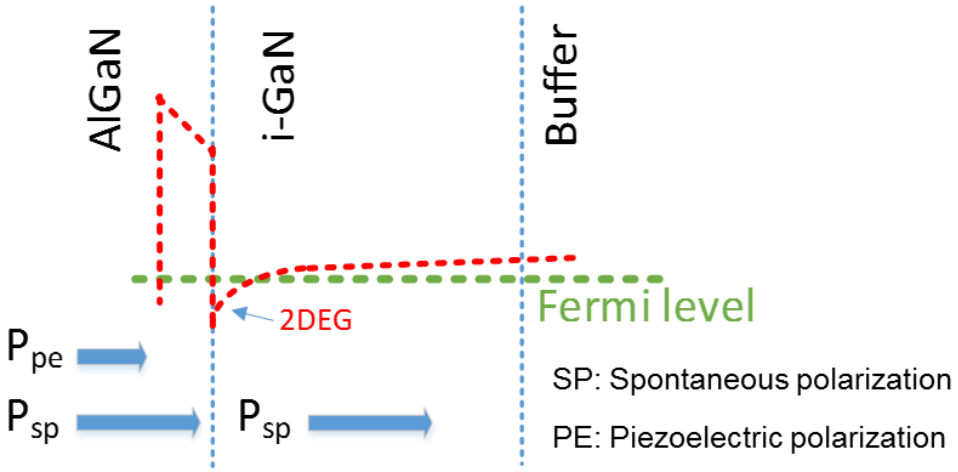


Figure 1- 3 The applications of GaN devices in power electronics field.

§1.2.3 Epitaxial growth of GaN

By the decades of development, silicon as the first generation semiconductor material has reached its material limitation. The second generation semiconductor material specifically refer to GaAs materials has been also commercial for many years. And with the progress of the human society, the higher demands for electric devices are presented. The wide bandgap of GaN material as a representative of the third generation semiconductor is researched. The epitaxy growth and investigation of GaN has been more than eighty years, since the first reported on the synthesis of GaN via the reaction of metallic Ga and NH_3 stream in 1932 by Johnson *et al* [28]. At the early years, only the GaN powder and single crystalline GaN needles can be obtained by growth. By the scientific-technical progress, the epitaxial equipment has the great progress that is from previous reactive sputtering to metal organic chemical vapor deposition (CVD) and Hydride vapor phase epitaxy (HVPE) now [29, 30]. Due to the shallow donors of substitutional Si, O impurities and the native N vacancies during the crystal growth, the unintentional doped GaN exhibits the high n-type background doping concentrations of 10^{15}-10^{17} cm^{-3}. For compensating the native background doping, the p-type doping is needed. By the development of years, the C and Fe as acceptor are introduce. Meanwhile, the semi-insulating GaN (SI-GaN) with high resistance is also achieved [31-34]. In 1991, the p-type GaN was proposed with the high concentration Mg-doping using MOCVD [35].

Considering the limited availability and relatively high cost of GaN substrates as shown in table 1.2, GaN epitaxial growth are generally proposed on foreign substrates, such as sapphire (Al_2O_3), silicon carbide (SiC), and silicon (Si) [36]. GaN-on-sapphire substrate technology is very mature and is the mainstream in the light-emitting diode (LED) market, but it's unsuitable for power applications due to the poor thermal conductivity of sapphire [37]. However, 6H-SiC and Si are also popular substrates, the 6H-SiC has a low lattice mismatch, good electrical conductivity and low film stress; the Si has large wafer size, low cost and integration of Si devices [38-40]. Now, the substrate of sapphire, SiC and Si have been commercial available, which is applied in different fields. Among the various substrate materials, a Si substrate due to the large scale and low cost especially attracts the attentions from GaN-based device, which owing to decades of

development of the Si semiconductor industry [42-43].

Table 1.2 Material properties of substrates [36, 41]

Material properties	GaN	Si	Sapphire	SiC
Lattice parameters (Å)	*a*=3.1891	*a*=5.431	*a*=4.765	*a*=3.081
	c=5.1855		*c*=12.982	*c*=15.117
Lattice constant mismatch to GaN	/	17%	15%	3.51%
TEC* (10^{-6} K^{-1})	5.6	3.59	7.5	4.2
Thermal conductivity (W cm^{-1} K^{-1})	1.3	1.56	0.25	3.8-4.9
Dislocation density	/	$>10^9$ cm^{-2}	$>10^8$ cm^{-2}	$>10^8$ cm^{-2}
Diameter (inches)	2-4	2-12	2-6	2-6
Cost	More expensive	Cheap	Less expensive	Expensive

*TEC: Thermal expansion coefficient

§1.2.4 AlGaN/GaN heterostructure HFET

The epitaxial structure of conventional AlGaN/GaN heterostructure field-effect transistor (HFET) is shown in Fig. 1-4. To utilize the characteristic of the 2DEG, the AlGaN/GaN HFETs exhibit the great performance, while this kind of HFET is also named the high electron mobility transistors (HEMTs). The mobility of AlGaN/GaN HFET is confirmed to around 2000 $cm^2v^{-1}s^{-1}$ [44], which is depend on the 2DEG characteristics.

Since the M. A. Khan et al reported the first GaN metal semiconductor field-effect transistor (MESFET) [45], GaN-based HFET technology has a great improvement. For example, the ohmic formation of AlGaN/GaN heterostructure adopt generally the Ti/Al as the contact layer and high temperature annealing [46]. Many high performance HFETs were reported. To utilize the free-standing GaN wafer, the high epitaxy quality and a low SS of 60 mV/dec was achieved by X. K. Liu et al [47]. J. Lee et al fabricated the T-gate HFET with a transconductance of 146 mS/mm, cutoff frequency of 38 GHz and a max oscillation frequency of 130 GHz [48]. And the high-temperature performance of AlGaN/GaN was fabricated on SiC substrate by R. Gaska et al, that is with 0.95A/mm source-drain current and maximum dissipated DC power of 0.6 MW/cm/sup 2 [49]. The passivation layer and the adoption of field-plate structure significantly alleviate the current collapse and increase the breakdown voltage [50-52].

However, the normally-on characteristics is commonly observed for HFETs which owing to the turn-on of 2DEG channel in zero bias voltage [53]. And the threshold voltage (V_{th}) of the conventional AlGaN/GaN HFETs is almost less than 0V. Therefore, it leads to many drawbacks in practical circuit, such as high consumption, potential safety risk, inherent failsafe operation and complicate circuit configuration [54-58]. Therefore, the normally-off operation is required.

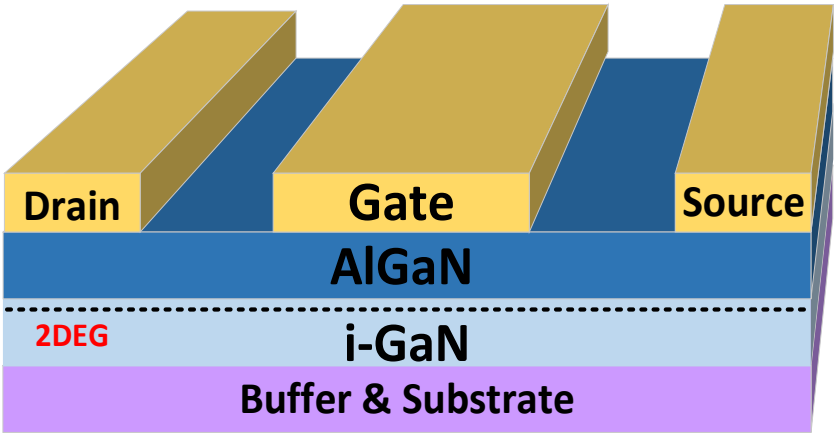


Figure 1- 4 The epitaxy structure of conventional HFETs.

§1.3. Mechanism of the normally-off characteristic by p-GaN layer

As known, the most unique property of AlGaN/GaN heterostructure is the existing of high density 2DEG in a quantum well along a heterojunction which the 2DEG in AlGaN/GaN heterojunction is induced by polarization effects. The polarization effects cause extremely strong electric field within the heterojunction, which would modulate the band structure and make the quantum well of GaN side deep and narrow, and this is benefit to attract and accumulate free electrons into the well.

However, for the purpose of achieving the normally-off operation, the 2DEG need to be efficiently depleted and achieve a reasonable threshold voltage V_{th}. On the other hand, many methods for normally-off operation is also to deplete the 2DEG at the gate voltage of 0 V. Among kinds of methods, the p-GaN cap layer is the most effective method. As shown in the Fig. 1-5, due to the p-type doping, the Fermi level of the p-type GaN is more closed to the value level. Moreover, when the p-GaN closed to the AlGaN/GaN heterostruture, the energy band of the 2DEG channel is raised above the conduction level. Therefore, the 2DEG is depleted by the p-GaN cap layer.

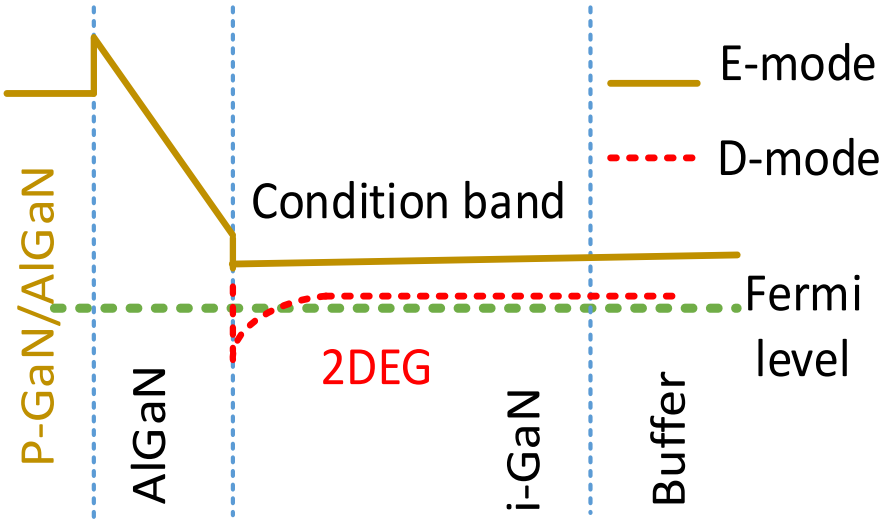


Figure 1-5 the energy band diagram of E-mode and D-mode.

On the other hand, the mechanism of the depleted 2DEG could to be also expressed by the P-N junction theory [59]. Owing to the p-type doping of p-GaN layer and the high density 2DEG, the p-GaN/AlGaN/GaN HFET structure can be seen as a P^+-N junction. So the built-in field can be formed around the p-GaN/AlGaN which is due to the electrons drift and diffusion. Furthermore, we know the built-in field direction is reversed to that of P-N junction. The depletion layer is existing in both sides. And as a P^+-N junction, the non-doping side has the more wide depletion layer. So the 2DEG is depleted by the built-in field of the P-N junction.

The GaN-based power transistors can be applied at power amplification field as linear device and electricity conversion field as power switching, and the representative devices are AlGaN/GaN heterostructure field-effect transistor (HFET) and metal oxide semiconductor field-effect transistor (MOSFET), respectively. After more than 20 year's efforts, significant progress in development of GaN-based field-effect transistors (FETs) has been achieved.

§1.3.1 Normally-off GaN MISFET with gate recess

Compared the large leakage current of Schottky gate for conventional AlGaN/GaN HFETs, the low gate leakage current contributes to improve low-frequency noise [60]. To suppress the gate leakage current and increase the breakdown voltage, the MOS gate was firstly fabricated by F. Ren et al using a Ga_2O_3 film [61]. For the decade year development,

varied oxidation is applied as the gate dielectric layer while the better breakdown and leakage characteristics is achieved [62-64].

However, the normally-on operation is always obstacle for the further development of GaN-based HFETs. Many groups focus on the researching of the recess-gate structure, which purpose is reduction the 2DEG underneath the gate region by removing the AlGaN barrier layer [65-66]. Meanwhile, the MOS channel is also combined to the recess-gate structure as shown in Fig. 1-6. This kind of MOS-HFET is benefit for control the V_{th} by the recess depth, while the gate leakage current is also suppressed at a low level. Some group had achieved the relatively high V_{th} and mobility [67-69]. Nevertheless, for the removing AlGaN barrier process, the contamination and damage are introduced by ICP dry etching [70]. This is another critical issue for reaching the positive V_{th}. The low bias dry etching is purposed to alleviate the damage, Wang Q et al fabricated a MOS-HFETs with a V_{th} of 0.1 V and mobility of 148 $cm^2V^{-1}s^{-1}$ by using the 100/20 W ICP/Bias recipe [71]. Ye Wang et al reported a normally-off Al_2O_3 gate-recessed MOSFET using a low-damage digital recess technique. The 8 V of V_{th} and 251 $cm^2V^{-1}s^{-1}$ is obtained [72]. And the J. S. Lee et al utilize the photo-electrochemical gate recess etching to fabricate AlGaN/GaN HFET, the approach is also obtain a low damage surface [73].

On the other hand, the selection of the oxide dielectric layer is another key for the device performance. At early stage, the Ga_2O_3 and SiO_2 as the dielectric layer are investigated in some group [74-75]. Recently, due to the high quality deposition by atomic layer deposition (ALD), the Al_2O_3 was commonly developed for a normally-off operation [76].

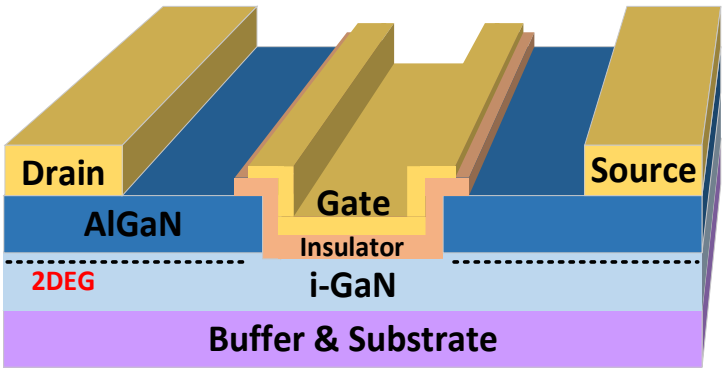


Figure 1- 6 MIS-HFET with gate recess process

§1.3.2 Normally-off GaN HFET with thin AlGaN barrier

For the AlGaN/GaN heterostructure HFETs, the Ni/Au is the commonly gate metal. However, the conduction band offset formed by metal Ni with AlGaN layer is not sufficient to deplete the 2DEG which is induced by the AlGaN of conventional thickness. According to the mechanism of the 2DEG, the 2DEG density depends linearly on thickness of AlGaN layer within a certain range. To consider the ICP damage in dry etching process, the thin AlGaN barrier HFETs have more benefits for normally-off operation as shown in Fig. 1-7.

T. Hashizume et al realize the quasi normally-off HFETs with less than 10 nm AlGaN layer and a V_{th} of -0.3 V [77]. By combining the Al_2O_3 insulated-gate, the gate sweep is up to 4 V without leakage problems. Y. H. Wen et al fabricated the normally-off AlGaN/GaN heterostructure HFETs with 10 nm AlGaN barrier layer. They use the selective area growth technique to achieve a good ohmic contact on SD region. The HFETs exhibits a good performance of peak transconductance of 135 mS/mm with a V_{th} of 0.4 V [78]. The normally-off HFETs with 10 nm AlGaN barrier layer is reported by H. C. Chiu et al [79]. A V_{th} of 0.5 V and high transconductance are observed with TiW gate compare to the conventional Ni/AlGaN Schottky gate.

On the other hand, the AlGaN/GaN heterostructure is also applied for high frequency applications [80-82]. The thin AlGaN barrier thickness is key to enhance high frequency characteristics [83-85]. L. Yang et al utilize the thin barrier AlGaN/GaN HFETs by TiN-based source contact ledge enhancing g_m to 415 mS/mm and power-gain cutoff f_T to 110 GHz [86]. And the Johnson's figures of merit (J-FOM = $BV_{GD} \times f_T$) is 10.4 THz-V, which is the highest record so far.

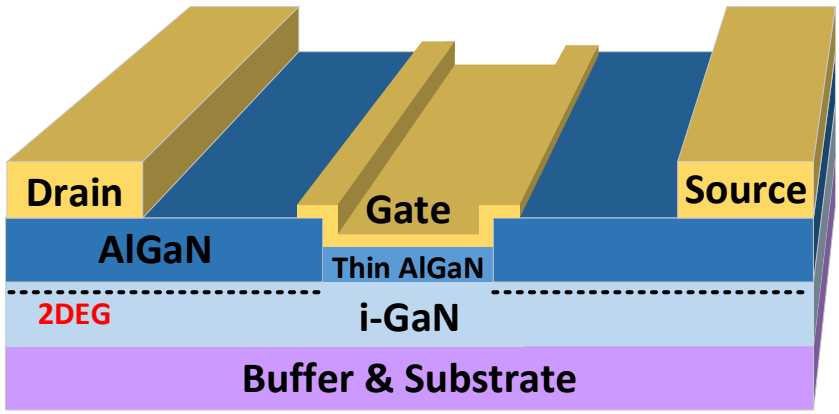


Figure 1- 7 Thin AlGaN barrier HFET assisted by selective region growth

§1.3.3 Noramlly-off GaN HFET with F^- ion implantation

For avoiding the dry etching damage by ICP, an alternative approach of normally-off operation is developed as shown in Fig. 1-8. Due to the strong electronegativity, the F^- ion can effectively raise the potential in AlGaN barrier and deplete the 2DEG channel. And the V_{th} can be modulated by F^- ion implanted during the plasma treatment. Consequently, the normally-off operation can be fabricated [87]. The method of F^- ion implanted is widely researching which is owing to the merits such as good repeatability, high saturation current and transconductance.

Y. Cai et al demonstrate the control of V_{th} of AlGaN/GaN HFETs by fluoride plasma treatment [88]. The V_{th} can be continuously shifted from -4 to 0.9 V, it shows a good thermal stability. And the plasma-induced damage can be repaired by a post-gate annealing at 400 ºC. A V_{th} of 3.6 V and specific on-resistance of 2.1 $m\Omega \cdot cm^2$ are exhibited in AlGaN/GaN HFETs with MIS gate structure by SiN_x [89]. Due to the F^- ion implantation and SiN_x dielectric layer, both the V_{th} and the gate swing has a great improvement, respectively. In HFETs device structure, the insulator can be as the gate dielectric while it features energy-absorbing layer that slows down the high energy F^- ion to reduce the implantation damage [90]. This method combining the F^- ion implantation and dielectric layer is also applied by C. Chen et al [91]. They combine the F^- ion implantation and Al_2O_3 layer to realize the V_{th} shifting from -4.8 to 0.11 V. And the normally-off HFETs exhibit a high transconductance of 153 mS/mm and saturated current of 547 mA/mm. This pave a new way to integrate the normally-off/on HFETs for analog integrated circuits.

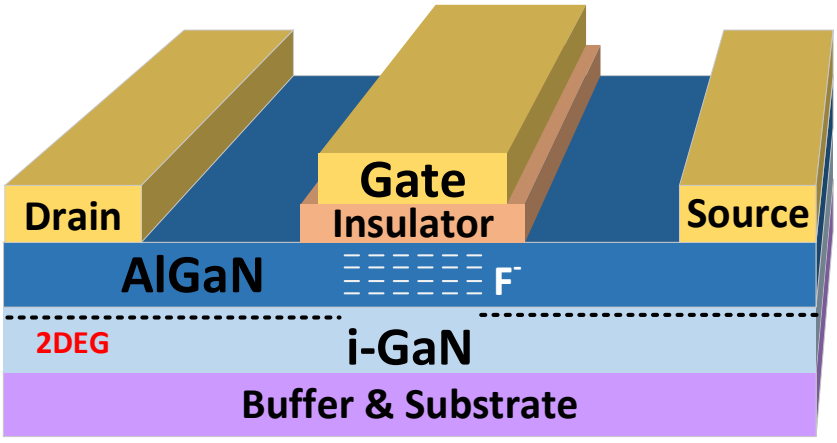


Figure 1- 8 MIS-HFET with F^- ion implantation

§1.3.4 Noramlly-off GaN HFET with Fin gate

By the utilizing of the electron beam (EB) lithography, the fin-shaped gate in GaN-based HFETs is investigated as a promising candidate for high performance normally-off GaN MOS-FETs. When the width of gate is thin enough, the channel can be turned off through the side-gate and top-gate. And the FinFETs have the more broad g_m characteristics than typical planar-type HFETs. For GaN-based FinFETs, several research groups have reported methods of achieving normally-off operation using the AlGaN/GaN based tri-gate FinFETs as shown in Fig. 1-9 [92].

D. S. Kim et al utilized the electron-beam lithography and dry etching to fabricate the fin-shaped gate which is a height of 120 nm and a width of 50-80 nm [93]. Number of fins in parallel success pinch-off the channel, the V_{th} of 4.2 V and transconductance of 662 mS/mm are confirmed. L. C. Chang et al reported that the relationship between fin width and V_{th} [94]. They exhibit that the normally-off operation can be realized when the fin width is less than 100 nm. And Y. W. Jo utilized the EB lithography and wet etching to fabricate fin-shaped gate with very steep side-wall [95]. The HFETs demonstrate extremely broad transconductance ranging from 0-8 V at drain of 10 V, which is essential for high linearity device performance. A low leakage normally-off fin-gate GaN-based MISFET was fabricated by B. Lu et al [96]. The fin-gate shows a very low off-state drain leakage current of 0.6 μA/mm at a breakdown voltage of 565 V, while maintains a low on-resistance of 2.1 mΩ·cm^2 and V_{th} of 0.8 V. On the other hand, K. S. Im et al fabricated a GaN HFETs with deep-submicron gate length [97]. The HFETs with a gate length of 350 nm shows a maximum cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are 2.45 and 9.75 GHz.

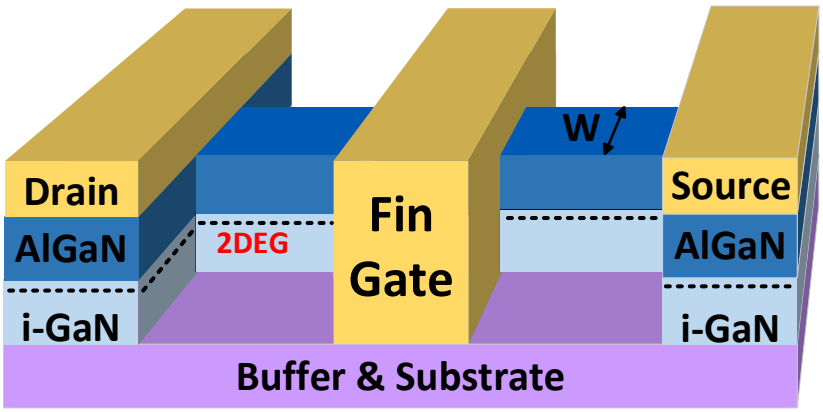


Figure 1- 9 Fin-HFET with three dimensional (3D) gate

§1.3.5 Advances of P-GaN gate in Noramlly-off GaN HFETs

Some groups have reported several methods to obtain normally-off GaN-based HFETs. In general, the 2DEG can be depleted under a thin AlGaN barrier layer with a low Al concentration. However, to consider for the device R_{ON}, the 2DEG channel at access region must keep turn-on, and the 2DEG channel below the gate region should be able to completely restore the sheet carrier density through applying a positive gate bias.

Hence, a recessed-gate structure as the first approach to purpose for the normally-off GaN HFET has been studied by selective etching the AlGaN barrier layer by ICP plasma dry etching process [98]. It's well-know that the precise control of the AlGaN etching process is required in this approach. In addition, the damage induced by the etching process need to be considered which could lead to high gate leakage current and V_{th} non-uniformity effects. Therefore, to improve the V_{th} uniformity and obtaining a low R_{ON}, a novel partial recession of a barrier layer composed by several AlGaN layers with different Al concentration has been researched [99]. Moreover, based on the partial recession, the introduction of p-type oxidation is an alternative approaches to obtain normally-off operation [100].

On the other hand, the fluorine ion implantation on the gate region has been also utilized to achieve normally-off operation. In this case, the F^- ions as negative charge is introduced either by plasma etch or ion-implantation [88], which depletes the 2DEG channel, thus leading to a positive shift of threshold voltage V_{th} of the transistor. However, the V_{th} stability after high temperature annealing can be a concern in this kind of device [101].

Recently, the Fin-shaped FETs as an alternative approach to obtain normally-off also attract widely attentions. However, the Fin-shaped FETs need the complex process and more precise EB photolithography, that more researching is essential before practical application.

Now, the most promising approach is the utilizing a p-GaN (or p-AlGaN) cap layer upon the AlGaN/GaN heterostructure at the gate region as shown in Fig. 1-10 [102]. The p-GaN layer lifts up the conduction band, resulting in the depletion of the 2DEG channel even in the absence of an external applied bias (V_G of 0 V). This structure is receiving a great attention, as a matter of fact, the p-GaN gate becomes the normally-off GaN HFET

which is only commercially available to date. Obviously, the technology of normally-off HFETs with p-GaN is further developed, and the device structure can be greatly influenced by several layout and processing conditions.

Y. Uemoto et al analyzed the mechanism of normally-off operation and firstly propose the conception of hole injection [102]. J. Kim et al reported a V_{th} of 2.8 V p-GaN gate power devices on 200 nm Si substrate by TO-220 packaged [103]. Obviously, there are some important issues about reliability, which need to be analyzed such as V_{th} stability [104, 105], charge trapping mechanisms [106], degradation processes induced by positive gate bias [104] or induced by high drain bias in off-state [106].

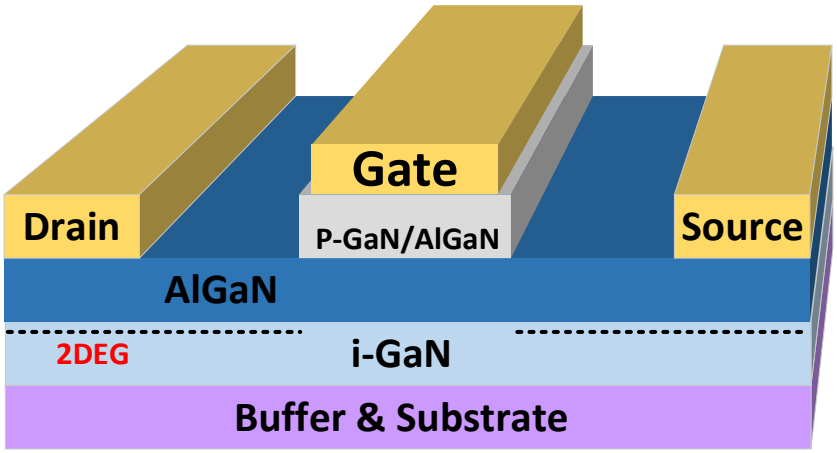


Figure 1- 10 Juntion-FET (JFET) with P-GaN/AlGaN cap layer

§1.4 Motivation of this research

1. Motivation

The wide bandgap semiconductor materials (such as diamond, SiC and GaN) had been under extensive academic research for more than 20 years and promise to replace silicon with better energy efficiency. While silicon IGBT and PiN diodes remain a primary choice for automotive power modules, large power electronics makers are already interested in emerging technologies that enable higher power conversion efficiency or reduced system cost. GaN semiconductor is one of the most anticipated candidates for the next-generation power electronics applications. However, the negative gate voltage is drawback for the AlGaN/GaN heterostructure HFET devices in practical applications. This leads to the disadvantage of complicate circuit design. On the other hand, the safety issues is also

need to be considered due to the normally-on operation. Moreover, in some power switching applications, devices with high V_{th} (e.g. >6V) and large gate swing (e.g. >10V) are required to prevent the devices from faulty turn-on that is induced by the electromagnetic interference or failure of gate driver.

So the normally-off characteristics are required for power switching applications to guarantee a safe operation and a simple gate drive configuration. Many methods have been adopted to realize the normally-off AlGaN/GaN HEMTs. Among these methods, the p-GaN gate structure is the unique commercially available “real” normally-off GaN HEMTs to date because of its excellent figure of-merits and robust normally-off operation.

2. Objectives

This thesis investigates the normally-off operation for AlGaN/GaN heterostructure HFETs. To the conventional AlGaN/GaN HFETs, the p-GaN cap layer as the most promising approach can effectively deplete the 2DEG channel by raising the conduction band upon the Fermi level underneath the gate region. Based on the normally-off operation, to investigate the mechanism of the normally-off operation by the p-GaN cap layer. For the p-GaN gate device, the relationship between V_{th} and i-GaN thickness (inserting into p-GaN and AlGaN) is investigated, and the blocking feature of i-GaN layer is confirmed. For the MIS-HFETs with p-GaN layer, the influence of SiN_x as dielectric layer to V_{th} was evaluated. Then, by optimizing the device structure is to improve the device performance and threshold voltage. For reducing the turn-on resistance, the self-aligned-gate (SAG) was fabricated, while the low temperature ohmic was also achieved. The performance of SAG gate was analyzed, the results exhibited that the MIS-HFET with SAG p-GaN gate is an efficiently method to develop as power device.

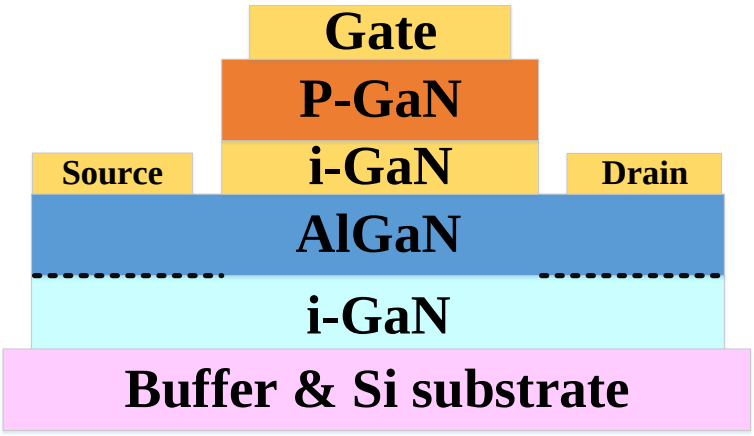
Chapter 2： Fabrication Process, test methods and evaluation technology of Normally-off p-GaN gate HFETs

§2.1. Fabrication process of the normally-off HFET with p-GaN gate

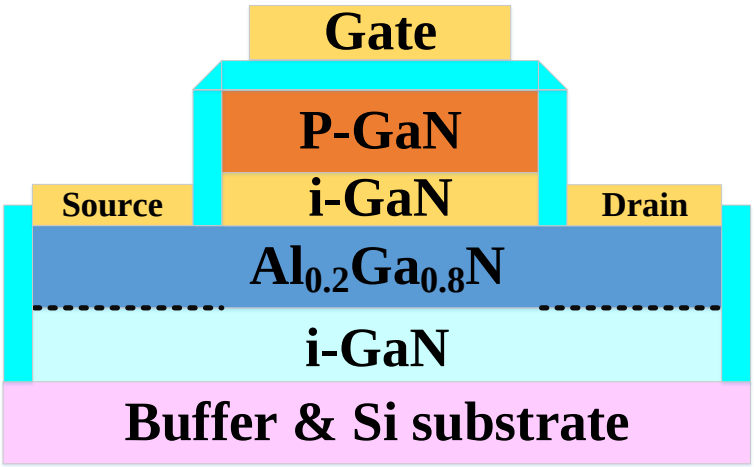
§2.1.1. Structure of the HFET with p-GaN gate

In conventional HFET with p-GaN gate shown in Fig. 2-1a, the source and drain ohmic contacts are realized after removing the p-GaN layer above the SD region and then the 2DEG is formed as a consequence. Moreover, the channel is formed by applying the positive gate voltage, and the 2DEG can be depleted by the p-GaN layer at equilibrium condition in gate region.

The gate length L_g of the device is 94 μm, the gate efficient width W_g is 819 μm, and the spacing between source/drain electrode and gate electrode is 6 μm (Fig. 2-1d). There are several different gate structures like MIS-gate, SAG MIS-gate (Fig. 2-1 b and c). And due to the different gate structures, the spacing between source/drain electrode and gate electrode have a difference with each other.



(a)



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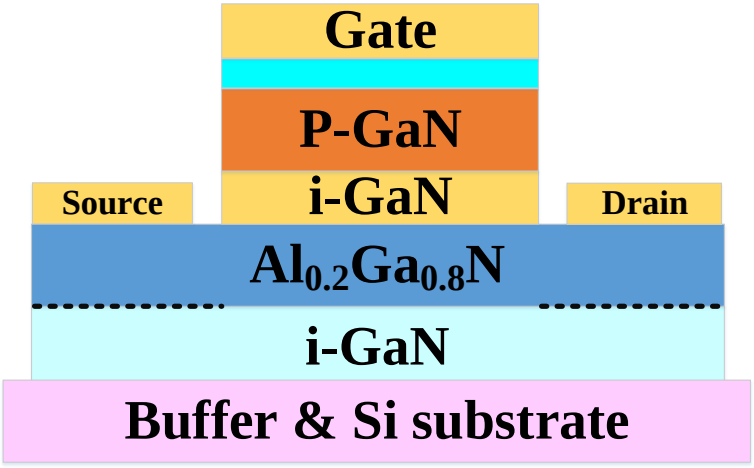

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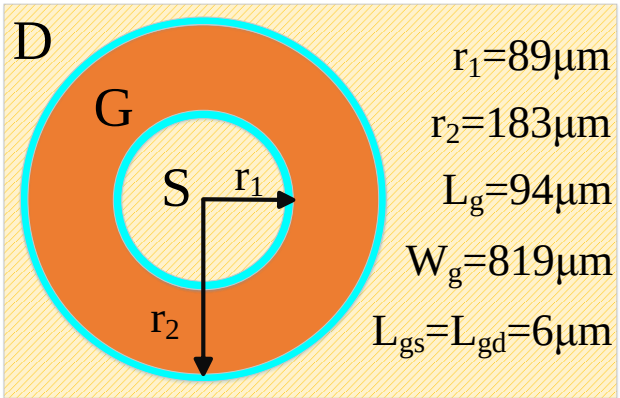


(d)

Fig. 2-1 The cross section of p-GaN gate (a), MIS-gate (b) and SAG MIS-gate (c) and bird view of the device structures with p-GaN gate.

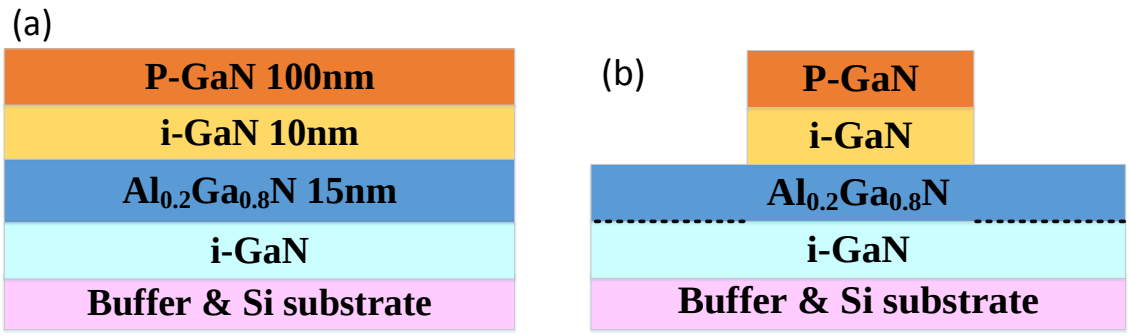
§2.1.2. Epitaxy structure of the HFET with p-GaN gate

Except for the p-GaN cap layer, the remaining epitaxy structure is similar with the conventional AlGaN/GaN heterostructure HFETs. The AlGaN and GaN are as the barrier layer and channel layer, respectively. The AlGaN layer has a great influence on 2DEG. Dislike the conventional Al content and thickness in AlGaN layer, the low Al component and thin AlGaN barrier layer are generally adopted in normally-off operation device with p-GaN gate.

For p-type GaN, the Mg^{+} doping is the most commonly adopted as the acceptor in p-type doping with a high doping concentration. It's due to the low hole concentration resulted from the low activation rate of Mg^{+} doping in p-type GaN. However, because of the self-compensation effects [107], the increasing Mg concentration doesn't lead an increasing hole concentration. For GaN, there is a maximum for an Mg concentration. When increasing the Mg concentration beyond this value, the hole density drops rapidly. On the other hand, to consider the wafer epitaxy quality, the doping concentration of the Mg^{+} is kept around 10^{19} -10^{20} cm^{-3}. And for the simplification of the epitaxy growth process, the in-situ epitaxy growth method is adopted during p-GaN cap layer growth. Of course, for achieving some special purpose, the complicated second epitaxy technique is also used in the device fabrication.

§2.1.3. Process flow of the HFET with p-GaN cap layer

According from the GaN HFETs fabrication process, the conventional p-GaN gate AlGaN/GaN HFETs processing schemes often proceed through a sequence of (a) wafer cleaning, (b) p-GaN gate defining, (c) mesa isolation, (d) ohmic metallization and annealing, (e) gate and contact pad metallization, as shown in Fig. 2-2.



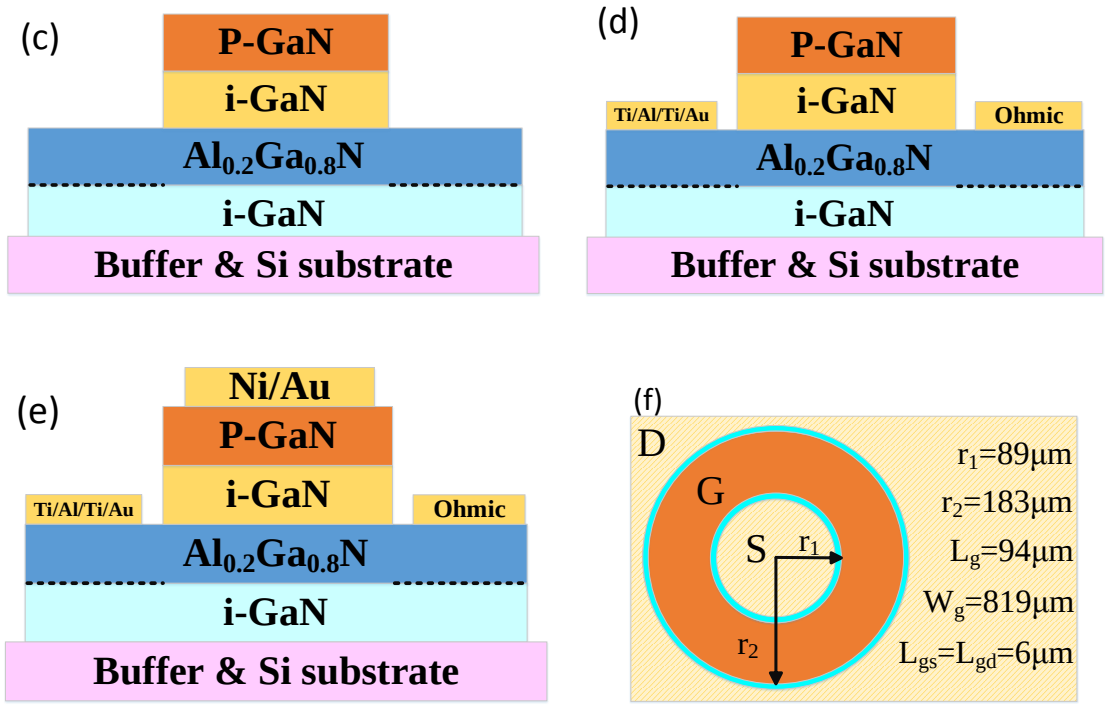


Fig. 2-2 The fabrication process flow of AlGaN/GaN HFET with p-GaN gate, (a) wafer cleaning, (b) p-GaN gate defining, (c) Meas isolation, (d) Ohmic metallization and annealing, (e) Gate and contact pad metallization.

The fabrication process is based on the standard photolithography and lift-off technologies. The detailed instruction of each process will be introduced.

(a) Wafer cleaning

The wafer is cleaned by SPM solution (H_2SO_4:H_2O_2=4:1, volume ratio) and heated at 100 ^oC for 10 min, cleaned with deionized (DI) water and blow-dry using nitrogen gun. And following by rinsing in organic solution in sequence. The wafer is dipped in the acetone solution and heated, then ultrasonic cleaner for a few minutes. Finally, the wafer was rinsed by methanol, and DI water in sequence.

(b) P-GaN gate defining

During the p-GaN gate HFETs fabrication, the p-GaN gate defining is a key step. To prevent the two etching in following Mesa isolation process, the p-GaN gate defining is done before the Mesa isolation. According to the epitaxy structure, the residual 2-3 nm thickness need to be retained before reaching the AlGaN layer. The etching rate need to

be accurate controlling.

For reducing the ICP damage and alleviating the degradation of the AlGaN surface during etching process, a low damage recipe with ICP/bias power of 100/20 W was adopted with the $SiCl_4$ etching gas [70]. The $SiCl_4$ gas is with a flow rate of 4 sccm and chamber pressure of 0.5 Pa. A low average etching rate of approximately 1.88 nm/min was measured by atomic force microscope, which can lead an accurate control of p-GaN etching. At the same time, the 2DEG is revived at access region.

In our experiments, an ICP system–RIE-200-iPG (from SAMCO, Inc., Fushimi, Kyoto, Japan) was implemented with a $SiCl_4$ gas and a Cl_2 gas. Fig. 2-3 shows the internal components of the equipment. Inductively coupled coils generates plasma and the plasma density is controlled by ICP power. The bias power controlled the speed that plasma move towards sample, a higher bias power means a stronger ion bombardment on the sample. A helium gas was used for cooling to keep the sample stage at room temperature during the etching process. Usually, a 1.5-2 μm positive photoresist (AZ-4210, Clariant Corp.) layer is used as the etching mask.

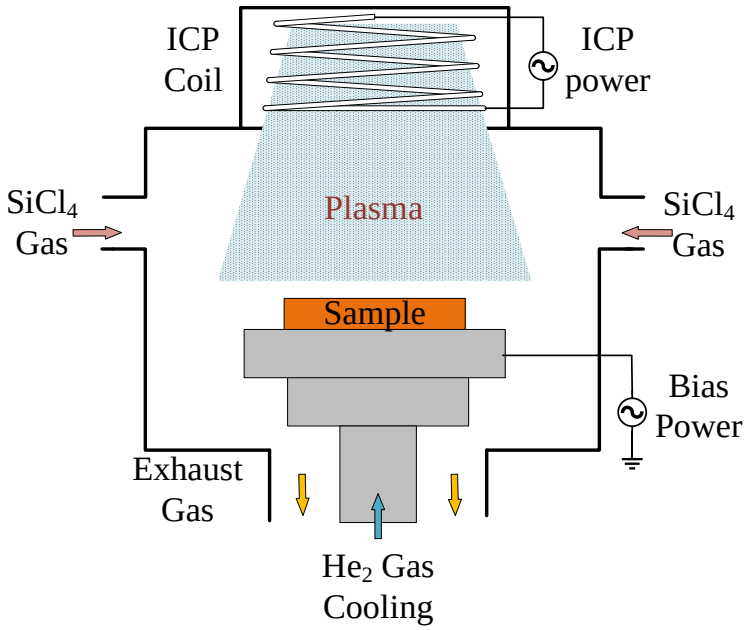


Fig. 2-3 Schematic of internal components in the ICP system.

(c) Mesa isolation.

Mesa isolation is formed by ICP dry etching. Due to the characteristics of GaN crystal

structure, the most common etching method for GaN-based is inductively coupled plasma (ICP) etching which is due to high-density plasma and high uniformity over large areas, lower ion bombardment energy relative to RIE, and lack of electromagnets and waveguides required for electron cyclotron resonance (ECR). After 100 nm device isolation by the dry etching with the ICP, surface treatment was done by immersing the wafers in the HNO_3/HF for 10 min to clean the possible Si contamination on the etched surface.

(d) Ohmic metallization and annealing.

The ohmic contact for AlGaN/GaN heterostructure is usually adopted the Ti/Al/x/Au metal stacks deposited on the AlGaN surface in sequence, where x may be Ti, Ni, Pt, Mo or Pd. Each one of metal layers play a definite role. The ohmic contact is formed at annealing temperature of more than 800 ^{o}C. During the annealing process, the N vacancy is formed which owing to the good conductor TiN is comprised by Ti and N in AlGaN. The N vacancy is benefit for the ohmic contact. On the other hand, due to the 600 ^{o}C melt temperature of Al metal, the ohmic electrode has a rough surface after annealing as shown in Fig. 2-4.

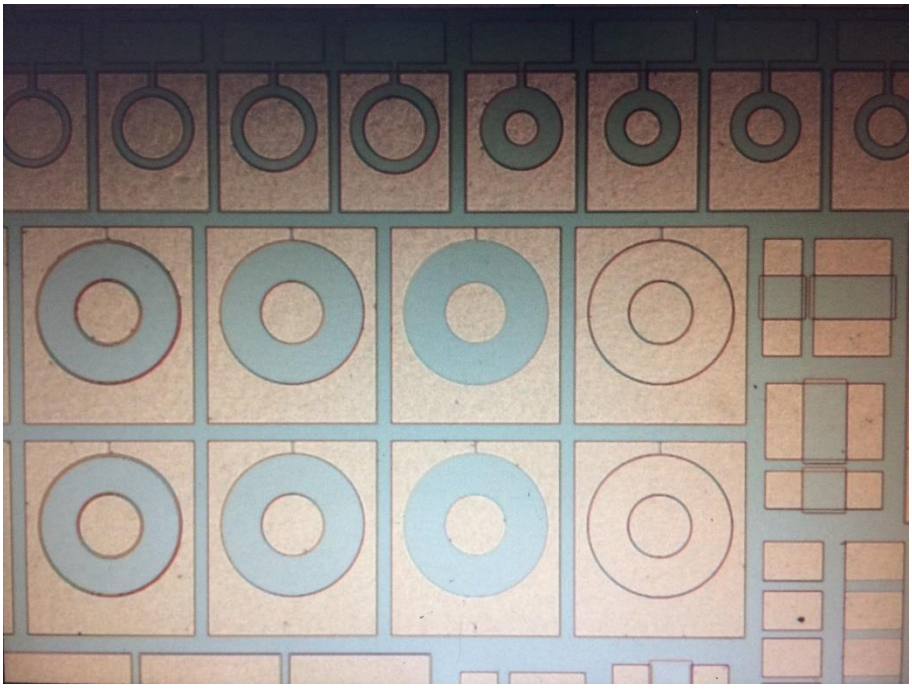


Fig. 2-4 Picture of the ohmic electrode after 850 ^{o}C.

The ohmic contact on the p-GaN gate HFETs is related to the ICP etching depth. If the etching depth is less or more, there is a great effort to the ohmic contact. In our experiment, a Ti/Al/Ti/Au (50/200/40/40 nm) is adopted as ohmic electrode by the sputtering (ALVAC MNS-2000-RF-HS). And the standard lift-off technology is implemented, and annealing process is carried out at 850 ^{o}C for 3 min in N_2 ambient by rapid temperature annealing (RTA). However, due to adopt the thin AlGaN barrier layer and low Al content in p-GaN gate HFETs, the ohmic contact results are less than that of the conventional AlGaN/GaN heterstructure HFETs with about 25 nm AlGaN barrier. As shown in Fig. 2-5, with a 20nm $Al_{0.2}GaN$ barrier layer in p-GaN gate HFETs, the ohmic contact results are derived by the transmission line model (TLM).

On the other hand, the gate first process is developed for improving the device performance. However, the common ohmic process need the high temperature annealing above 800 ^{o}C, it is easy to cause the gate degradation. So the heat-resisting metal materials and low temperature ohmic are the developing directions for gate-first. Recently, the low temperature (below the 600 ^{o}C) ohmic technology is reported in gate-first process. It is also alternative method to develop the ohmic contact for the normally-off p-GaN gate HFETs. The low temperature ohmic process is mainly assisted by the N vacancy generated by the ICP plasma treatment. Previously the ohmic metal depletion, the SD region is treated by the ICP plasma on after removing the p-GaN layer. Then, the relative low ohmic annealing at 500 ^{o}C is processed for 20 min in N_2 ambient. The result ohmic contact exhibits a great improvement than the common ohmic contact at high temperature. The experimental details would be discussed in subsequent section.

(e) Gate and contact pad metallization

Similar to the most AlGaN/GaN HFETs, Ni/Au bi-layer as the common gate electrode is also utilized in p-GaN gate HFETs due to good electrical properties and adhesion to the AlGaN surface. Before the gate metal deposition process, the possible oxide layer was removed by the diluted HCl ($HCl:H_2O=1:1$) solution for 5 min after the lithography process. For the higher device performance, Ni/Au (10/10 nm) was deposited as the gate metal and annealing in O_2 ambient for 10 min in out experiments, which is to form the similar ohmic contact with the p-GaN gate. Finally, Ni/Au (70/30 nm) was deposited as the gate metal pad, and the post-annealing of 300 ^{o}C for 10 min in N_2 ambient is done. Fig. 2-6 shows a picture of AlGaN/GaN HFETs after finishing the gate metallization.

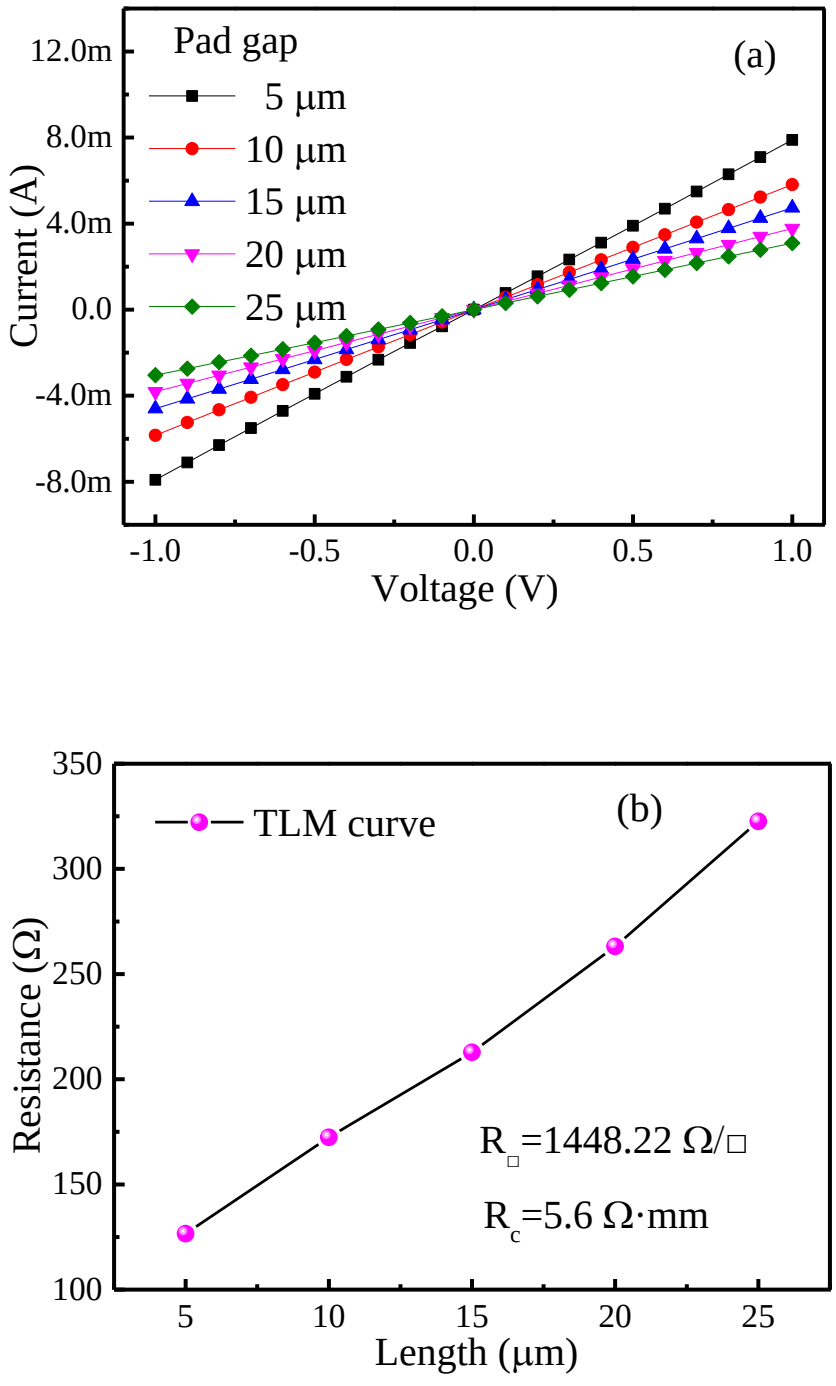


Fig. 2-5 Ohmic contact results of (a) ohmic electrodes current-voltage (I-V) curve and (b) Ohmic contact results calculated by TLM curve.

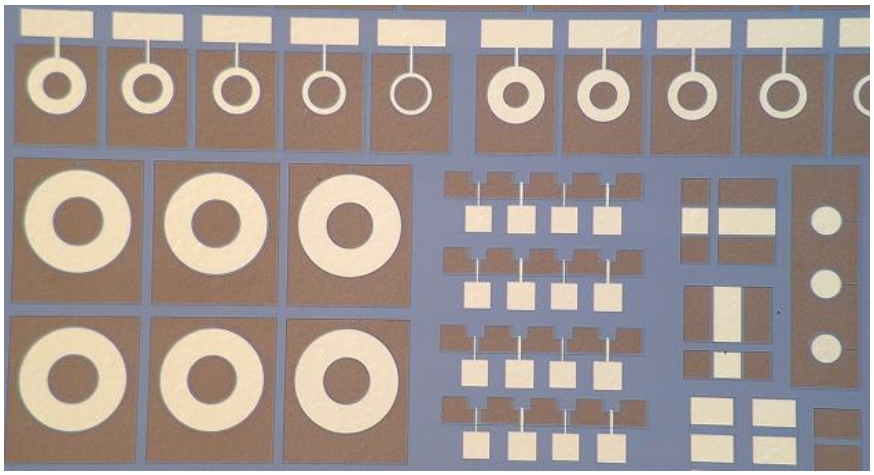


Fig. 2-6 The picture of AlGaN/GaN HFETs after finishing the gate metallization.

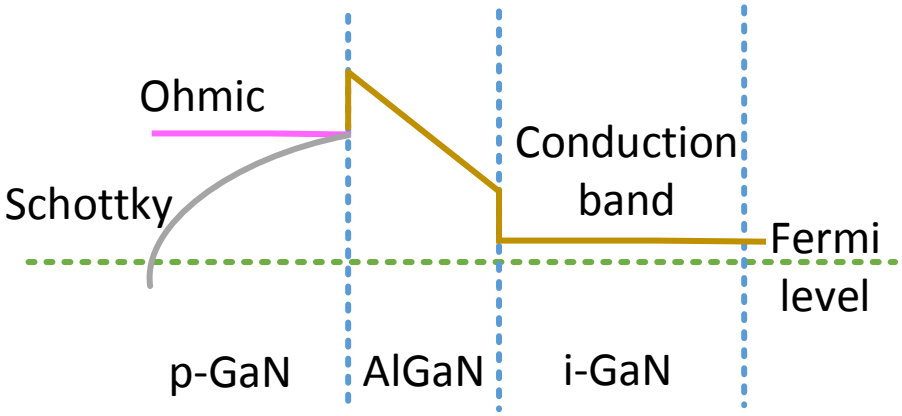


Fig. 2-7 Energy band of ohmic gate and Schottky gate.

However, other candidates for p-GaN gate electrode have been proposed, such as W/Au, Ti/Au, Mo/Au [108]. The contact method on p-GaN gate play an important role to obtain good device performance in normally-off deivce. Recently, there is different gate contact method in HFET with p-GaN gate. It mainly divides into two kinds: ohmic contact and Schottky contact. The formation of ohmic gate on p-GaN adopt the metal or metal oxide with high work function. As show in Fig. 2-7, the ohmic gate is formed between p-GaN and electrode. However, for the Schottky gate, the metal electrode with low work

function is adopted, and the relative thickness depletion layer is presented in the p-GaN surface. These two gate contact methods could achieve the good device characteristics. On the other hand, the dielectric layer/p-GaN as an alternative method is also investigated in this context. And the details will be discussed in later sections.

§2.1.4. Test methods of p-GaN gate HFETs

The p-GaN gate HFETs are characterized by I–V measurement with semiconductor parameter analyzer (Agilent HP 4155C). The I–V characteristics of TLM test can extract the ohmic contact resistance and sheet resistance. The I–V test on the DC performance of p-GaN gate HFETs include gate current-gate voltage (I_g-V_g), drain current-drain voltage (I_d-V_d), and drain current-gate voltage (I_d-V_g). Transconductance gm as an important parameter reflects the controlling ability of p-GaN gate upon the channel current, and equals to the derivatives of I_d-V_g characteristics.

(a) The ohmic contact test by TLM

A TLM structure was used to measure the ohmic contact resistance and sheet resistance as shown in Fig. 2-8. The ohmic electrodes formed on GaN cap layer or AlGaN layer, and the surrounding area including spacing was formed by different isolation methods. The spacing between each two electrodes were 5 μm, 10 μm, 15 μm, 20 μm, 25 μm, respectively.

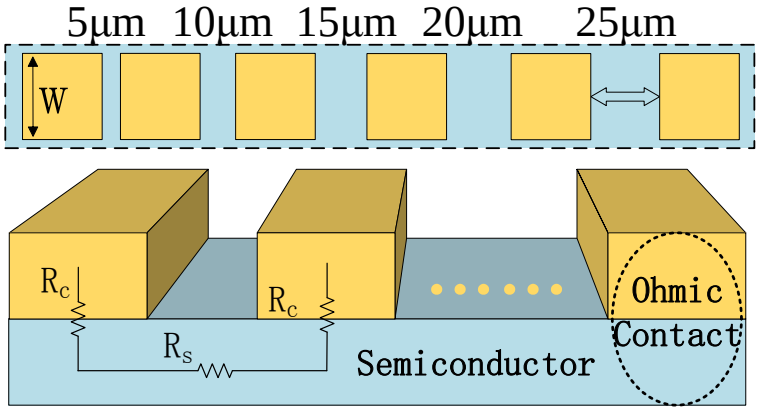


Fig. 2-8 Picture of the ohmic electrode after 850 °C.

To obtain high-accuracy measurement, four probes are used in I–V test. The resistances

R between each two electrodes changed with spacing d, and were measured by I–V test, then R-d characteristics was obtained by the equation (2.1).

$$R = \frac{\rho_s d}{W} + \frac{2R_C}{W} \tag{2.1}$$

Where ρ_s is sheet resistance of isolation region (Ω/□), W is width of electrodes, and R_c (Ω·mm) is ohmic contact resistance.

(b) The calculation of the mobility by the C-G_m method

In the conventional MOSFET, field-effect mobility is often extracted by the gate capacitance-transconductance method (C-G_m) from the transfer characteristics. This method is also fit to HFETs with p-GaN gate [109].

In the linear region, the current equation is shown in (2.2)

$$I_D = \frac{WC_{ox}}{L}\mu\left\{(V_G - V_T)V_D - \frac{1}{2}V_D^2\right\} \tag{2.2}$$

In a low electric field condition, the gradual channel approximation (GCA) model is adopted. When the $V_D \ll V_G$-V_T, namely, V_D is small enough, the approximated current can be expressed by equation (2.3)

$$I_D \approx \frac{WC_{ox}}{L}\mu\{(V_G - V_T)V_D\} \tag{2.3}$$

Generally, the V_D is set to be 0.1 V.

According to the definition of the gate transconductance shown in equation (2.4)

$$G_m = \frac{\partial I_D}{\partial V_G} \tag{2.4}$$

Substitute equation (2.3) into equation (2.4), the result is shown in (2.5)

$$G_m = \frac{WC_{ox}}{L}\mu V_D. \tag{2.5}$$

From equation (2.5), the field-effect mobility μ_{FE} can be express as equation (2.6)

$$\mu_{FE} = \frac{G_m L}{C_{ox} W V_D} \tag{2.6}$$

here G_m is the transconductance which can be extracted from I_D-V_G characteristics , L and W are the gate length and width, V_D is the drain voltage, C_{ox} is the gate oxide capacitance which can be extracted from the C-V measurement.

The derivation previously is fit to the bar type HFETs. However, for the ring type HFETs, the W need to be considered again. The equivalent L/W could be expressed by equation (2.7)

$$\frac{L}{W} = \frac{1}{2\pi} \ln\left(\frac{r_{out}}{r_{in}}\right) \tag{2.7}$$

And the equation for ring type HFETs is shown in (2.8)

$$\mu_{FE} = \frac{G_m \ln(r_2/r_1)}{2\pi C_{ox} V_D} \tag{2.8}$$

§2.2. Normally-off MIS-HFETs with p-GaN gate

In a normally-on MIS-HFETs, the insertion of the dielectric layer can adjust the device performances such as the V_{th}, gate voltage swing, leakage current and drain current. Several key requirements are important to realize a good MIS structure: (a) a good dielectric layer with low leakage current; and (b) a good interface between the dielectric layer and semiconductor with low interface state density. In this case, the high-k materials is recommended to adopt for device performance.

Similar to the normally-on MIS-HFETs, the HFETs with p-GaN gate is also considered to be the MIS gate, which is expected to gain higher device performance. The structure of MIS-HFETs with p-GaN is shown in Fig. 2-9. The MIS gate consist of gate metal electrode, dielectric layer and p-GaN cap layer. Due to the relatively mature growth technique, in this work, the SiN_x is used as the dielectric layer.

The fabrication processes of MIS-HFET with p-GaN is a little complicated than HFET with p-GaN. The difference is the dielectric layer deposition after mesa process. The dielectric layer of SiN_x is deposited by plasma enhanced vapor deposition (PECVD) at 350 ^oC. Then the post-annealing is conducted for enhancing the interface state between

dielectric and semiconductor. Finally, the Ni/Au of 70/30 nm as the gate metal electrode is deposited by magnetron sputtering.

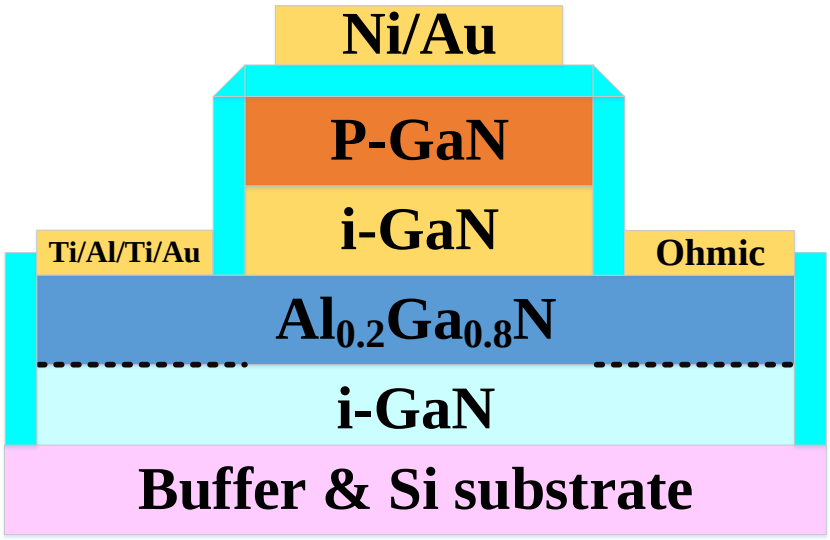


Fig. 2-9 schematic of MIS-HFETs with p-GaN.

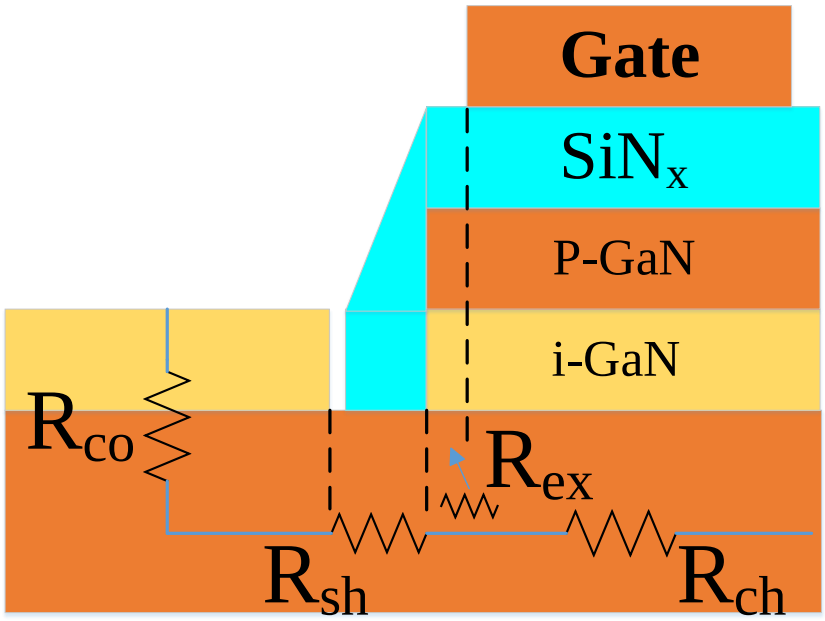
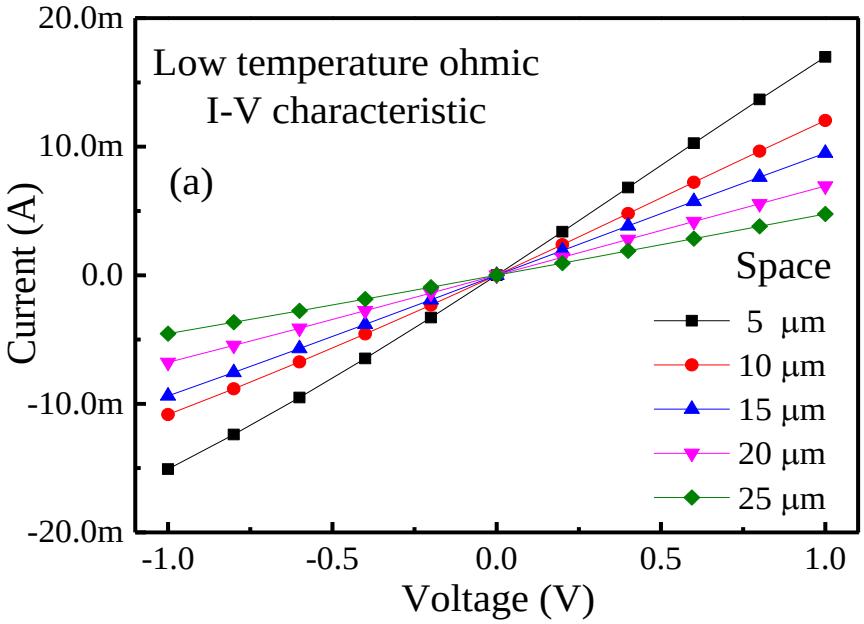


Fig. 2-10 the model of the normally-off MIS-HFETs with uncovered region.

§2.3. Normally-off MIS-HFETs with self-aligned-gate (SAG)

The normally-off MIS-HFETs with p-GaN has the drawbacks of large on-state resistance (R_{on}), and it mainly ascribes to the large channel resistance. As shown in Fig. 2-10, if a conventional ohmic-first fabrication sequence is adopted, the metal electrode cannot cover all the gate area due to the limitation of the alignment process after the mesa isolation. Therefore, the channel resistance will increase due to the depletion feature of the p-GaN layer in the uncovered region. To address this issue and optimize the device performance further, the more effective MIS-HFET structure should be raised.

Now, a gate-first process is necessary to form a self-aligned gate (SAG) structure among the p-GaN layer, the dielectric layer and the gate metal electrode. To distinguish from reason of lowering the access resistance for conventional self-aligned gate, this self-aligned gate is mainly to decrease the channel resistance. Furthermore, the conventional high-temperature (HT) ohmic annealing should be avoided concerning the gate degradation, which is observed in p-GaN HFET device with a metal gate. Microcrystalline in the gate dielectric was also observed during the HT ohmic annealing. Therefore, a low-temperature (LT) ohmic technique is required for the gate-first process to protect the dielectric. We have proposed a LT ohmic technique with the assistance of inductivity coupled plasma (ICP) treatment. The results of MIS-HFETs with p-GaN is shown in Fig. 2-11. A good ohmic contact can be confirmed.



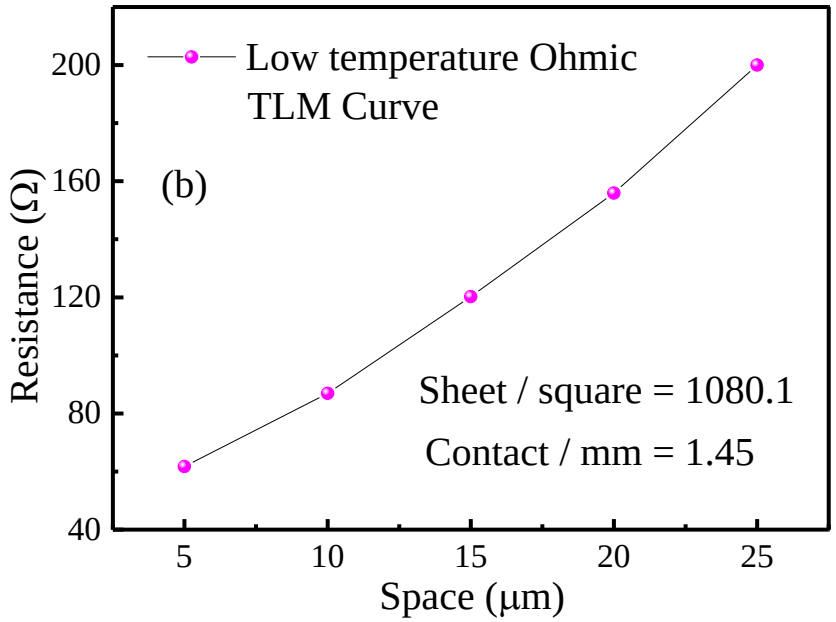


Fig. 2-11 (a) I-V characteristics of TLM in different space, and (b) ohmic result by fitting TLM curve.

§2.4. Conclusion

This section analysis the principle of the normally-off operation. The epitaxy structure of the HFET with p-GaN gate is investigated. At the same time, the mechanism of the 2DEG depletion by p-GaN is presented in different theory. Moreover, the specific fabricated process is developed to achieve the HFET with positive threshold voltage. On the other hand, the ohmic contact and gate contact method are emphasize. The low temperature ohmic process could obtain great ohmic contact compared to the high ohmic process by ICP assistance. Finally, gate contact including the ohmic and Schottky contact is discussed.

Chapter 3：Normally-off AlGaN/GaN Heterostructure Junction Field-Effect-Transistors with Blocking layer

§3.1. Normally-off HJFETs with p-GaN gate for power switching

Due to the great performance, a significant progress of AlGaN/GaN HFETs technology are obtained. AlGaN/GaN HFETs have demonstrated low on-state resistance and high breakdown characteristics which is due to high electron mobility and high blocking field characteristics. AlGaN/GaN HFETs on Si substrate are potential for power switching application. It is efficient power switching up to approximately 1200 V. However, the inherent normally-on operation impedes the further development for power switching technology. For a simple gate control design and a fail-safe operation, a normally-off AlGaN/GaN HFETs with p-GaN gate for power switching are developed. Now, AlGaN/GaN heterostructure FETs with a p-GaN gate structure (p-GaN gate HEMTs) with off-state 650 V breakdown voltage at gate of 0 V have been reported as a component of MHz-switching power device commercially, in which a p-GaN layer on top of an AlGaN barrier depletes 2DEG carriers in the channel [110].

As previous mentioned, many methods have been adopted to realize the normally-off AlGaN/GaN HFETs. So as to realize normally-off devices, namely the enhancement mode (e-mode) transistors, the gate region needs to keep switch-off at gate voltage of 0 V. An effective method to obtain the normally-off operation is the p-GaN gate. The p-type gate HEMTs realize the normally-off device by raising the conduction band in the channel at equilibrium. So the normally-off AlGaN/GaN HFETs with a p-type cap layer is called the Heterostructure Junction Field -Effect-Transistors (HJFETs). As the most promising material for realizing the normally-off operation, both in industry and in research centers, continued research and development of normally-off p-GaN gate HFETs power transistors is ongoing. However, during the actual p-GaN epitaxial growth, the high temperature around 1000 ^{o}C is necessary. Meanwhile, the Mg^{+} as a common p-type dopants has the possibility to out-diffusing into the AlGaN and GaN channel. And the 2DEG would be degraded. It leads a low device performance [111].

We employ the AlGaN/GaN HFETs with p-GaN gate and intrinsic GaN layer as insertion layer placed between p-GaN cap layer and AlGaN barrier to fabricate the device.

And through adjust the thickness of i-GaN layer, the different devices characterization would be investigated. Nevertheless, the trade-off need to be make for V_{th} and device characterizations.

§3.2. Fabrication of normally-off HJFETs with p-GaN gate

The schematic view of epitaxy structure is shown in Fig. 3-1a. A conventional AlGaN/GaN heteroepitaxy structure is grown on a silicon substrate by MOCVD. The vertical structure of wafer consists of a buffer layer, a carbon-doped high resistance GaN, and an i-$Al_{0.2}Ga_{0.8}N$/GaN (20/200 nm) heterostructure from bottom to top (referred as Device D). Based on this structure, wafers with 20 nm (referred as Device A), 10 nm (referred as Device B) and 5 nm (referred as Device C) of i-GaN inserting layers beneath the 130 nm p-GaN layer are grown for normally-off device fabrication. The fabrication process is refer to the conventional HFETs with p-GaN gate.

§3.3. DC characterization of HJFETs with p-GaN gate

A ring-type device with inner radius r_1 of 89 μm and outer radius r_2 of 183 μm was used for device evaluation (Fig. 3-1b). Gate length L_g and effective gate width W_g are 94 and 819 μm, respectively. The spaces between the gate, drain and the source (L_{gs} and L_{gd}) are 6 μm. The output drain current-voltage (I_d-V_d) characteristics of the three p-GaN gated HJFETs (Device A, B and C) and normally-on HFET (Device D) as reference are shown in Fig. 3-2. All the devices present good pinch-off characteristics. The maximum output current density decrease with the decreasing i-GaN layer thickness. The current density of device A is approximately 54 mA/mm at V_{gs} of 5 V that is similar to the device D with 55 mA/mm at V_{gs} of 1.5 V in Fig. 3-2b, while it is only approximately 6 mA/mm at V_{gs} of 5 V for device C when the i-GaN layer decreased to 5 nm. This phenomenon is ascribed to that the degradation of 2DEG channel by the p-GaN layer, especially when the i-GaN layer is thinner. Furthermore, the gate current-voltage characteristics of the devices (the inset in Fig. 3-2a) demonstrate that the devices B and C show slightly smaller gate leakage than device A. As can be also seen in the next discussion, the channel degradation from the effect of the Mg diffusion lead to a larger resistance. Owing to the increasing turn-on

resistance, the gate leakage current in the forward bias deceased with the decreasing i-GaN layer thickness.

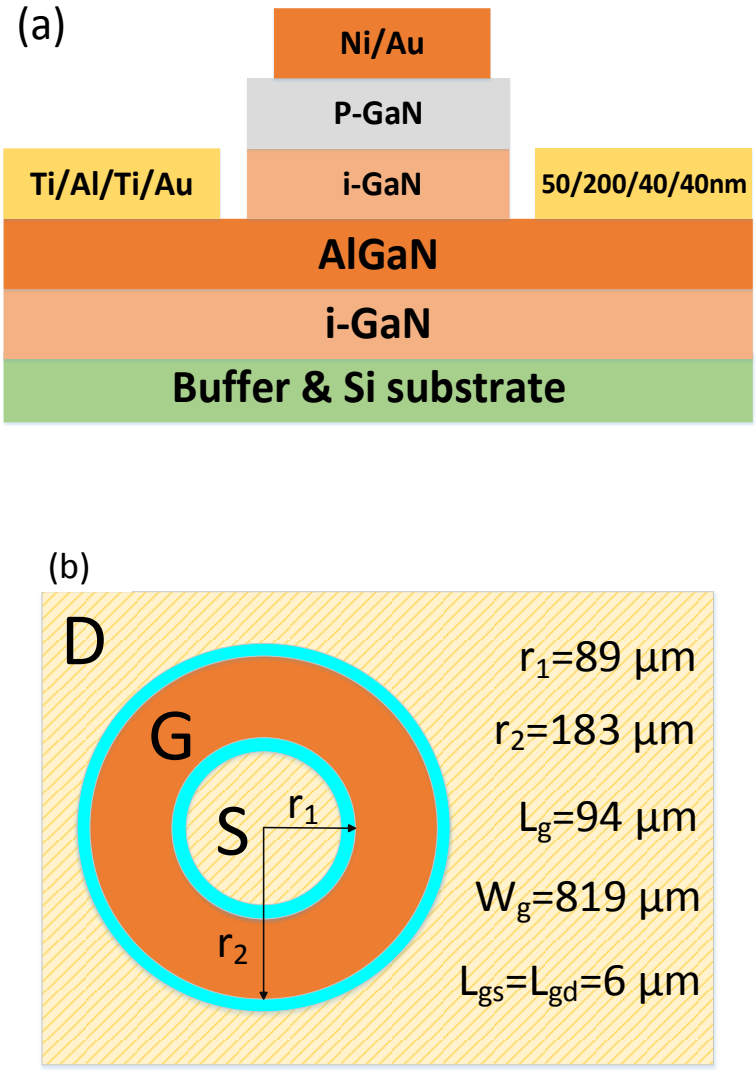


Fig. 3-1 (a) Schematic structure of p-GaN gated AlGaN/GaN HJFETs with different i-GaN layers, (b) a ring-type HJFET for device evaluation.

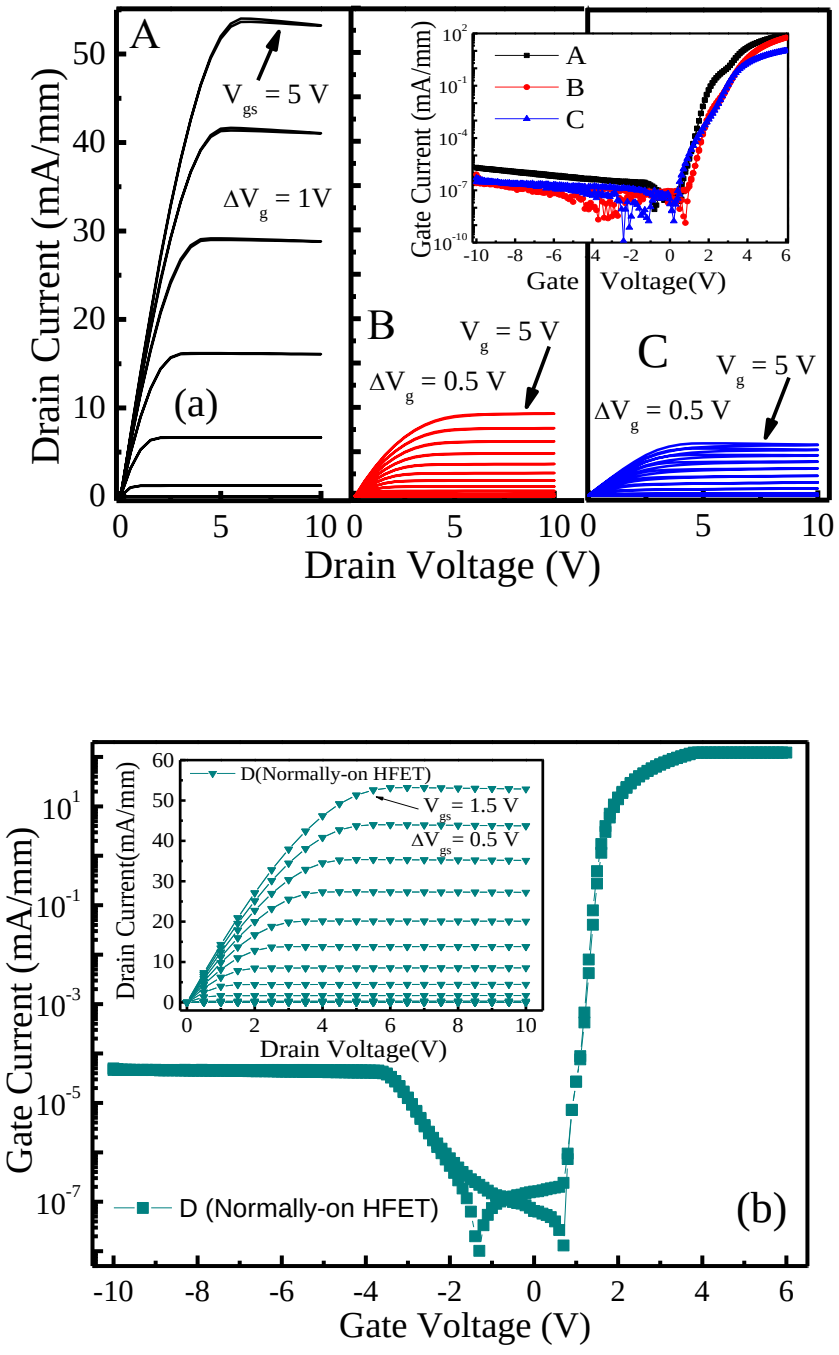
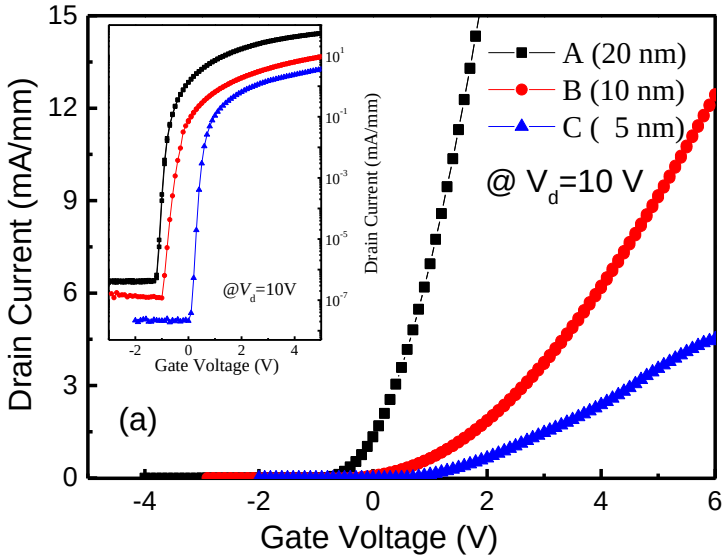


Fig. 3-2 (a) Output current-voltage (I-V) characteristics of devices A, B and C. Inset is the gate current-voltage characteristics in different devices, (b) the gate current-voltage characteristics of device D and output current-voltage (I-V) characteristics in inset.

Fig. 3-3 shows the transfer characteristics of fabricated devices at drain voltage (V_d) of 10 V. The threshold voltage (V_{th}) are extracted by linear fitting the forward region and are -0.1, 1.54 and 1.77 V for device A, B and C, respectively. The on/off ratios calculated from the logarithmic plot of transfer characteristics (inset of Fig. 3-3a) are 1.5×10^7, 3×10^6 and 1×10^6 for the devices with 5, 10 and 20 nm i-GaN layer thickness, respectively. This also indicates that a smaller i-GaN layer thickness is beneficial for suppressing the leakage current. In order to further understand the transfer characteristic, the band diagrams in equilibrium status were simulated with Silvaco TCAD software taking into account the polarization charges (shown in Fig. 3-3b). For device C with the highest V_{th}, the depletion layer (build-in field) between p-GaN and heterostructure is relatively larger. The conduction band of the heterostructure is totally lifted up above the Fermi level, which would deplete the 2DEG channel at the interface between AlGaN and GaN for normally-off operation. However, the depletion layer (build-in field) of junction decreased with the increasing thickness of the i-GaN layer, and then the conduction band became close to the Fermi level gradually. Finally, the 2DEG starts to accumulate in heterostructure channel for Device A, which means that the depletion effect of p-GaN is very weak when the thickness reached 20 nm and the threshold voltage shifts negatively below zero.



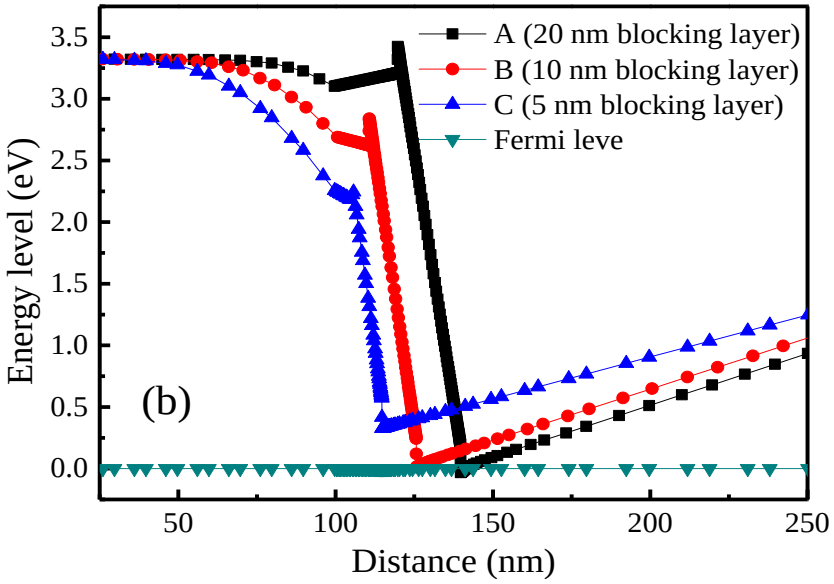


Fig. 3-3 The linear and the corresponding logarithmic (inset) plots of transfer characteristics, and (b) the energy band of devices A, B, and C.

The field-effect channel mobility (μ_{FE}) of the devices was measured based on the equation as equation (3.1) by the gradual channel approximation (GCA):

$$\mu_{FE} = \frac{G_m L_g}{W_g C_{HJFET} V_d} \tag{3.1}$$

Where L_g and W_g is the gate length and effective width, C_{HJFET} the capacitance per unit area and Gm the transconductance measured at a relatively small drain voltage (V_d) of 0.1 V. The calculated mobility curve of the devices A, B and C are shown in Fig. 5. When the thickness of inserting layer is 20 nm, the mobility is approximately 1200 $cm^2V^{-1}s^{-1}$. This value is comparable with the result obtained from conventional AlGaN/GaN heterostructure, which means that the p-GaN cap shows no obvious degradation on channel mobility. However, the calculated mobility for devices with thinner inserting layer degraded obviously to approximately 700 $cm^2V^{-1}s^{-1}$. A possible reason may be ascribed to the Mg diffusion into the AlGaN/GaN heterostructure, which may causes some scattering factors, such as charged defect scattering and ionized impurity scattering.

The mobility degradation with a thinner inserting layer is more serious because of the distance between Mg dopants and channel is shorter and the diffusion is more easily.

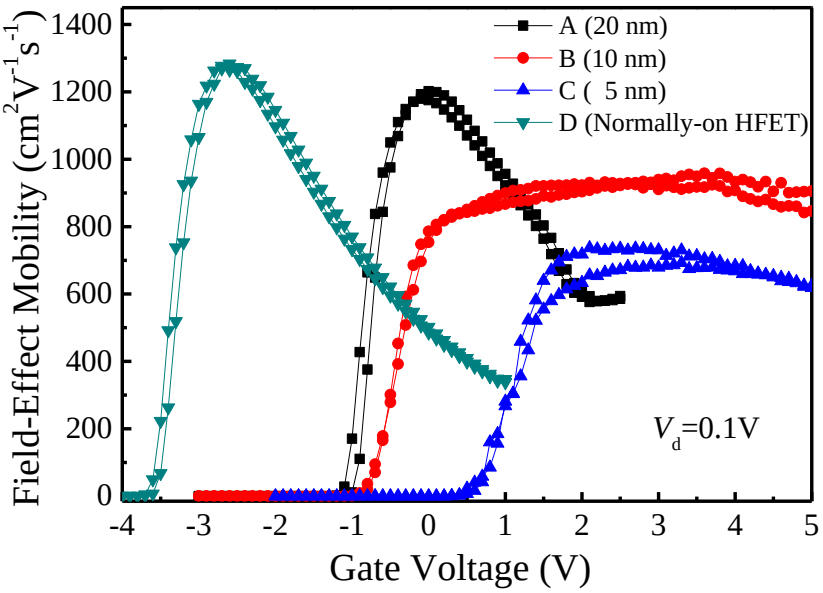
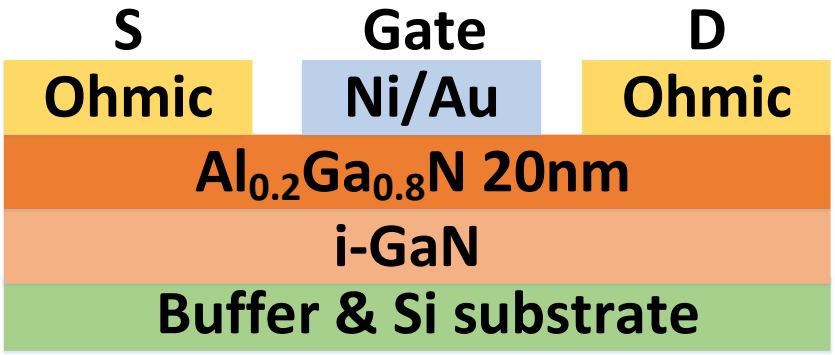
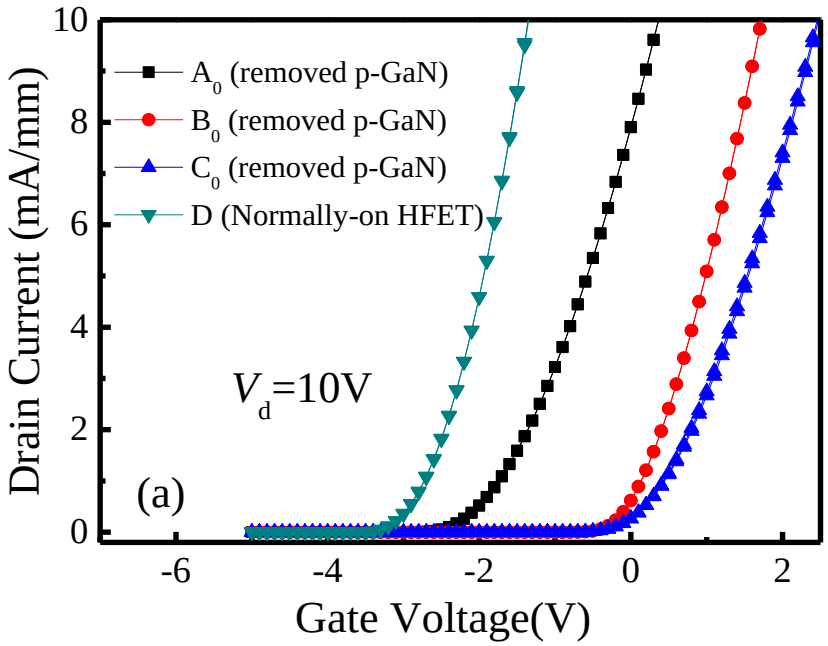


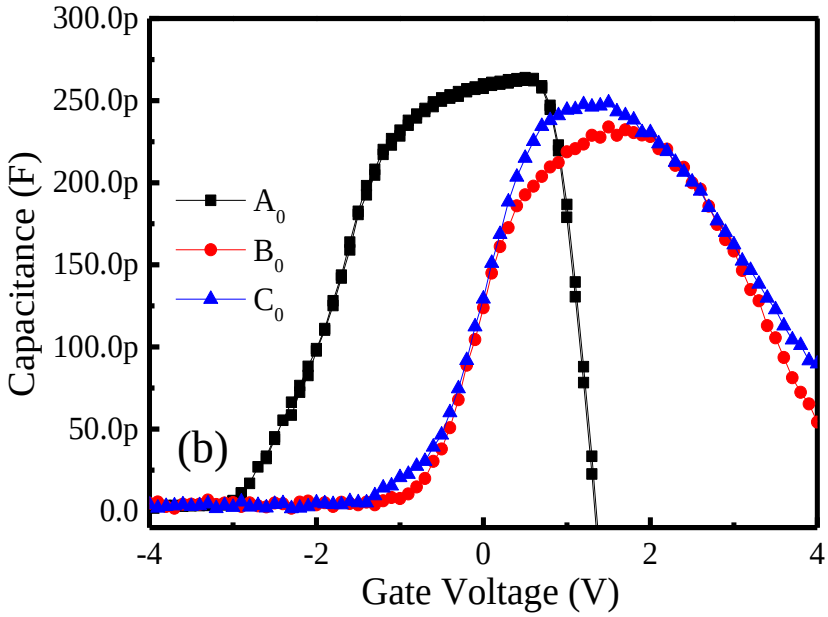
Fig. 3-4 The field-effect mobility of device A, B, and C

In order to further investigate the effect of i-GaN layer, we evaluated devices A0, B0 and C0 fabricated in recessed region (shown in inset of Fig. 3-5 and the dimension shown in Fig. 3-1b) which were removed the p-GaN and i-GaN layer with quite low etching rate. Generally, the 2DEG channel recovers when there is no p-GaN cap and the devices should operate like the conventional normally-on AlGaN/GaN device (device D). However, compared with the normally-on HFETs (device D shown in Fig. 3-5a), the V_{th} shows obvious positive shift from approximately -2.8V for device D to -1.9, -0.2 and 0.2 V for device A0, B0 and C0, respectively. One possible reason which causes the positive threshold voltage shift is the etching damage. The Fig. 3-5b shows the 2DEG channel position by C-V calculated is approximately 22, 23 and 23.5 nm for device A0, B0 and C0 after dry etching, respectively. So it means that there is about 2-3 nm residue i-GaN and the surface damage of AlGaN layer induced by dry etching is negligible. On the other hand, the Hall text result is also shown in the inset table. After removing the p-GaN and i-GaN layers, the A0 has the highest carrier concentration and mobility of 2.6×10^{13} cm^{-3}

and 1092 $cm^2/V\cdot s$ at 300 K. But these value drop to 3.7×10^{12} cm^{-3} and 494 $cm^2/V\cdot s$ for C0. It shows that the carrier concentration and mobility have an obviously decrease even after removing the p-GaN and i-GaN. The most serious problem is that there might be a p-type AlGaN or GaN existing in the AlGaN barrier and the channel region due to the Mg diffusion, which acts as the p-GaN cap and will lift-up the conduction band and depletion the 2DEG channel.







Sample	2DEG channel position	Carrier concentration	Mobility
A0	22 nm	2.662E13	1092
B0	23 nm	7.359E12	609
C0	23.5 nm	3.729E12	494

Fig. 3-5 (a) the threshold voltage of devices removed p-GaN layer and blocking layer. Inset is the epitaxy structure of A0, B0, C0, D devices, (b) the capacitance-voltage curve and the remaining AlGaN thickness (inset).

To confirm the existing of the Mg, the spatial distribution of Mg dopant was measured by SIMS using an IMS 7f magnetic sector SIMS system. Figure 3-6 shows the Mg concentration profile versus the depth from the wafer surface. The Mg concentration remains a high level of approximately 4×10^{19} cm^{-3} in the first 130 nm p-GaN cap. For device A, the Mg concentration decreases drastically in the 20 nm GaN i-GaN layer. In fact, a decrease in the Mg diffusivity in i-GaN is reported [111]. Therefore, the Mg concentration way exhibits the faster dropping which has a thicker i-GaN layer. And there are different Mg concentration way for different device structures in Fig. 3-6. Then the low Mg concentration can be firmed in channel position. And the Mg concentration is increasing when the i-GaN layer decreases to 10 and 5 nm, the Mg concentration in channel has an obviously increasing, which will deteriorate the mobility of 2DEG and

lead to a serious degradation on the device channel. Those results indicate that the obviously blocking feature of i-GaN layer and a suitable thickness for i-GaN layer is necessary for preventing the Mg diffusion much effectively.

On the other hand, the sheet resistance (obtained by transmission line model) and field-effect channel mobility (μ_{FE}) of all the devices are also presented in Fig. 3-7. The sheet resistance increased from about 500 Ω/sq (device D) to approximately 6112 Ω/sq with the decreasing blocking layer thickness to 5 nm (device C0). Besides, the mobility of device A0, B0 and C0 are 1013, 470 and 373 $cm^2V^{-1}s^{-1}$, respectively. This results further confirm the mobility degradation caused by the Mg diffusion into the AlGaN/GaN heterostructure and some lattice damage during ICP etching. It should be mentioned that other method is still necessary to make a positive threshold voltage shift when a GaN blocking layer is introduced. On the other hand, the time dependent output characteristics was carried out to evaluate the reliability as shown in Fig. 3-8. A drain stress voltage of 5 V and a gate stress voltage of 3 V are applied to the devices. Both of the stress duration and interval are 2h. After 4 cycles, the output characteristics of all samples are relatively stable without no obvious degradation, implying the good stability.

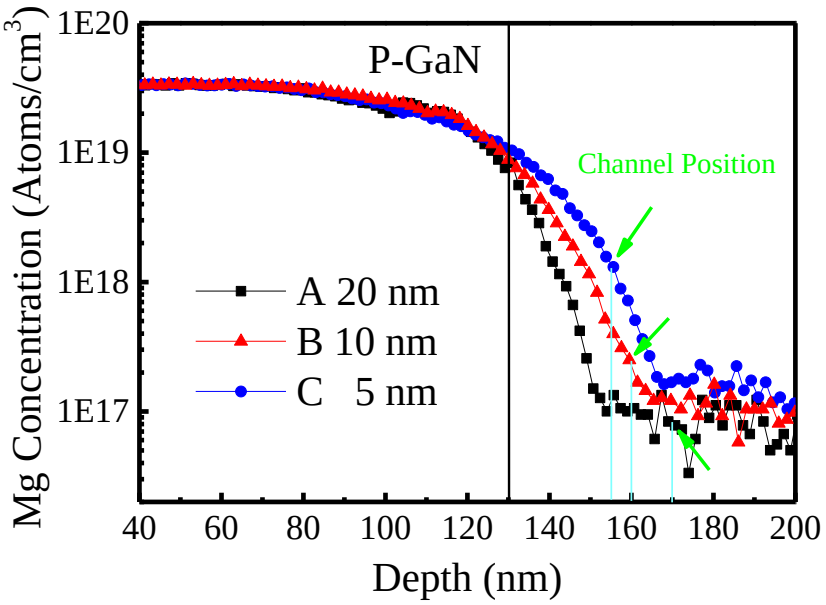


Fig. 3-6 Mg concentration profile of wafers with different i-GaN blocking layer measured by SIMS. The channel position in different devices is also marked with arrow.

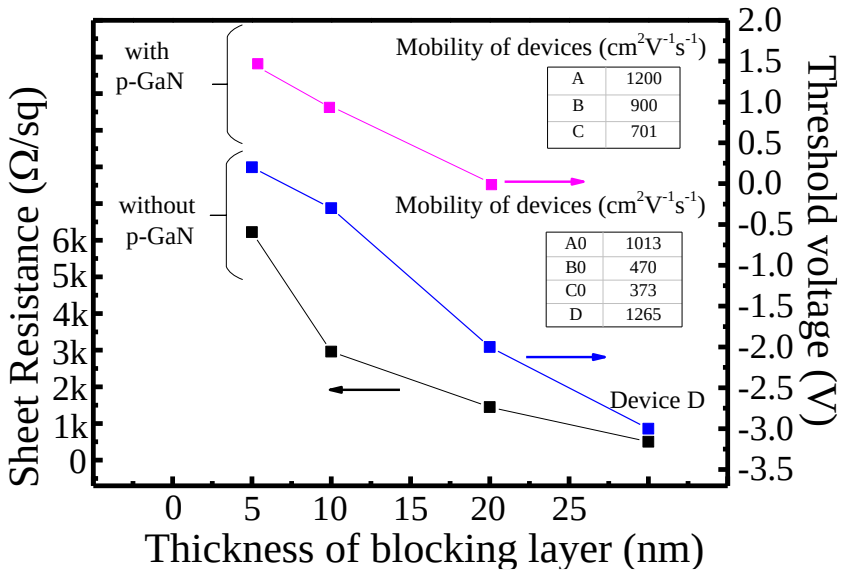


Fig. 3-7 The sheet resistance and V_{th} for all of devices after removing the p-GaN and blocking layer, and mobility of devices in inserted table.

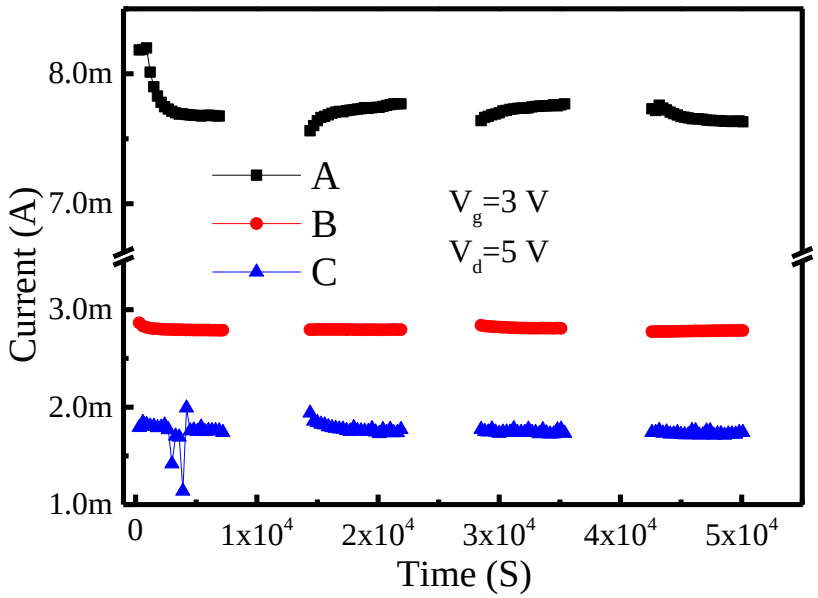


Fig. 3-8 The time dependent output characteristics of A, B, and C devices.

§3.4. Conclusion

In conclusion, we proposed a p-GaN gated AlGaN/GaN HJFET with i-GaN blocking layer and evaluated the effect of the blocking layer thickness on the electrical properties of the devices. With the blocking layer thickness decreasing, even though the threshold voltage had positive shift, the output current of the device decreased and channel deterioration could be found due to the serious Mg diffusion. However, with the i-GaN blocking layer with thickness of 20 nm, the Mg diffusion into the AlGaN/GaN heterostructure can be efficiently blocked and channel performance is comparable with the conventional AlGaN/GaN heterostructure owing to the introduction of the blocking layer. To keep the performance of the AlGaN/GaN heterostructure, a suitable blocking layer is necessary for preventing the Mg diffusion.

Even if, the i-GaN of 20 nm can effectively block the Mg diffusion and obtain a good channel quality which is compared with the conventional normally-on AlGaN/GaN heterostructure. However, the performance of normally-off is influenced by the 20 nm i-GaN blocking layer, the V_{th} of device is around 0V. Therefore, a trade-off need to be make for normally-off operation. Further, the promising method is to develop more advanced epitaxy process

Chapter 4: Normally-off AlGaN/GaN Heterostructure Junction Field Effect Transistor with SiN_x layer

§4.1. Requirement for the higher threshold voltage

Recently, GaN-based heterostructure field effect transistors (HFETs) have received much attentions in power switching. However, the AlGaN/GaN heterostructure has the negative threshold voltage performance which need extra gate voltage to pinch-off the channel, so a more complicate circuit design and high consumption. Normally-off AlGaN/GaN HFETs are more preferable for power switching applications than normally-on devices. Meanwhile, for realizing inherent failsafe operation and simple circuit configuration for power switch applications, the threshold voltage (V_{th}) of the device should be higher than +3 V to prevent the device from an incorrect action. Moreover, in some power conversion applications, a higher threshold voltage over +6 V is required to avoid the device damage from faulty turn-on that is induced by the electromagnetic interference. However, the conventional AlGaN/GaN device usually shows normally-on operation due to the high density two dimensional electron gas (2DEG) in the channel which increase the power consumption. Depletion of the 2DEG effectively is required to obtain normally-off operation with higher threshold voltage for power electronic applications.

According to the previously summary, the p-GaN (or p-AlGaN) cap layer is the one of the most promising method to achieve the normally-off operation. For normally-off HFETs with p-GaN gate, a further improvement of the V_{th} and gate voltage swing is always the key issue in practical. So the epitaxy structure of device need to be redesigned. Refer to previous discussion results, a thin i-GaN blocking layer with p-GaN gate is recommended, that the p-GaN layer need to be perfected. On the other hand, the SiN_x as the matured insulator layer is widely used in semiconductor devices which is due to the good thermal stability and simple compound process. Based on the normally-off operation with p-GaN gate (V_{th} is close to 1 V), a MIS-like novel gate structure of SiN_x /p-GaN stacks is proposed for further improving the device V_{th}. Therefore, the characteristics would be investigated which the SiN_x layer is between the gate metal and the p-GaN cap layer. Besides, due to the higher breakdown field of 10-12 MV/cm in SiN_x,

the introduction of SiN_x is also beneficial for suppressing the gate leakage current and improving the maximum gate voltage [112].

§4.2. Fabrication of Normally-off AlGaN/GaN heterojunction HFETs with a MIS gate

The schematic view of epitaxy structure is shown in Fig.4-1a. A conventional AlGaN/GaN heteroepitaxy structure is grown on a Si substrate by metal organic chemical vapor deposition (MOCVD). The vertical structure of the wafer consists of a buffer layer, a carbon-doped high resistance GaN and an $Al_{0.2}Ga_{0.8}N$/GaN (20/200 nm) heterostructure from bottom to top (Fig. 4-1a). Then, 10 nm i-GaN blocking layer and 100 nm p-GaN cap layer is grown for normally-off device fabrication with optimized epitaxial condition. An i-GaN layer beneath p-GaN serves as blocking layer to suppress the Mg diffusion.

The fabrication process is based on the standard photolithography and lift-off technologies, and simulate to the conventional p-GaN gate device. The steps consist of 1) cleaning by SPM and organic solution, 2) p-GaN recess by ICP dry etching, 3) Meas etching by dry etching, 4) SiN_x deposition by PECVD, 5) ohmic metal electrode deposition and annealing, 6) gate metal electrode formation as shown in Fig. 4-1 (a)-(g). The differences with the conventional p-GaN gate device is SiN_x deposition and ohmic formation. The SiN_x as the insulator layer with thickness of 0-30 nm was deposited by employing the plasma enhanced chemical vapor deposition (PECVD) (Fig. 4-1d). Then the annealing at 1000^{o}C for 10 min in N_2 ambient was done which was reported as an annealing condition to minimize the interface state density. For realizing the ohmic contact, the SiN_x layer on source/drain region was removed by immersing the wafers in the BHF solution (Fig. 4-1e). And the SiN_x layer on access region was existed as the passivation to reduce the surface state. Then a Ti/Al/Ti/Au (50/200/40/40 nm) multi-layer structure on source/drain was deposited by magnetron sputtering and annealed at 850^{o}C for 3 min in N_2 ambient by rapid thermal annealing (RTA) (Fig. 4-1f). Before the gate metal deposition process, the samples were treated by O_2 plasma ashing. Then the possible oxide layer was removed by the diluted HCl (HCl:H_2O=1:1) solution for 5 min after the lithography process. A Ni/Au (70/30 nm) gate electrode was formed and annealed at 300^{o}C for 10 min in N_2 ambient as post-annealing (Fig. 4-1g).

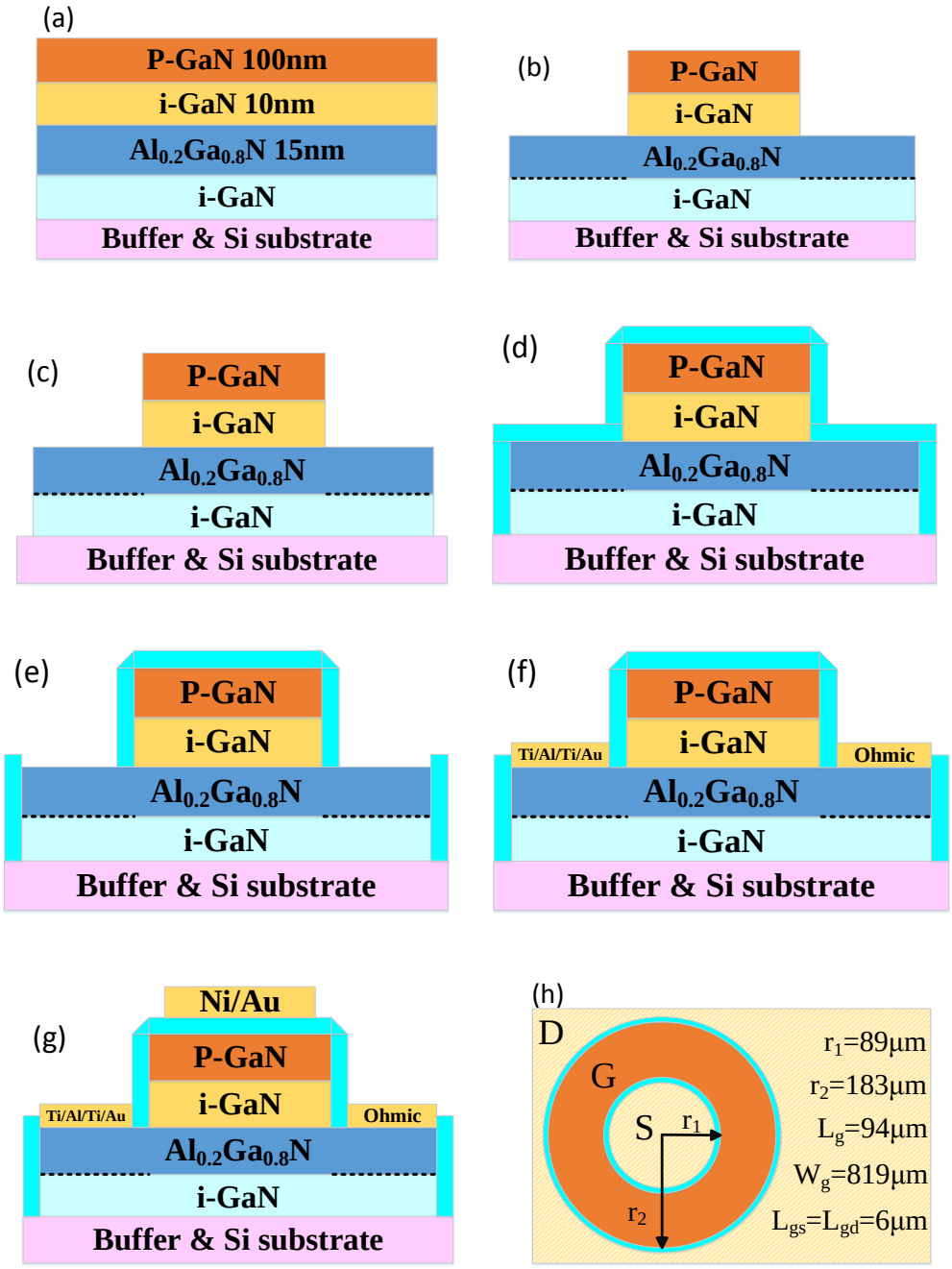


Fig. 4-1 (a)-(g) The fabricated process flowchart, and (h) the device dimension.

§4.3. Characterization of AlGaN/GaN heterostructure with MIS gate

The output current-voltage (I_d-V_{ds}) characteristics of the normally-off MIS-JFETs with different SiN_x layer thicknesses are shown in Fig. 4-2. The device is a ring-type device

(Fig. 4-1h). We set the output drain current density of the around 14 mA/mm devices as criterion in Fig. 4-2. Obviously, in the device with thicker SiN_x layer, the higher gate voltage is needed to reach this current density. The details are show that the current density of device with 30 nm SiN_x is 14 mA/mm at V_{gs} of 15 V with respect to 14 mA/mm at V_{gs} of 12 and 13 V in devices with 20 and 30 nm SiN_x, respectively. This phenomenon maybe ascribe to the larger voltage drop in thicker SiN_x layer than other devices. Furthermore, Fig. 4-3 demonstrates the gate current-voltage characteristics of devices with the gate voltage range of -20 to 20 V. All the devices shows a low reverse gate leakage current around 1×10^{-7} mA at V_{gs} of -20V. It worth noting that the device without SiN_x also exhibits small gate leakage due to the existence of the PN junction in device. The minimum forward leakage current is achieved in device with 30 nm SiN_x layer which is 1×10^{-7} mA at voltage of 20V. It indicates the great insulation performance for SiN_x layer.

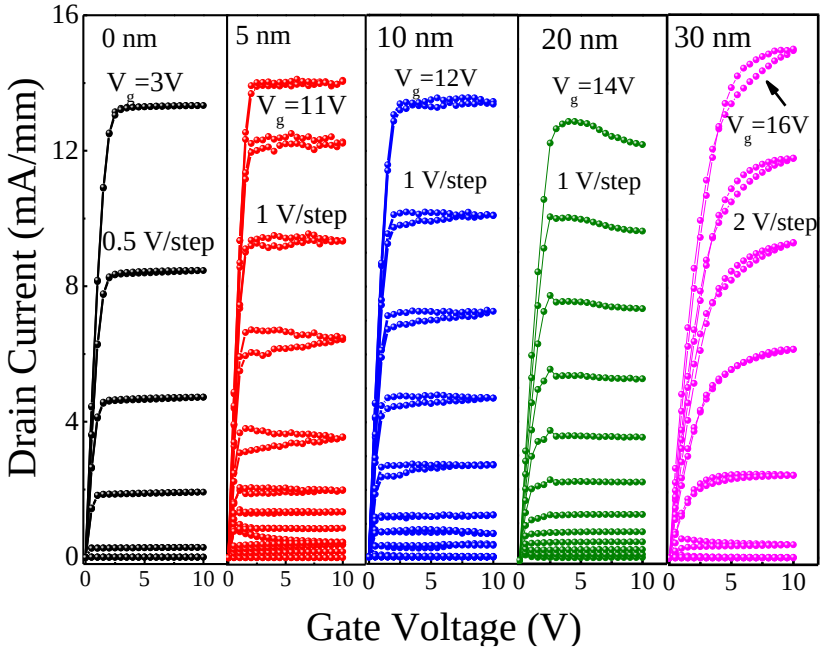


Fig. 4-2 Output Current-voltage (I-V) characteristics of devices with SiN_x thickness 0, 5, 10, 20 and 30 nm. The dimensions of the device are $L_g/W_g/L_{gs}/L_{gd}$=94/819/6/6 μm.

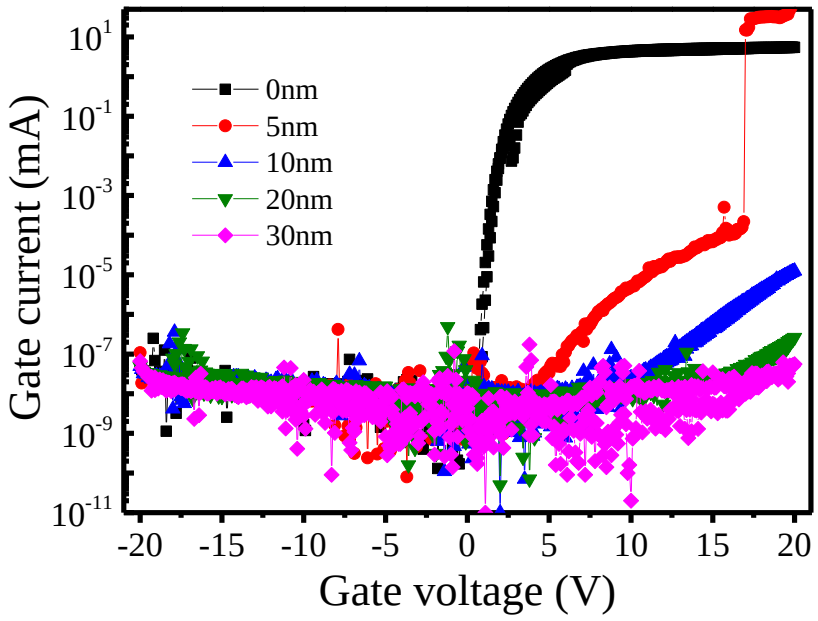


Fig. 4-3 The logarithmic of gate current-voltage characteristics in devices with different SiN_x layer.

Fig. 4-4a shows the linear transfer characteristics of devices at a drain voltage of 10V. The V_{th} of device without SiN_x layer is 0.7V. And the V_{th} of devices is 1, 2.4, 6, 8V responding to the 5, 10, 20 and 30 nm SiN_x layer which was extracted by linear fitting the forward region. It indicates that the MIS-JHFET is an alternative method to improve the device threshold voltage. And the semi-log scale is shown in Fig. 4-4b. The visible positive shift is observed for thicker SiN_x device. And the subthreshold swing is also exhibited in Fig. 4-4b. The increasing subthreshold swing (SS) value is obtained with the thicker SiN_x layer. However, the 5 nm SiN_x device has the lower SS value than 0 nm device. It's due to the SiN_x layer lead a lower leakage current. Meanwhile, the three sections in semi-log transfer characteristic curve is found, it's more obviously in 30 nm SiN_x layer device. The first and third part of curves is common in conventional semi-log transfer characteristics curve. The distinguishing one is the second part, which is possible due to the voltage dropping of the SiN_x and the large channel resistance. Fig. 4-5 shows the energy band diagram at the critical threshold condition with dielectic thickness from 0 to 30 nm. It describes the situation of a critical threshold condition in which the gate metal is biased with threshold voltage obtained from Fig. 4-4a.

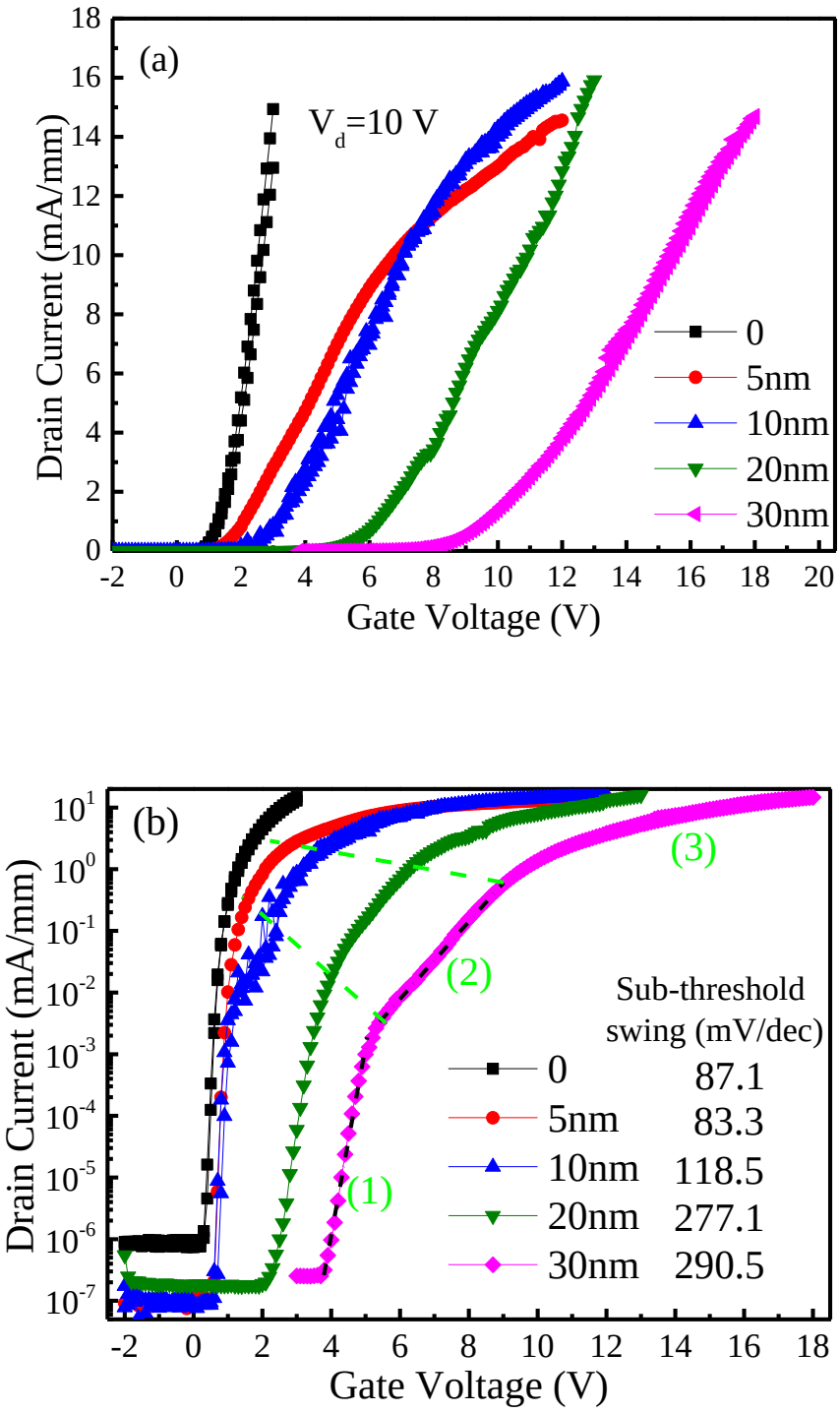


Fig. 4-4 Transfer characteristics of devices in the linear coordinate in (a), and the semi-log scale in (b).

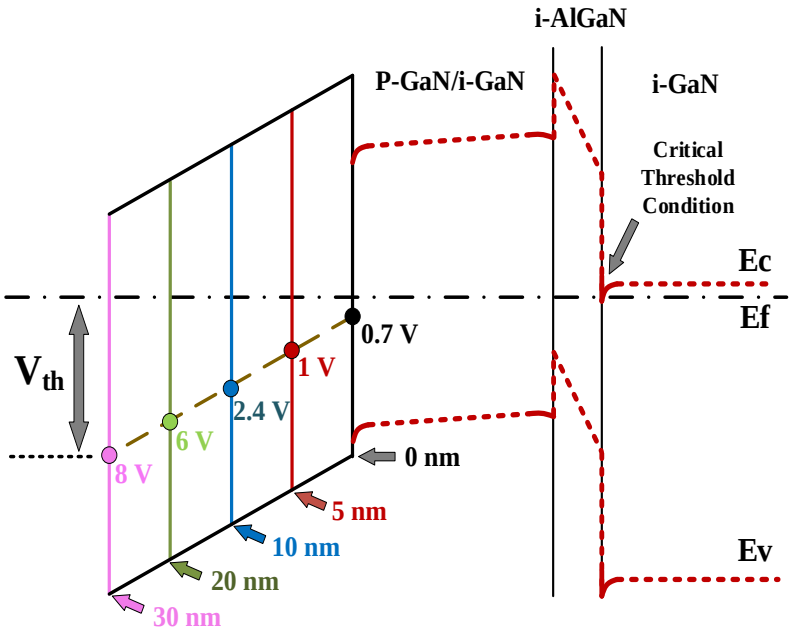


Fig. 4-5 Energy band diagram at the critical threshold condition with different thickness SiN_x layer.

The breakdown voltage (V_{BD}) was shown in Fig. 4-6a. The device with 0 nm SiN_x has the minimum V_{BD}. And the V_{BD} increased linearly with the increasing thickness of the SiN_x insulator layer. A breakdown field of approximately 8.3 MV/cm is deduced from the relationship between V_{BD} and thickness of SiN_x (Fig. 4-6b), which is beneficial for suppressing the gate leakage current and improving the maximum gate voltage swing. This breakdown field of 8.3 MV/cm has a little difference from the ideal value. It maybe ascribe to the rough crystal quality which is deposited by PECVD, it's expected to be increased if the low pressure chemical vapor deposition (LPCVD) is used. Furthermore, the relationship between the V_{th} and total capacitance of MIS gate HFETs can be explained by an equivalent circuit model formula (inset of Fig. 4-6b), in which V_{th} (JHFET) is the V_{th} of JHFETs without SiN_x, V_{th} (MIS) is the V_{th} of MIS gate JHFETs and C_{SiN} is the insulator capacitance. Fig. 4-6b shows the curve of threshold voltage versus the SiN_x layer thickness, the threshold voltage was increasing linearly with the thicker SiN_x layer. The experimental result almost coincides with the results estimated using the simple equivalent circuit model. Owing to the existence of the SiN_x layer, the applied gate voltage would partly appear across the SiN_x layer and partly across the semiconductor.

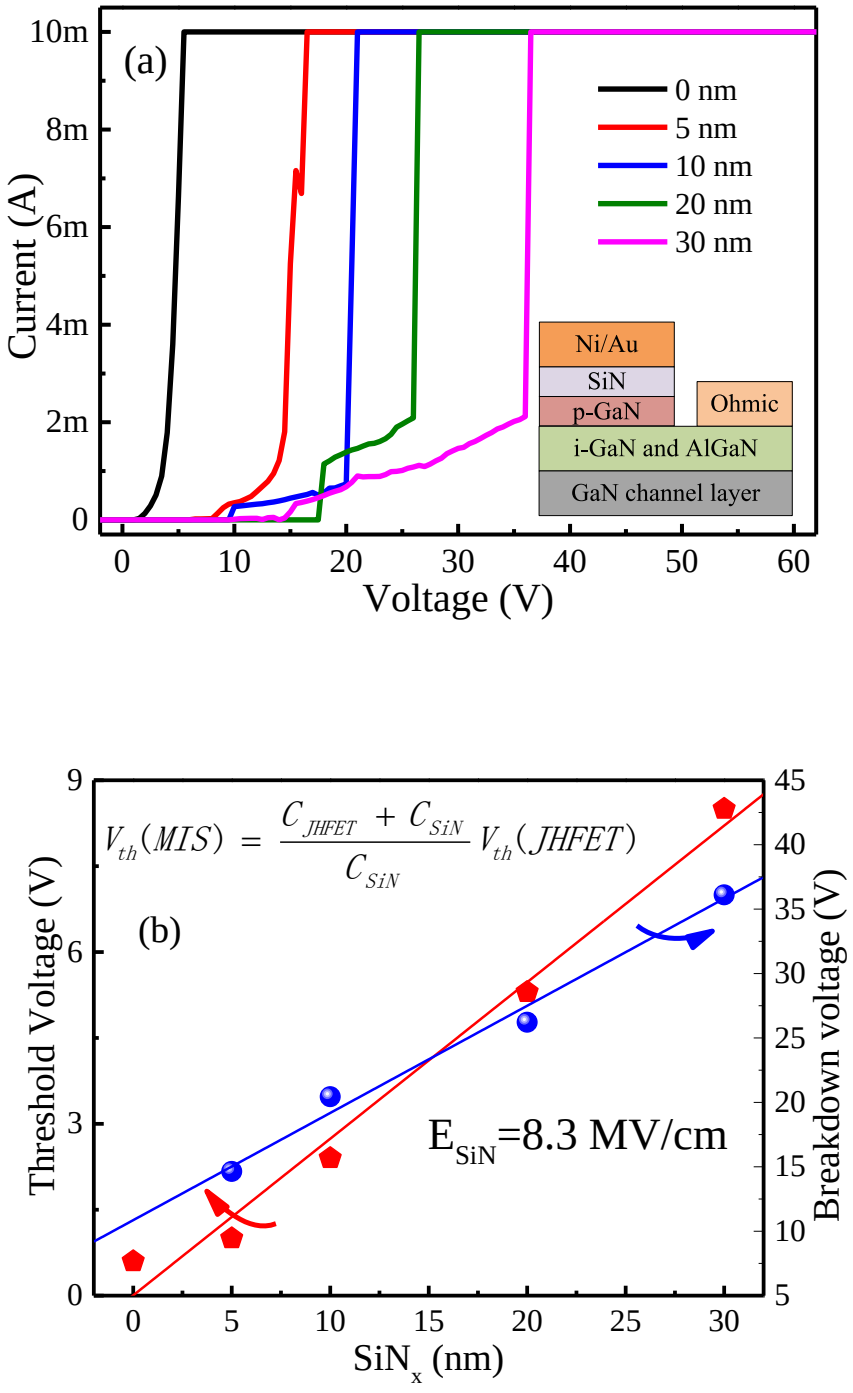


Fig. 4-6 (a) The breakdown voltage of the devices with varied thickness of SiN_x. Inset is the schematic structure for breakdown measurement, (b) the threshold voltage and breakdown voltage depend on the SiN_x thickness.

Figure 4-7 shows the capacitance-voltage (C-V) characteristics of the devices with and without SiN_x layer. The C-V curve of the 0 nm SiN_x device and the Normally-on device is demonstrated in inset of Fig. 4-7. The plateau with similar C-V value can be found in inset. It indicates that the p-GaN cap layer is a good conductor with the ohmic contact and less contribution to the C-V characteristic. Then the introduction of SiN_x layer at the gate region shows an obvious effect on the C-V characteristics, including the positive shift of threshold voltage and the appearance of double capacitance plateaus. The increased threshold voltage with the increasing SiN_x thickness is consistent with the transfer curves. While the come out of the second plateau with a relatively larger capacitance (equal to the SiN_x capacitance, C_{SiN}) reflects the electron transfer from the AlGaN/GaN to SiN_x/AlGaN interface. At the same time, when the positive voltage apply on the gate, the hole injection is happened. The hole would go through the SiN_x/AlGaN interface and reach the 2DEG channel. So the first plateau in the C-V curve not only represents the total capacitance value of the series of C_{SiN} and C_{AlGaN}, it's more complicated.

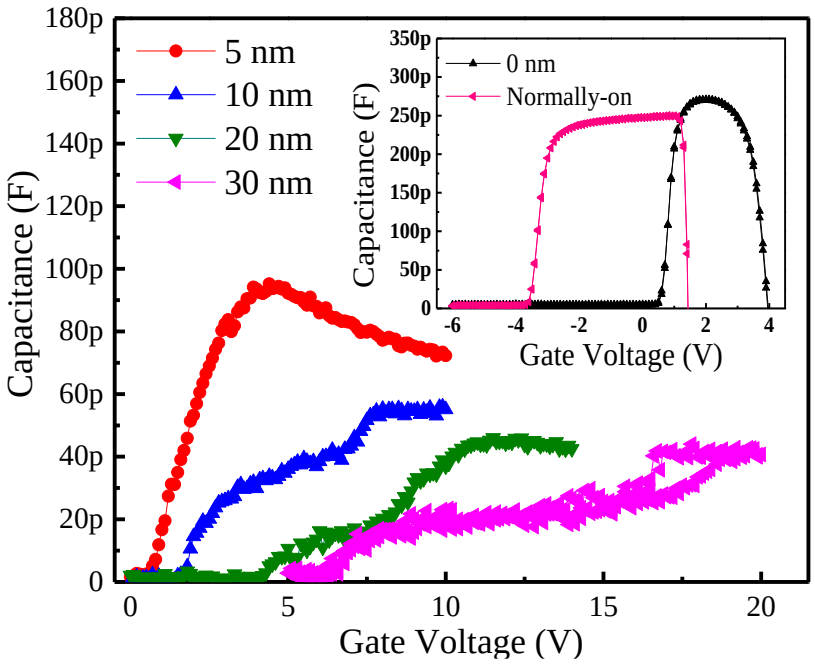


Fig. 4-7 Capacitance characteristics of devices with different SiN_x thickness. The inset is the C-V curve of the device without SiN_x layer and normally-on device.

The field-effect channel mobility (μ_{FE}) of the devices was measured and plotted in Fig. 4-8 based on the equation as follows:

$$\mu_{FE} = \frac{G_m L_g}{W_g C_{JHFET} V_d} \quad (4\text{-}1)$$

Where L_g and W_g is the gate length and effective width of the FATFET (94 μm×819 μm), C_{JHFET} the capacitance per unit area (at the first plateau) and g_m the transconductance measured at a relatively small drain voltage (V_d) of 0.1 V. The field effect mobility of all devices is around 1600 $cm^2V^{-1}s^{-1}$. It demonstrated that the mobility value of the devices with different SiN_x thicknesses are comparable to the device without SiN_x layer, implying that the SiN_x insulator shows no obvious effect on the 2DEG mobility.

The normally-on MIS devices with different thickness SiN_x layer on access region is also investigated. Figure 4-9 shows the capacitance-voltage (C-V) characteristics of the devices with and without SiN_x layer. The threshold voltage (V_{th}) demonstrates a visible regularity that the V_{th} is decreasing with the increasing thickness of SiN_x layer. The same reason is also fit for the capacitance value. Due to without dielectric layer, the 0 nm device has the highest capacitance value and drastic drop in positive gate voltage induced by leakage current.

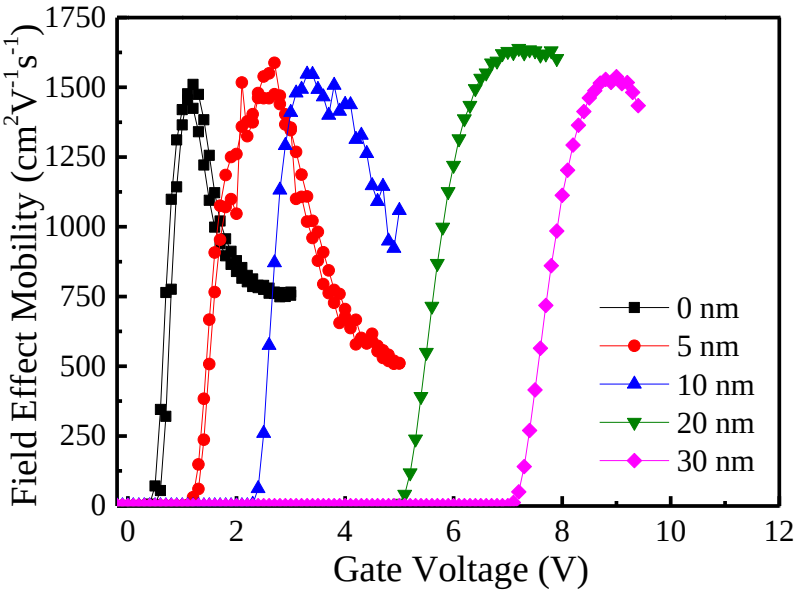


Fig. 4-8 The field-effect mobility of devices with different SiN_x thickness.

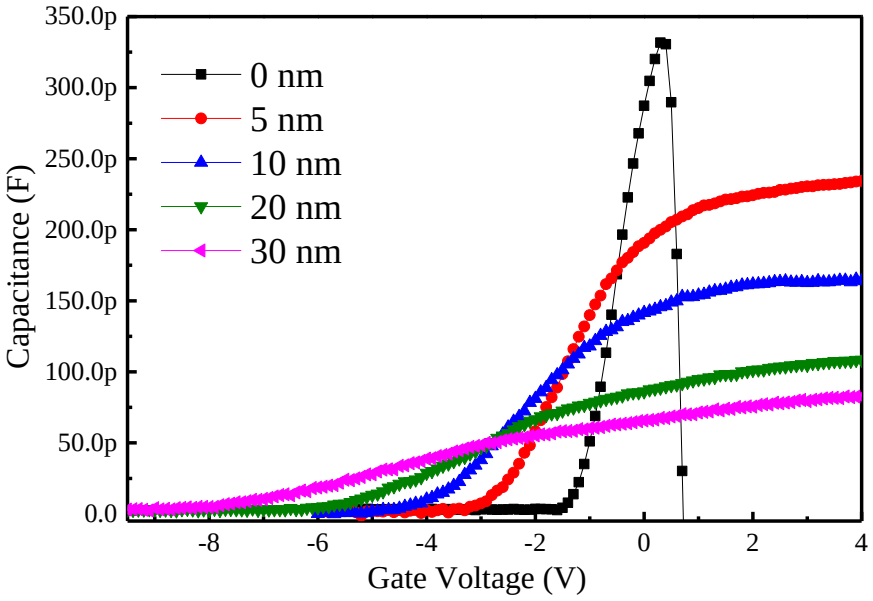


Fig. 4-9 The capacitance-voltage (C-V) characteristics of MIS devices with different SiN_x thickness on recess region.

The field-effect mobility of the normally-on MIS devices is shown in Fig. 4-10. The similar mobility of approximate 800 $cm^2V^{-1}s^{-1}$ is observed with different thickness of SiN_x layer for normally-on MIS devices on access region. The same level 2DEG density can be found in normally-off MIS devices. It indicates that there is a closed channel quality under same process, it has no directly relationship with the thickness of dielectric layer. However, the little low 2DEG density in normally-on MIS device may be due to without SiN_x passivation layer on the access region. And a lower mobility on normally-on MIS devices maybe ascribe to the possible dry etching damage with respect to the normally-off MIS device with p-GaN. Due to the thinner AlGaN barrier layer, the 2DEG quality is more likely to be impacted by the dry etching damage.

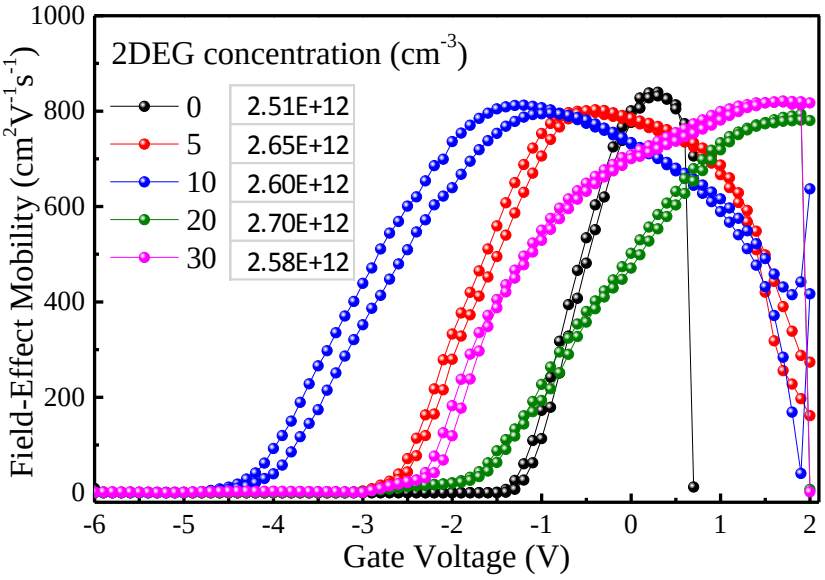


Fig. 4-10 The field-effect mobility of normally-on MIS devices without SiN_x layer.

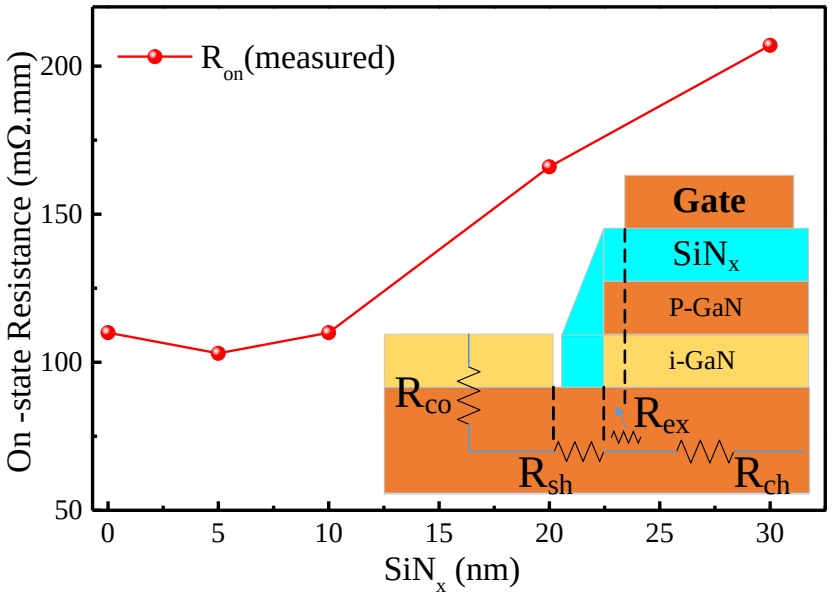


Fig. 4-11 The field-effect mobility of normally-on MIS devices without SiN_x layer.

On the other hand, the influence of the SiN_x layer on on- resistance (R_{on}) is discussed. The calculation of R_{on} is $R_{on}=2R_c+R_A+R_{CH}$. The R_C is the contact ohmic in drain and source, the R_A is the access resistance between gate and drain or source, the R_{CH} is the channel resistance. The resistance model of the device is shown in insert of Fig. 4-11. Due to the same epitaxy structure, the devices has the similar R_{CO}, R_A and R_{CH}. The higher on-resistance in device with 0 nm SiN_x layer is due to the low gate voltage of 3 V. For the similar current density of approximate 14 mA/mm, the R_{on} in normally-off MIS devices is increasing by improving the SiN_x thickness. The possible reason is the extra high resistance part in channel which is induced by incomplete covering of the gate electrode as shown in Fig. 4-11.

§4.4. Conclusion

In conclusion, normally-off junction heterostructure field effect transistors with high threshold voltage and field-effect channel mobility were fabricated. By inserting a SiN_x (thickness varied from 0 to 30 nm) layer between the p-GaN cap and the gate electrode, the threshold voltage positive shift from 1 to 8 V obviously. Besides, the introduction of SiN_x is also beneficial for suppressing the gate leakage current and improving the maximum gate voltage swing owing to the high breakdown field of approximately 8.3 MV/cm. The output current-voltage characteristics show that the device with thicker SiN_x needs a higher gate voltage to reach the same current density. This can be ascribed to that the applied gate voltage would partly appear across the SiN_x layer and partly across the semiconductor. The field-effect channel mobility measurement demonstrated that the SiN_x insulator shows no obvious effect on the 2DEG mobility.

Chapter 5：Normally-off Self-Aligned-Gate MISHFET with Gate First Process

§5.1 SAG structure for normally-off MISHFET with gate first process

Now, Gallium nitride (GaN) and its related AlGaN/GaN heterostructure HFETs have abundant of application in wide fields such as high-frequency, high-power and high-temperature due to the wide bandgap, low intrinsic carrier concentration, high electron mobility and high saturation velocity [113,114]. In common, conventional fabrication processes of the HFETs adopt the ohmic first flow, which is involving patterning and annealing the source and drain contacts before the formation of the Schottky gate contact. It's ascribed to that annealing at high temperature of more than 800 ^{o}C is necessary for forming Ohmic contact. After the formation of the Ohmic contact, gate electrode metal is then patterned and deposited by aligning the Ohmic patterns. Due to the alignment process, this approach limits the minimum source-to-gate and drain-to-gate distances and makes it very difficult to obtain small access resistances. Therefore, a self-aligned-gate (SAG) structure is proposed with the gate first process. Then, the gate and ohmic annealing are processed simultaneously with the ohmic annealing temperature. However, the gate metal electrode can't withstand the convectional high temperature ohmic annealing. Two methods are proposed to address this point. One is to develop the refractory metal nitrides, such as WN, TiN, TaN, and MoN, to stand the ohmic annealing temperature. Another one is to develop the low temperature ohmic annealing that the conventional gate metal can also withstand this temperature.

Different from the normally-on HFETs, the gate region of HFET with p-GaN cap layer has to be defined by the ICP dry etching. On the other hand, due to the limitation of the alignment process, the residual dimensions of p-GaN can't be covered at all by the gate electrode. It may cause the non-uniform potential distribution on the entire p-GaN layer in MIS structure. In general, the ohmic contact gate can obtain a stable electrodes and the uniform potential distribution along the p-GaN layer in normally-off HFETs. Beside the ohmic contact, an alternative approach to alleviate the non-uniform potential distribution in p-GaN layer is the equal dimension vertical gate stacks (SAG gate) by first process which is to employ the gate metal as the hard mask in p-GaN recessing procedure. In our

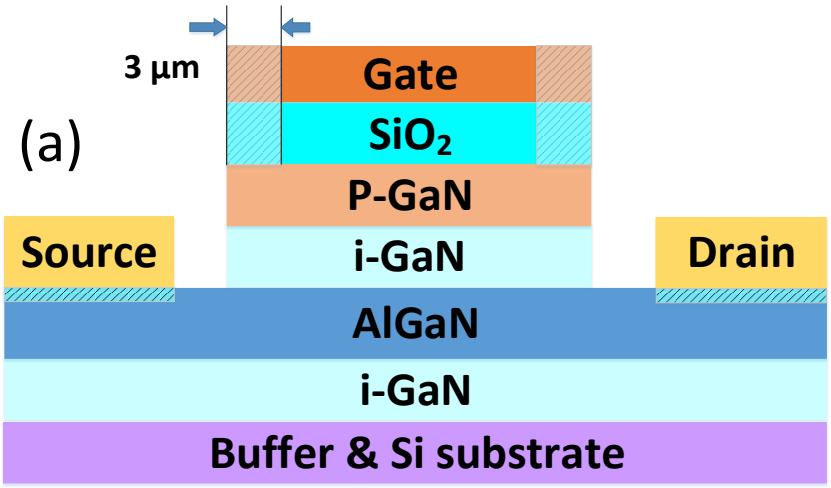
experiment, this SAG process is defined to have a vertical gate stacks from gate metal to p-GaN layer, it's different from the conventional self-aligned gate which has a T-shaped gate. At the same time, to address the high temperature impact on gate during the ohmic annealing, a low-temperature ohmic technique is proposed to avoid the gate degradation in high temperature. On the other hand, microcrystalline in the gate dielectric was also observed during the high temperature ohmic annealing. Therefore, a low temperature ohmic technique is required for the gate-first process to protect the dielectric.

§5.1.1 Fabrication process

The schematic view of epitaxy structure is shown in Fig. 5-1a. A conventional AlGaN/GaN heteroepitaxy structure is grown on a Si substrate by metal organic chemical vapor deposition (MOCVD). The vertical structure of the wafer consists of a buffer layer, a carbon-doped high resistance GaN and an $Al_{0.2}Ga_{0.8}N$/GaN (15/200 nm) heterostructure from bottom to top (Fig. 5-1a). Then, 10 nm i-GaN and 100 nm p-GaN cap layer is grown for normally-off device fabrication. The hole concentration of about 2×10^{17} cm^{-3} in p-GaN was confirmed after high temperature activation, and the activation ratio is around 1- 2%.

The fabrication process is based on the standard photolithography and lift-off technologies. Due to employ the gate first process, after cleaning the wafer by SPM and organic solution, the first step was the MESA with 120 nm depth by inductively coupled plasma (ICP) dry etching. Then the SiO_2 of 10 nm as insulator layer was grown by plasma enhanced chemical vapor deposition (PECVD) at 350 ^oC. And the 950 ^oC for 10 min post-annealing was followed in rapid thermal annealing (RTA). To consider the thermal stability of materials, the TiN/Ni (150/150 nm) as gate metal was formed by lift-off process after magnetron sputter deposition. In conventional gate (CG) device, the gate metal has 3 μm shorter in both side than the SAG device. Meanwhile, the gate metal was also as a hard mask during the SiO_2 wet etching by immersing the BHF solution and the following dry etching by ICP. In CG device, the mask for the SiO_2 wet etching and p-GaN recess process is replaced by the photoresist. The p-GaN recess process with low damage recipe with ICP/Bias of 100/20 W was adopted by $SiCl_4$ gas, then the SAG and CG structure were formed which was shown in Fig. 5-1a. After the ICP treatment on

ohmic region with ICP/Bias 100/100 W at 0.5 Pa for 12s, the Ti/Al/Ti/Au (20/200/40/40 nm) ohmic metal stack was deposited by magnetron sputter. The ICP treatment was to make enough damages (nitrogen vacancy) in ohmic contact region. Then the annealing at 500 ^{o}C for 20 min in N_2 ambient was done for the ohmic contact.



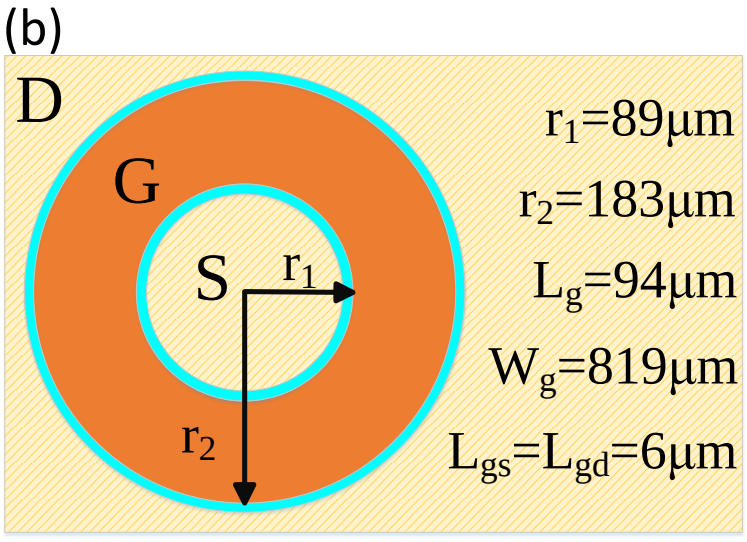


Fig. 5-1 The schematic diagram of (a) device with the SAG and the CG structure, and (b) dimensions of the device.

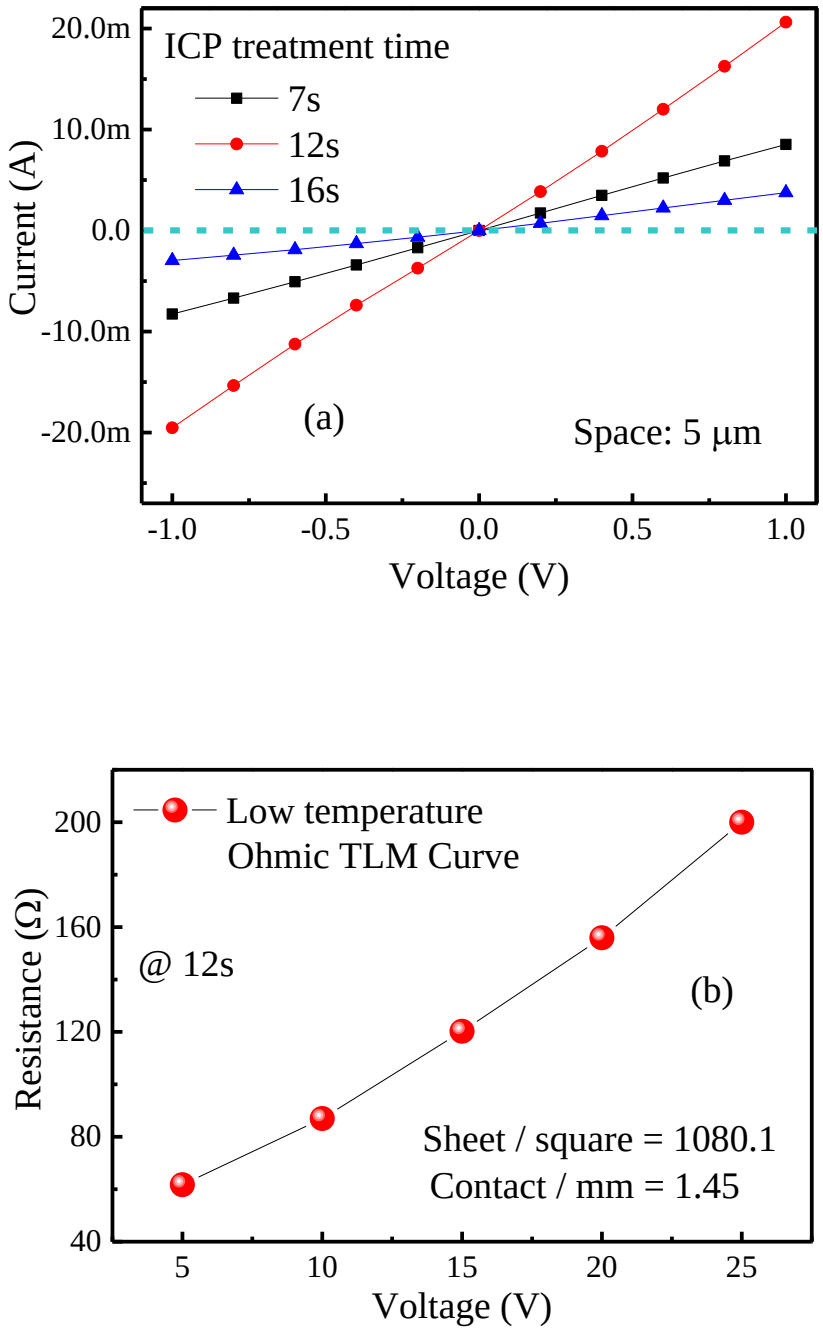


Fig. 5-2 I-V characteristics with different ICP treatment time (a) and inset shows the ohmic result by fitting TLM curve (b).

The principle of low temperature ohmic by ICP assistant is to make enough damages (nitrogen vacancy) in ohmic contact region. The N vacancies induced by ICP treatment is confirmed in our previous work. A higher bias power will lead to more damage (V_N) and much prefer to low-temperature ohmic contact.

In process, the ICP gas is $SiCl_4$. However, similar to the $SiCl_4$ gas, other gases such as BCl_3 and Cl_2 gas can also induce N vacancies through dry etching. We adopted $SiCl_4$ gas for low-rate etching (around 10 nm/min) and accurate control of the etching depth.

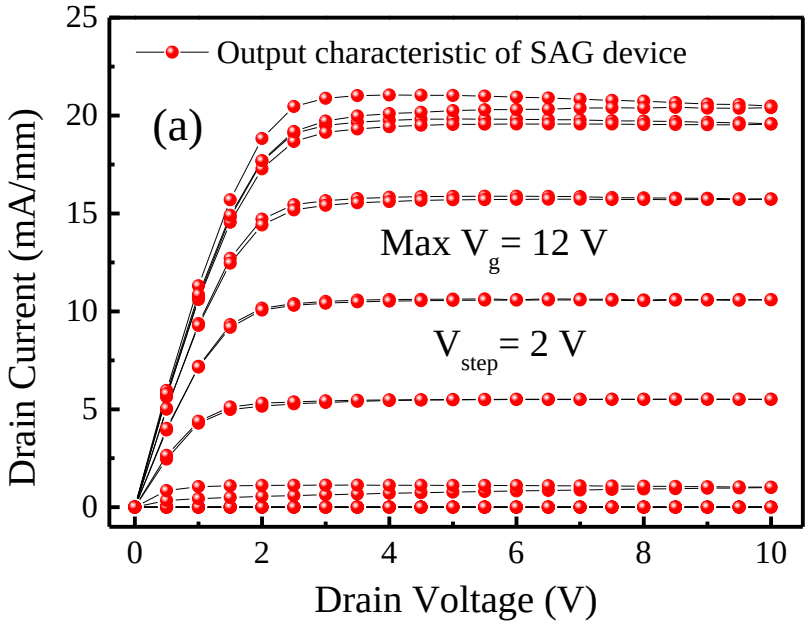
Compared with the N vacancies induced by ICP treatment, we confirmed that the Si containing is only existing on the surface and not as a dopant. The main reason for achieving the low-temperature ohmic contact is the donor-like N vacancies instead of the Si contamination. Then the annealing at 500 ^oC for 20 min in N_2 ambient was done for the ohmic contact.

For the ICP assistance, the treating time is important for N vacancies production which has a closed relationship with ohmic contact. Therefore, different treating time of 7, 12 and 16 seconds is investigated. The I-V curves for 7, 12 and 16 second is shown in Fig. 5-2a with the ohmic electrode of 5 μm spacing. Firstly, this figure illustrates that the ICP assistance for ohmic contact is an effective method. Then, from the I-V characteristics, the 12 s has a higher current than 7 s. Nevertheless, the current curve of 16 s become lower than 7 s, it may be due to the AlGaN barrier of 10 nm removing by ICP/Bias of 100/100 W for 16 s. So the ICP treating time of 12 s is the more preferable for ohmic contact.

The result of the low temperature ohmic process was investigated. In this process, the dry etching treatment by ICP/Bias of 100/100 W for 12 s and annealing condition of 500 ^oC for 20 min in N_2 ambient were defined as the low temperature ohmic recipe. Then the transmission line model (TLM) was adopted to evaluate the ohmic contact. The Fig. 5-2b shows the TLM fitting curve of the low temperature ohmic. A sheet resistance of 1080.1 Ω/□ and a contact resistance of 1.45 Ω·mm is obtained. It means that this low temperature ohmic recipe is valid to obtain a good ohmic contact in MIS-HFETs with p-GaN cap layer fabrication process.

§5.1.2 Device characteristics of SAG and CG structure

The output current-voltage (I_d-V_{ds}) characteristics of the SAG device is shown in Fig. 5-3a with V_g from -3 to 12 V in which the gate length L_g and effective gate width W_g are 94 and 819 μm, respectively (Fig. 5-1b). The maximum current density of the SAG device in Fig. 5-3a is around 21 mA/mm in V_g of 12 V. And the good pinch-off performance can be observed with gate bias up to 12 V due to the SiO_2 insulator layer. Meanwhile, the output current-voltage (I_d-V_{ds}) characteristics of CG device is also shown in Fig. 5-3b. The maximum current density in V_g of 12 V is just 3.7 mA/mm, there's a significant decreasing for the CG devices with respect to the SAG device by the same ohmic contact and p-GaN dimension. The same condition is also appeared in transfer characteristics and transconductance curves of SAG and CG structure in Fig. 5-4a and 4b. Due to the existing of the SiO_2 insulator layer, the V_{th} of SAG is 2 V. However, the CG device has a higher threshold voltage of 2.5 V by fitting the linear transfer characteristics curve, but the lower transconductance value. On the other hand, the second peak in transconductance curve of CG device at around 7 V is observed, it may be due to the channel opening at uncover position under p-GaN layer.



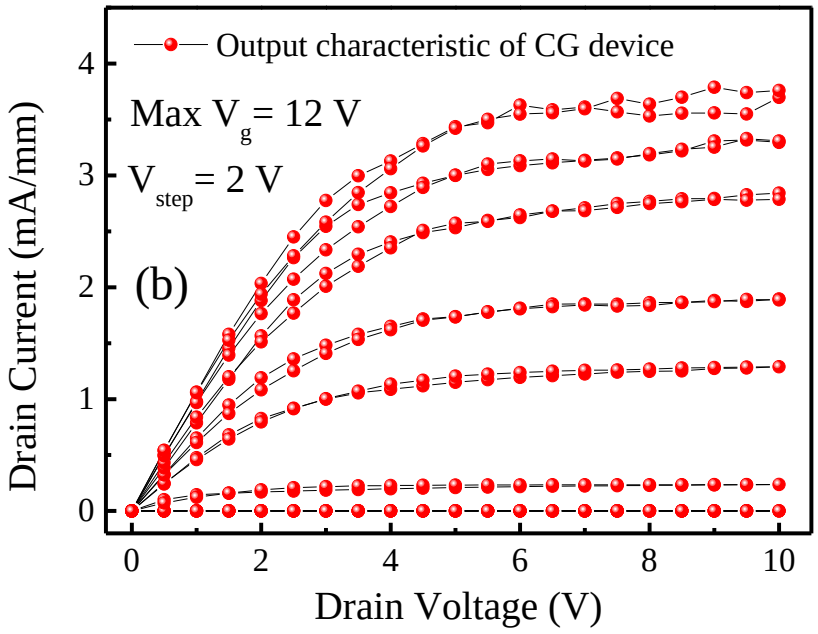
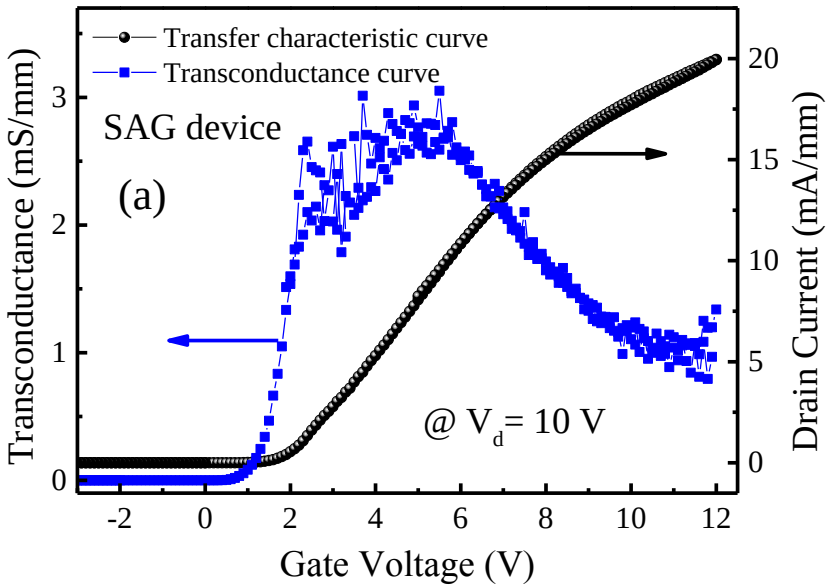


Fig. 5-3 Output characteristics of devices with SAG structure (a) and CG structure (b).



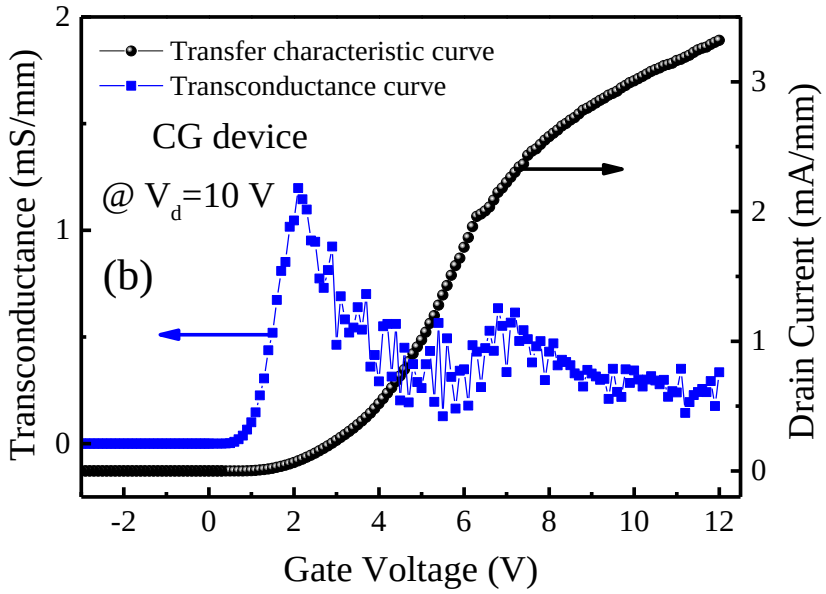


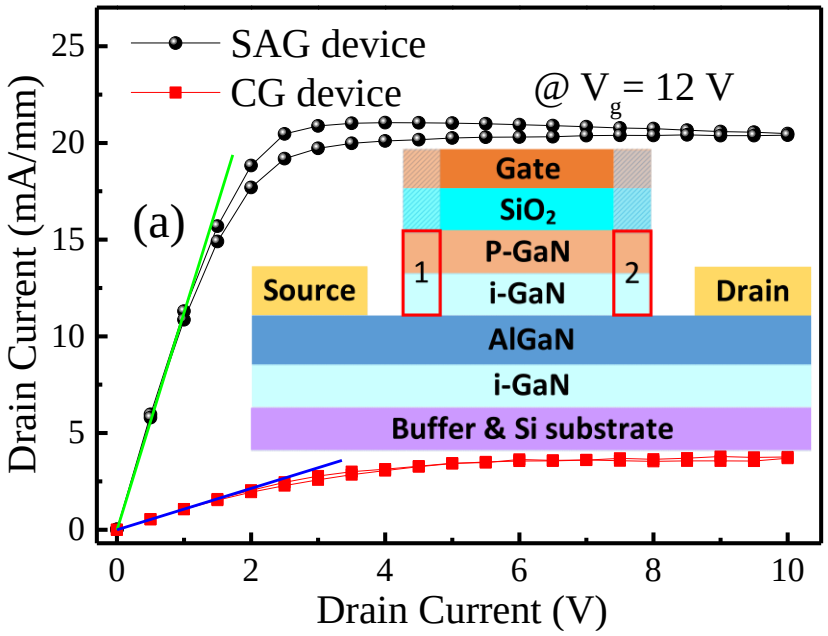
Fig. 5-4 Transfer characteristics and transconductance curves of SAG structure (a) and CG structure (b).

To investigate further the effect of gate dimension parameters, the on-state resistance (R_{on}) was extracted from the slope of linear region of the output characteristics curves of 12 V gate voltage in Fig. 5-5a. The lower R_{on} can be obviously observed in the SAG structure. It means that the CG device has the larger channel resistance than the SAG device. The inset in Fig. 5-5a is the epitaxy structure of the SAG and CG device. To a normally-off AlGaN/GaN heterostructrue HFET with p-GaN cap layer, the conduction band of AlGaN/GaN heterostructure channel is start to below the Fermi level. And the two-dimensional electron gas (2DEG) is accumulated in the channel when the V_g is above the V_{th}. In principle, to the SAG structure, the electric potential formed by gate voltage could apply to all of p-GaN layer. And the 2DEG is induced by the gate voltage in the channel which is equal to the p-GaN length. To take into account the CG epitaxy structure, the 1 and 2 region of p-GaN can't be applied directly by the gate voltage due to no electrode cover compare to the SAG structure. When the gate bias is equal to the V_{th}, the channel electron beneath the gate electrode is accumulated as well. Nonetheless, the

channel beneath the 1 and 2 region is in semi-open of the state, there isn't enough electron in the channel. And these region may be opening partly at higher gate voltage. In other words, there always exist the relatively less 2DEG with respect to the same position in SAG structure, hence there is high channel resistance and the lower current density in CG structure. However, the high channel resistance also obtain low device leakage current. The semi-log transfer and gate current-voltage characteristic is shown in Fig. 5-5b. The lower leakage current in off-state of transfer characteristic and forward direction of gate I-V characteristic is confirmed.

On the other hand, the investigation of on-resistance in device is also processed by the simulated with silvaco. At gate of 6 V and drain of 10 V, the electrical field simulated result is shown in Fig. 5-6 (a is for SAG, b is for CG). The significant electrical field difference at SAG and CG gate can be observed under dielectric layer. The SAG structure have more regional electric field than CG structure at operation.

Then, the capacitance-voltage (C-V) characteristics of SAG and CG device is shown in Fig. 5-7. The similar capacitance curve and value could confirm that the SAG and CG have the same dielectric thickness and AlGaN/GaN heterostructure. And the higher V_{th} observed in CG device coincide with the higher channel resistance conclusion.



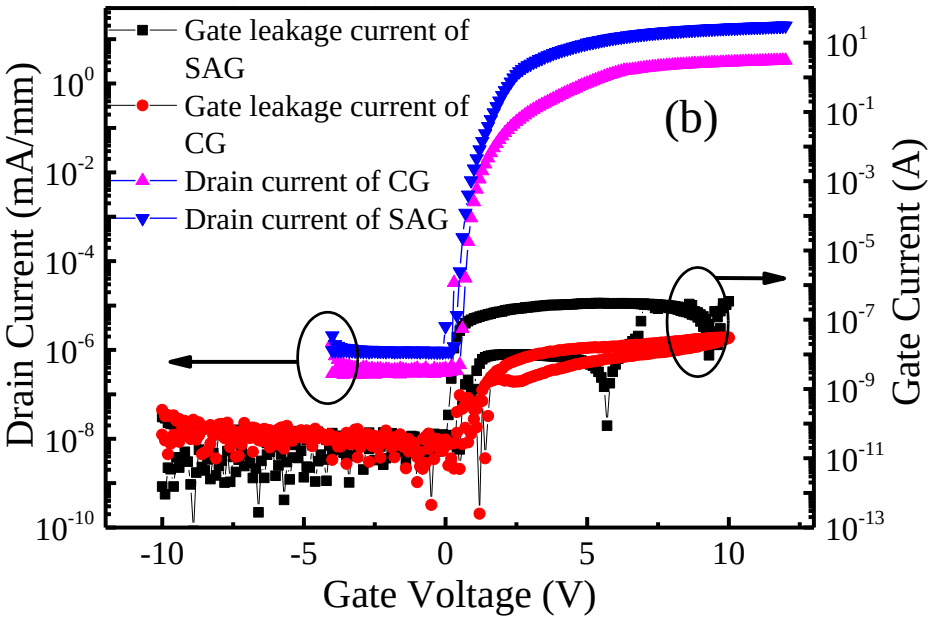
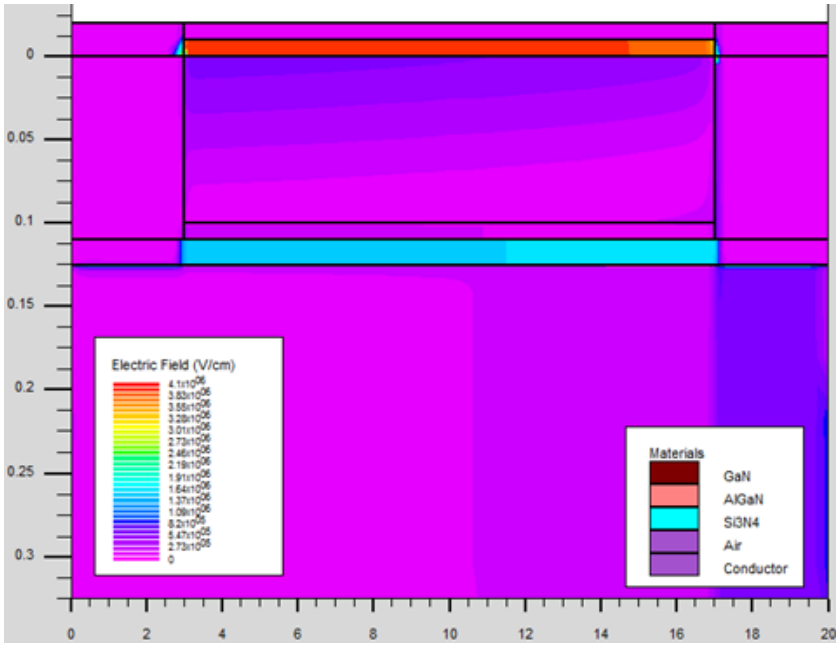
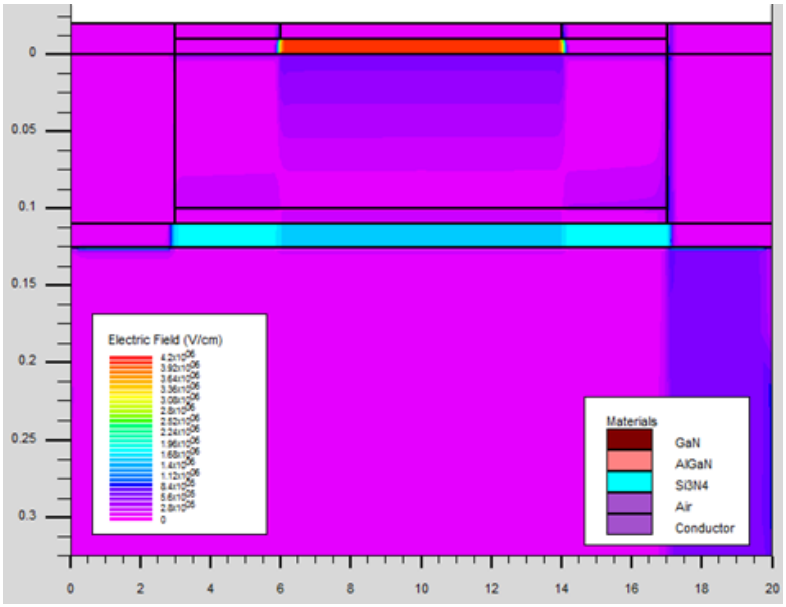


Fig. 5-5 (a) On-state resistance, and (b) the semi-log transfer and gate current-voltage (I_d-V_{ds}) characteristics for SAG and CG structures.



(a)



(b)

Fig. 5-6 The electric field simulated diagram for SAG device (a) and CG device (b) at gate of 6 V and drain 10 V.

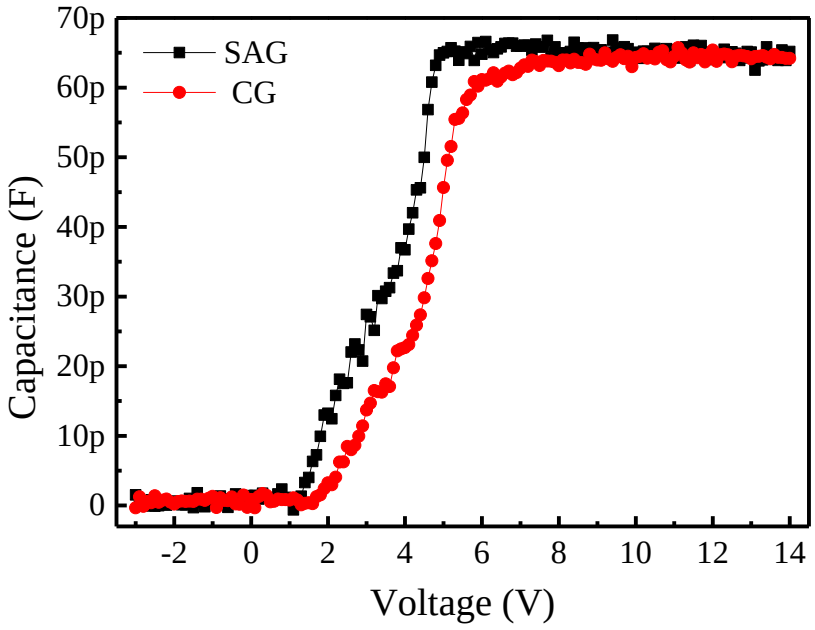


Fig. 5-7 The capacitance-voltage characteristics of SAG and CG device.

§5.2. Normally-off SAG MISHFET with SiN_x insulator

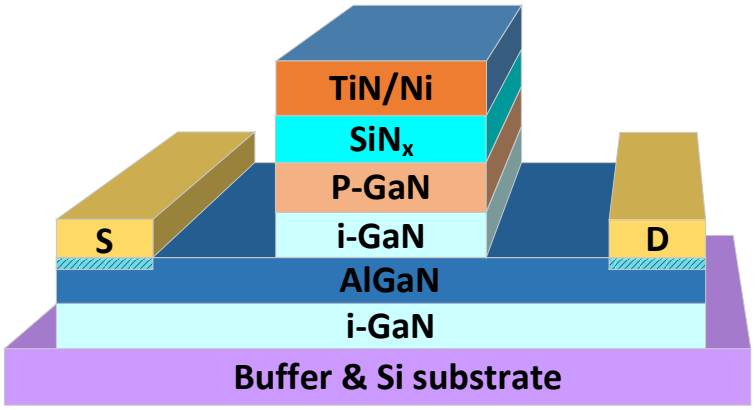
According to previous research, the normally-off SAG MISHFETs have a more stable output characteristic and repeatability than conventional MISHFETs with p-GaN cap layer. However, due to the 10 nm SiO_2 insulator layer, the gate swing is limited to about 12 V. At the same time, there would induce a complex interface states between the oxide dielectric film and p-GaN layer according to the research result from other group, the interface states has a significant impact on device performance. Therefore, the non-oxide dielectric film is recommended as the inserting layer between p-GaN and gate metal electrode.

For increasing the output current density further and achieving a preferable performance, a 50 nm thickness of SiN_x is adopted as the insulator to replace the SiO_2. It's also for avoid the influence of high temperature on device characteristics during the post annealing at 950 ^oC for SiO_2. On the other hand, Schottky contact on p-GaN with a lower work function metal can help to increase the V_{th} and enable a reduction of the gate leakage current. However, the Schottky contact presents obvious degradation after annealing at a temperature of 400 ^oC during the gate first process. At a high-temperature annealing, it can be expected that the Schottky contact will have much serious degradation. The low temperature ohmic process is essential to the normally-off HFETs with Schottky contact on p-GaN. However, the necessity of low temperature ohmic process need to be discussed in different device structure. And a metal gate as comparison is also fabricated by the gate first process.

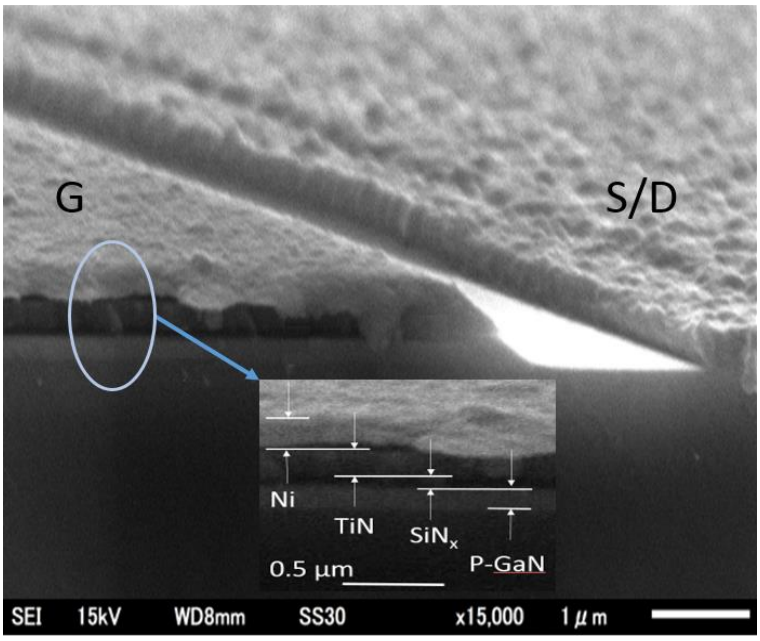
§5.2.1 Fabrication process

The schematic view of device structure is shown in Fig. 5-8a. The gate first fabrication process is based on the standard photolithography and lift-off technologies. Device isolation was conducted by ICP dry etching with an etching depth of 120 nm. Then, 50 nm SiN_x was grown as an insulator layer by plasma enhanced chemical vapor deposition (PECVD) at 350 ^oC followed with a 600 ^oC post-annealing for 10 min in N_2 ambient. Finally, Ni/TiN (150/150 nm) gate stack was formed by magnetron sputter deposition and lift-off process. The p-GaN was removed by a low damage recipe with ICP/bias of 100/20 W and $SiCl_4$ etching gas. After that, ICP treatment on ohmic region was done with

ICP/bias 100/100 W at 0.5 Pa for 12 s. Ti/Al/Ti/Au (20/200/40/40 nm) ohmic metal stack was then deposited by magnetron sputtering. With the assistance of the ICP treatment, ohmic contact was obtained when annealing at 500 °C for 20 min in N_2 ambient. The cross section scan electron microscope (SEM) image of the structure is shown in Fig. 5-8b, indicating clearly the different layers.



(a)

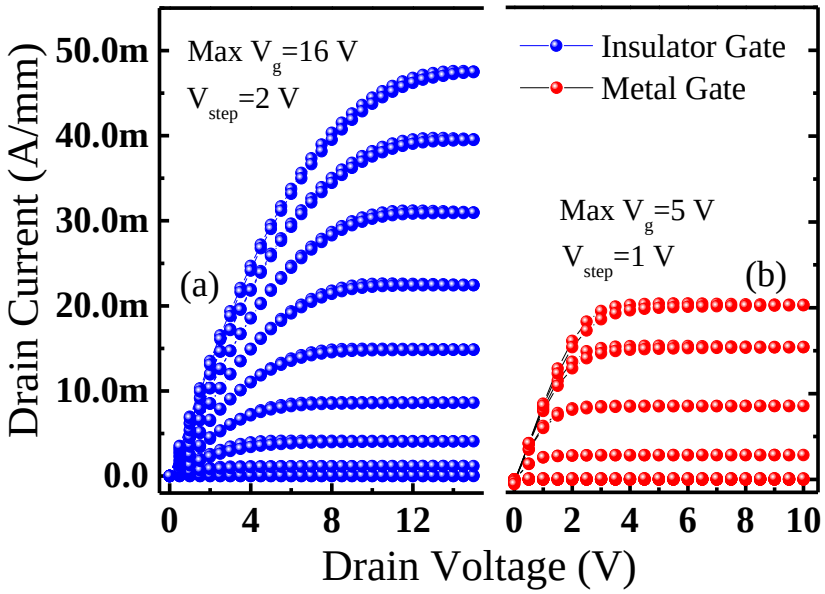


(b)

Fig. 5-8 (a) Schematic of device epitaxy structure, (b) the cross section SEM image of the structure.

§5.2.2 Characteristics of the SAG structure

Ring-type devices were adopted to evaluate the device performance in order to avoid the affect from the isolation region, as shown in inset of Fig. 5-9c. The output current-voltage (I-V) characteristics of the devices are shown in Fig. 5-9a and 9b with the gate voltage (V_g) swept from -2 to 16 V for insulator gate device and -3 to 5 V for metal gate device, in which the gate length L_g and effective gate width W_g are 94 and 819 μm, respectively (Fig. 5-9c inset). Good pinch-off characteristics can be observed with gate bias up to 16 V and 5 V for two devices. The maximum current density of the insulator gate device is around 47 mA/mm at a V_g of 16 V. No visible hysteresis in the output curve can be found, it's possible that the damage induced by ICP dry etching alleviate the dispersion effect after the SiN_x film removed. Obviously, the gate swing increases to 16 V due to the existence of the SiN_x insulator layer. The semi-log transfer and gate I-V characteristics is shown in Fig. 5-9c. The threshold voltage (defined as I_d=0.1 mA/mm) are 2 and 1 V for insulator and metal gate devices. More than the 10^8 on-off ratio is also observed. Positive shift of Vth for insulator gate device is also confirmed from the transfer characteristic of the √ I_d-V_g plot (not shown). Furthermore, the reason of positive shift for V_{th} is the larger turn-on resistance due to the insulator film, which can be confirmed around 0.1 mA/mm at semi-log curve. And for the same reason, the gate current in insulator gate is much less than the metal gate which the gate current reach the 1 mA/mm at gate voltage of 3 V.



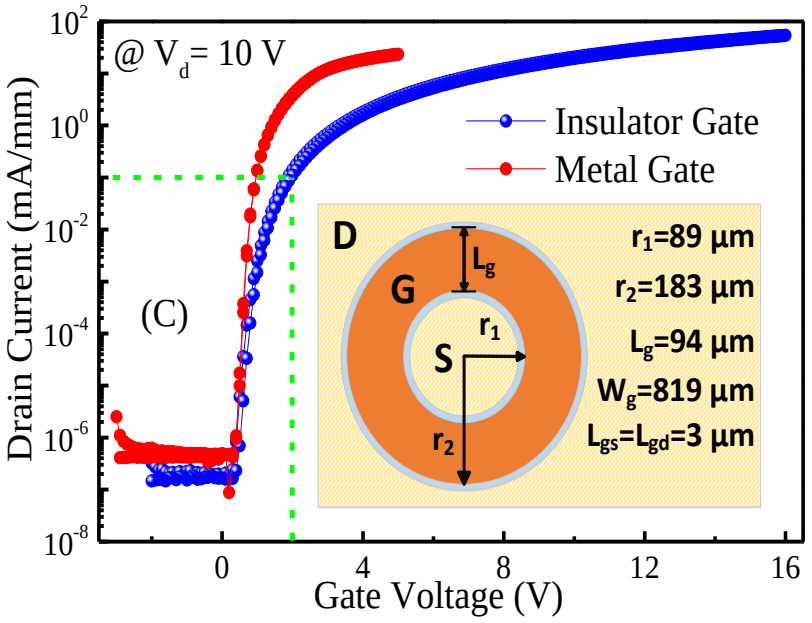
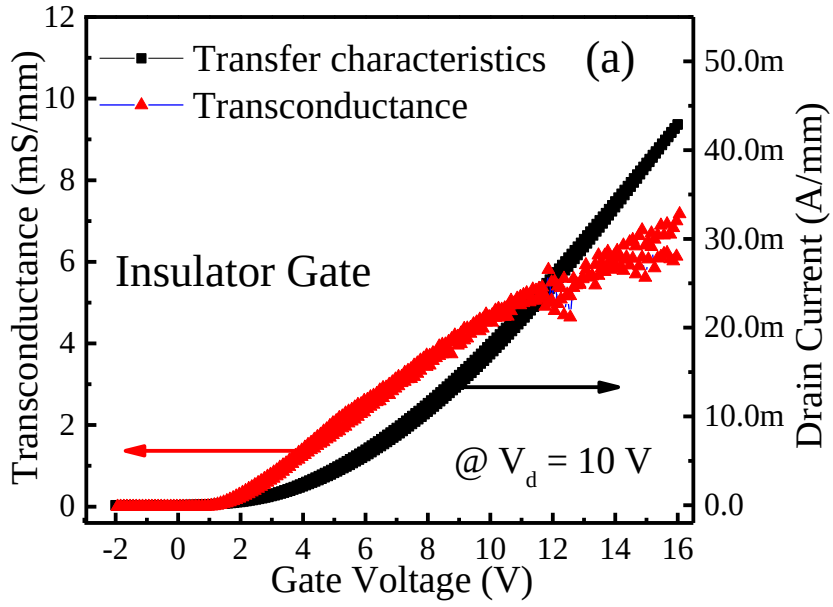


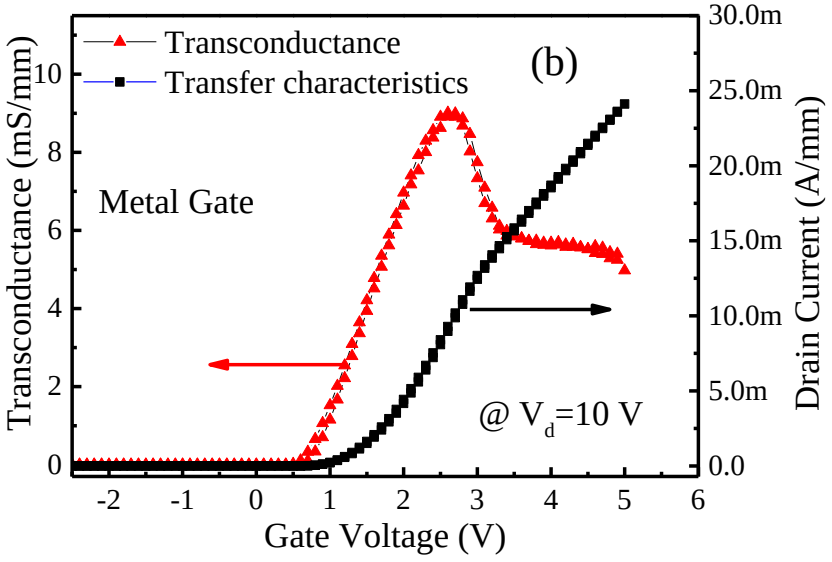
Fig. 5-9 (a), (b) The output characteristics and (c) semi-log transfer characteristic of insulator gate and metal gate.

The positive shift for V_{th} is due to that part of the voltage will drop in the insulator layer. The transfer characteristic and the transconductance of the insulator gate and metal gate device are shown in Fig. 5-10a and b. Owing to the existence of the p-GaN cap layer and the SiN_x layer, the value of the threshold voltage has an obvious positive shift. The metal gate has the higher transconductance value of 9.3 mS/mm and the rate to reach the peak with respect to the insulator gate device, that the low transconductance value in insulator gate is ascribed to the far distance from gate electrode to 2DEG channel and the long gate length. By alternating the SiN_x dielectric with high-k dielectrics and shrinking the gate length, the device performance can be further improved.

To clarify the necessity of the LT ohmic technique, we compare the gate I-V characteristics for the insulator gate device with high-temperature (HT: 850 °C) and LT (500 °C) ohmic annealing as well as the metal gate device with LT ohmic annealing (Fig. 5-10c). The gate leakage current of the metal gate device presents rectification behavior with a drastic increasing leakage after the turn-on of the p-n junction between p-GaN and

AlGaN/GaN. The introduction of dielectric through LT ohmic process can suppress the gate leakage current effectively, especially in the forward bias region. However, for the insulated gate device, high temperature ohmic annealing causes an obvious degradation on the gate leakage current. The possible reason is that microcrystalline structure appears in SiN_x dielectric after ohmic annealing at high temperature.





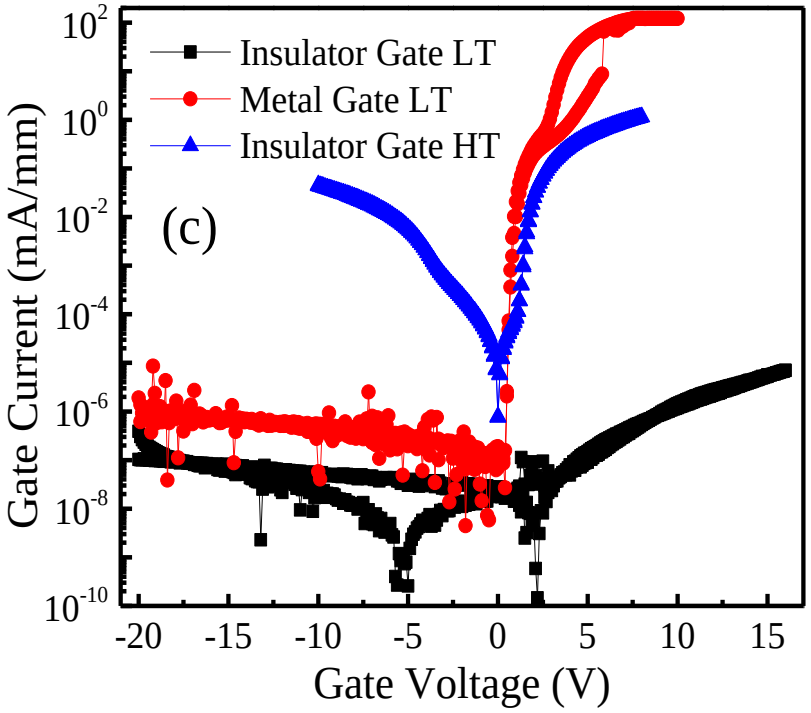


Fig. 5-10 The linear transfer and transconductance characteristic for insulator gate (a) and metal gate (b), and (c) gate current-voltage characteristics in different ohmic process conditions.

For confirming the SiN_x degradation in high temperature, the MIS-HFET with 20 and 30 nm SiN_x dielectric layer were fabricated as comparison, which was without the post-annealing at 600 ºC for 10min. And the ohmic annealing is 600 ºC for 15min to them. The transfer and gate current-voltage (I-V) characteristics are shown in Fig. 5-11a. No matter with or without the 600 ºC post-annealing process, the device with only ohmic annealing at 600 ºC for 15min also have an low leakage current which is similar to the 50 nm device. However, when the annealing temperature is raised to 800 ºC, the obviously leakage current can be found at reverse and forward direction in Fig. 5-10c. Therefore, from the gate leakage current, it's confirmed that the annealing less than 600 ºC don't cause the performance degradation. Furthermore, the transfer characteristic of the insulator gate with HT ohmic process is shown in Fig. 5-11c. The high reverse leakage current can be also observed after the HT ohmic process.

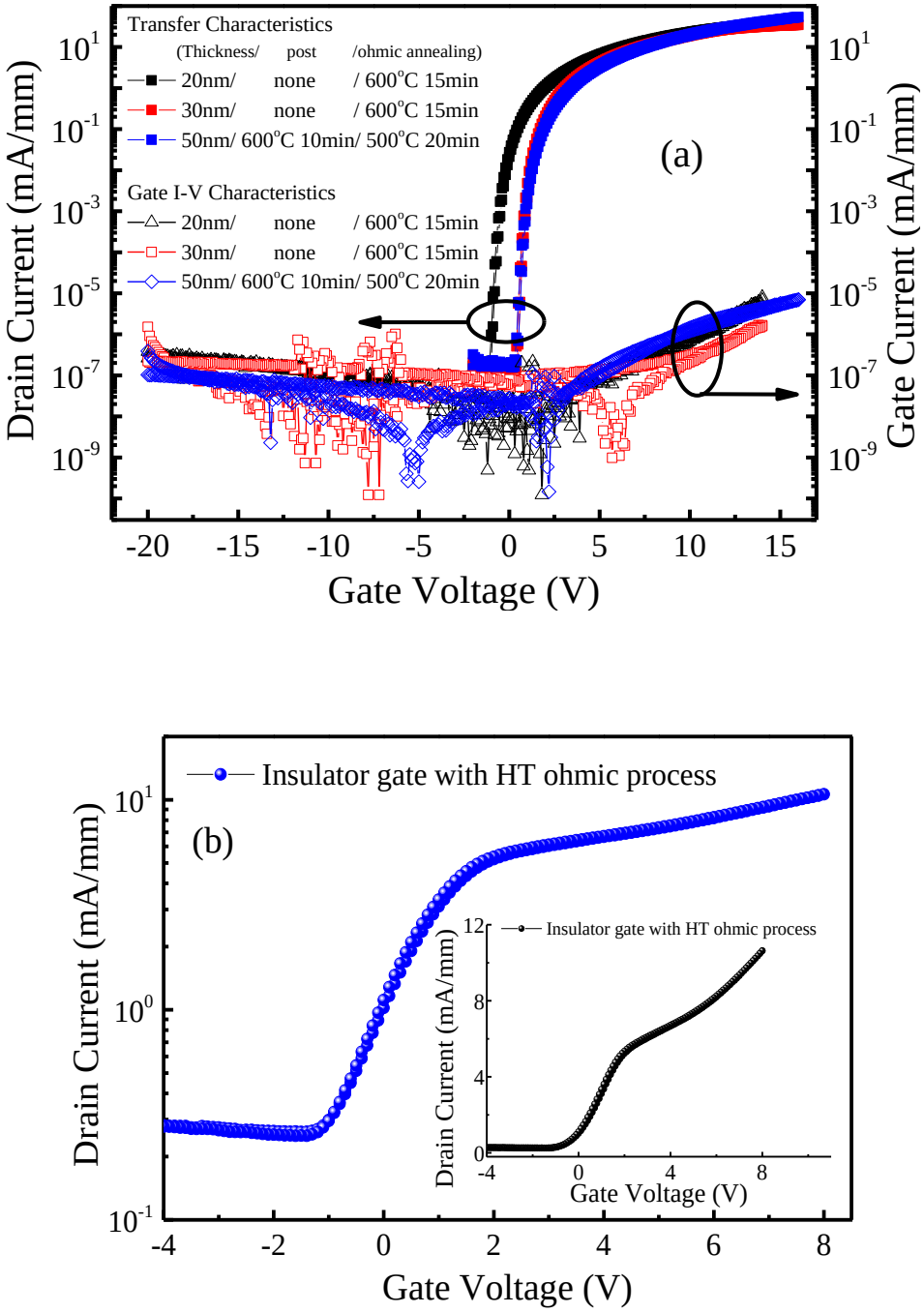


Fig. 5-11 (a) The transfer and gate current-voltage (I-V) characteristics in different annealing process, (b) transfer characteristic of insulator gate with HT ohmic process.

Generally, there is hydrogen in the ambient during the PECVD growth of SiN_x film, which may decrease the hole concentration in the p-GaN. The p-GaN diode is fabricated with a Schottky anode of tungsten (W) metal. Due to the low metal work function of W, the interface is Schottky contact between W metal and p-GaN layer which has the higher fermi energy level. To investigate the influence of hydrogen on p-GaN concentration, different PECVD process was adopted, that is with/without PECVD process (SiN_x film was removed by wet etching for device with PECVD process). By means of Schottky diodes fabricated as shown in inset of Fig. 5-12a, the capacitance-voltage (C-V) curves with different PECVD process are shown in Fig. 5-12. The C-V measurement can also be used to study impurity level. According to the depletion width (W_D) equation (as shown in equation 5-1) for a metal semiconductor contact.

$$W_D = \sqrt{\frac{2\varepsilon_S}{qN_D}\left(\varphi_{bi} - V - \frac{KT}{q}\right)} \tag{5-1}$$

Where the N_D is the donor concentration, ε_s is the permittivity of semiconductor, φ_{bi} is built-in potential, V is the applied voltage. Therefore, the capacitance of the depletion layer can be arise from equation 5-1,

$$C_D \equiv \frac{\varepsilon_S}{W_D} = \sqrt{\frac{q\varepsilon_S N_D}{2[\varphi_{bi} - V - (KT/q)]}} \tag{5-2}$$

Equation (5-2) can be written in the from

$$N_D = \frac{2}{q\varepsilon_S}\left[-\frac{1}{d(1/C_D^2)/dV}\right] \tag{5-3}$$

Then, we can deduce the doping concentration from the C-V characteristics. According to the capacitance-voltage (C-V) curves in Fig. 5-12a, the hole concentration in bulk p-GaN are deduced to approximately 1.66×10^{17} and 1.45×10^{17} cm^{-3} (as shown in Fig. 5-12b) for device without and with PECVD process, respectively. Hole at the surface of the p-GaN (approximately 20 nm) is depleted due to the surface depletion.

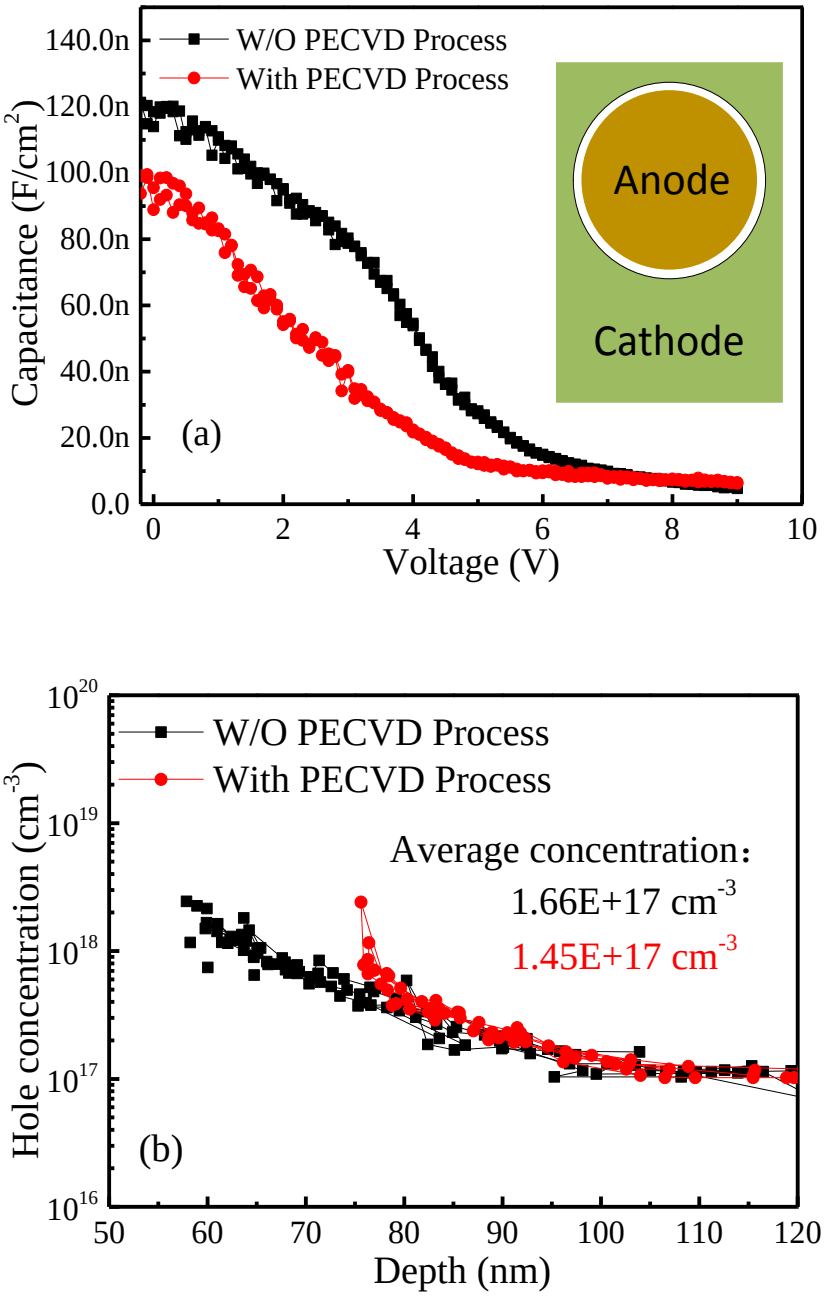


Fig. 5-12 (a) The Capacitance-Voltage (C-V) characteristics of the Schottky diode with/without PECVD process, (b) the hole concentration curves for Schottky diode with/without PECVD process.

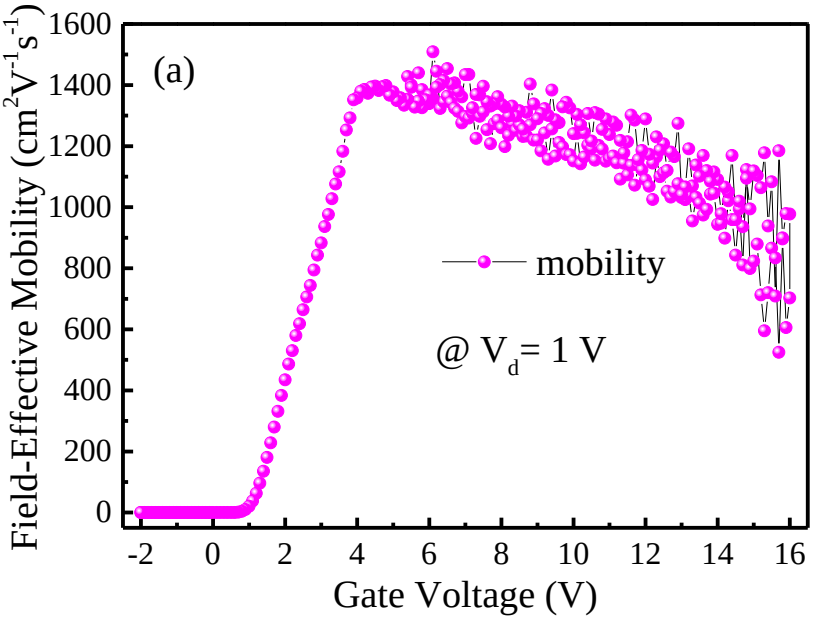
The field-effect channel electron mobility (μ_{FE}) of the device with insulator gate was measured and plotted in Fig. 5-13a based on a capacitance-transconductance method. A maximum field-effect mobility is around 1500 $cm^2V^{-1}s^{-1}$. This result is comparable with

the original HFETs, indicating that the combination of SiN_x dielectric layer and gate-first process is a promising way to fabricate a normally-off device with good performance. Besides, the existence of dielectric will increase the distance between gate electrode to the 2DEG channel. While the high mobility is mainly ascribed to the relatively low 2DEG concentraton because the $Al_{0.2}Ga_{0.8}N$ (15 nm) barrier presents a relatively thin thickness and low Al% content in the p-GaN device compared with the conventional heterostructure. The equation related to the 2DEG concentration and mobility is shown in equation 5-4

$$\mu = \frac{1}{nqR_{sheet}} \tag{5-4}$$

where μ is the mobility, n is the 2DEG concentration, Rsheet is the sheet resistance, and q is equal to 1.6×10^{-19}C. The 2DEG concentration is less than $4\times10^{12}cm^{-3}$ by the calculation, that coincide with the measurement result by hole method.

Moreover, as provided in Fig. 5-13b with different L_{gd} and V_g of 0 V, the off-state breakdown voltages are 133, 280, 670 V corresponding to the L_{gd} of 3, 6, 9 μm, respectively, at the I_{ds} of 1 mA/mm. The breakdown voltage is acceptable although the leakage current is relatively high at the small L_{gd}. The off-state breakdown properties can be further enhanced by optimization the surface passivation process in future.



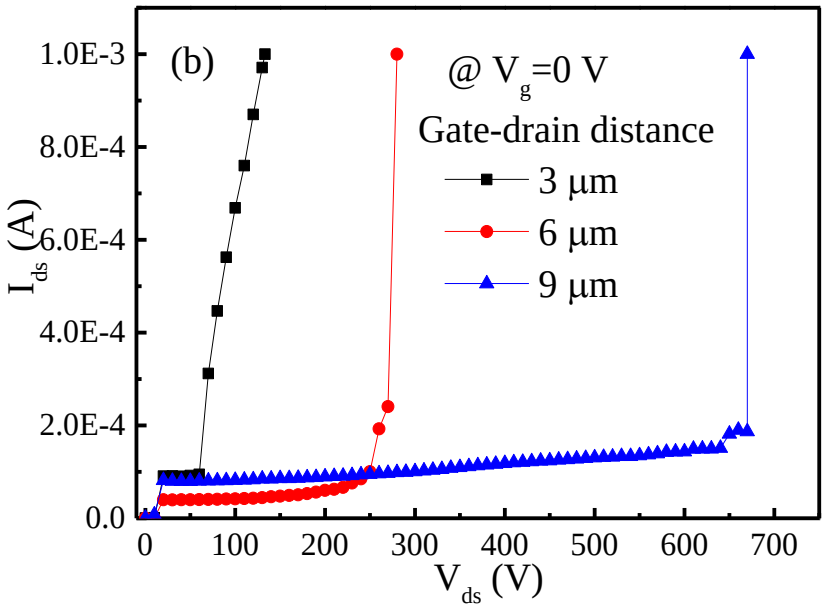


Fig. 5-13 (a) the field-effect mobility of the device with insulator gate device, (b) the off-state breakdown voltages of the devices with different L_{gd}.

The subthreshold swing (SS) for insulator gate and metal gate are also demonstrated in Fig. 5-14 (a) and (b). Compared to the Terman method, the I-V method is more convenient to calculate the interface state density by using the subthreshold characteristics and capacitance as shown in equation (1). The equivalent circuit of the MIS-HFET structure can be expressed as the gate dielectric capacitance C_{ox} connected in series with an interface-related capacitance C_{it}. In this case, the subthreshold swing (SS) can be calculated as

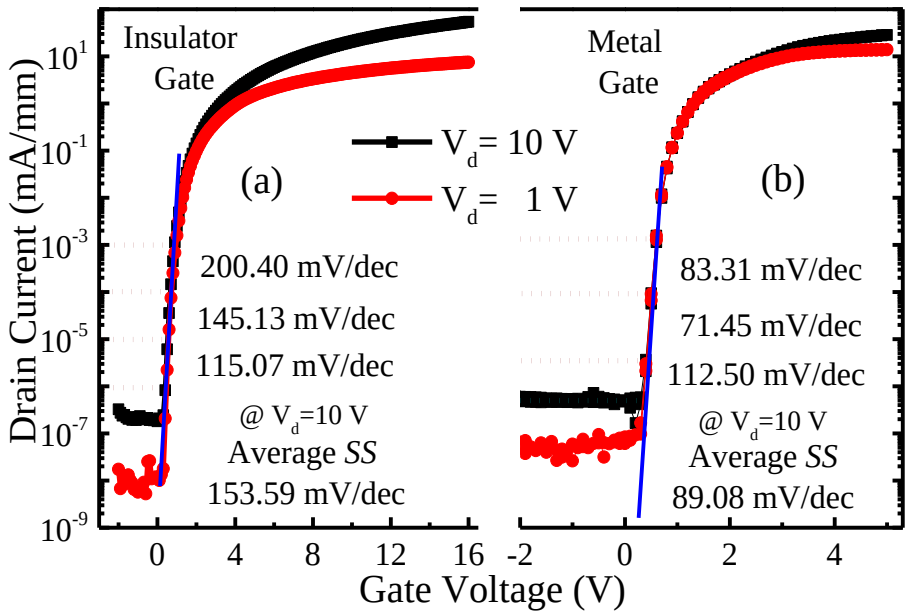
$$SS = \frac{dV_g}{d\log I_{DS}} = (\ln 10)\left(\frac{kT}{q}\right)\left(1 + \frac{C_{it}}{C_{OX}}\right) \quad (1)$$

where k is the Boltzmann constant, T the absolute temperature, and q the electron charge. When Cit is known, the interface state density Dit can be obtained by the equation (2).

$$D_{it} = \frac{C_{it}}{q^2} \quad (2)$$

A higher average SS of 153.59 mV/dec (@V_d =10 V) is observed in the insulator gate device, while 89.08 mV/dec for the metal gate one. Meanwhile, the corresponding capacitance of the insulator and metal gate device are approximately 33.2 and 98.7 pF, respectively. The interface density (D_{it}) of insulator gate device is about 3.31×10^{12} $cm^{-2}\cdot eV^{-1}$ using the SS and capacitance.

Finally, the stability measurement for the insulator gate device was carried out. The semi-log transfer characteristics after stressed for 1000s (V_g = V_d = 10 V) at RT (25 ºC) and HT (150 ºC) are plotted in Fig. 5-14c. The curve of stressed device at RT with stress for 1000s is almost coincide with the curve at RT. However, a slight positive shift in subthreshold region and decrease of drain current can be found after HT and HT with stress for 1000s. It indicates that the HT has a much more influence on device performance than stress. Besides, a clockwise hysteresis is observed, implying that the electron trap is responsible for the current collapse. Electron trap is expected to exist at the interface of SiN_x/p-GaN. Under the gate bias, the electron in 2DEG channel will be trapped by the interface defects, resulting in a decreasing output current and positive shift of V_{th}.



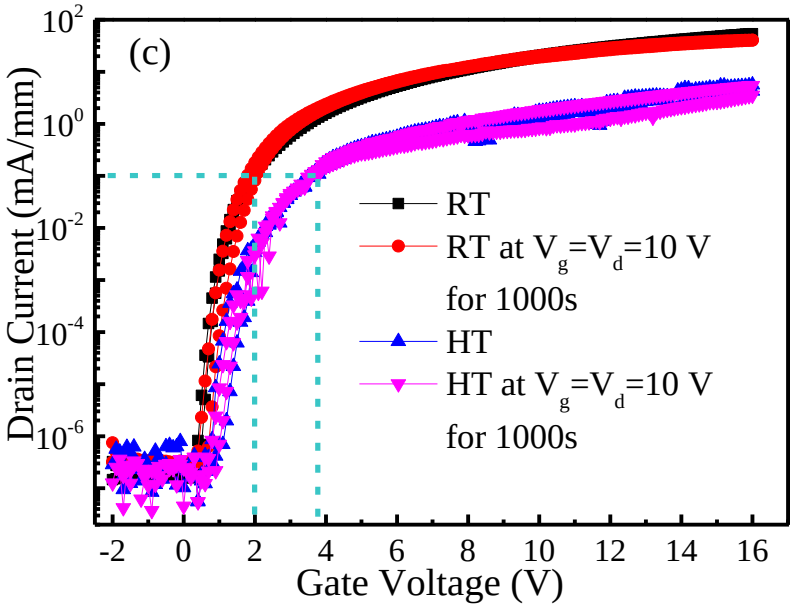


Fig. 5-14 (a) gate current-voltage characteristics in different ohmic process, (b) transfer characteristic of insulator gate with HT ohmic process, and (c) the stable test and diode C-V characteristics in inset.

§5.3 Conclusion

In conclusion, the normally-off MISFETs were demonstrated with the self-aligned-gate (SAG) and the conventional gate (CG) by the gate first process. The good ohmic contact of 1.45 Ω·mm contact resistance was obtained by the low-temperature ohmic technique. By employing the SiO_2 as the insulator layer, the V_{th} is close to 2 V in SAG device. Due to the difference of gate structure in SAG and CG device, the device performances were investigated. And the high channel resistance owing to the non-applied voltage region of p-GaN in CG device was discussed. It means that the SAG structure is the more advanced to achieve the good performance in normally-off MISFETs with p-GaN cap layer.

Further, based on the low temperature ohmic process, a normally-off HFETs with SiN_x insulator layer and gate-first process was fabricated. Good pinch-off characteristics with threshold voltage of 2.0 V and a field-effect mobility of 1500 $cm^2V^{-1}s^{-1}$ were achieved. And the gate leakage current was remarkably suppressed. The low-temperature ohmic process also exhibits a capability of solution to alleviate the gate degradation during the high-temperature annealing in a gate-first process.

Chapter 6: Conclusions and Future Works

§6.1 Summary and conclusions

P-GaN gate is a promising candidate method to achieve the normally-off operation. However, the Mg^+ out-diffusion would happened in relatively high epitaxy temperature. Then the blocking layer is essential to alleviate the 2DEG degradation from the Mg^+ out-diffusion. According the experiment result, the 20 nm i-GaN layer is the suitable choice, and the 2DEG characteristic is more close to the normally-on HFET with p-GaN cap layer than other thickness. However, the relatively low threshold voltage need to be concerned.

For further increasing the threshold voltage, the normally-off HFETs with insulator gate was fabricated. By inserting a SiN_x (thickness varied from 0 to 30 nm) layer between the p-GaN cap and the gate electrode, the threshold voltage positive shift from 1 to 8 V obviously. Besides, the introduction of SiN_x is also beneficial for suppressing the gate leakage current and improving the maximum gate voltage swing owing to the high breakdown field of approximately 8.3 MV/cm. The output current-voltage characteristics show that the device with thicker SiN_x needs a higher gate voltage to reach the same current density. This can be ascribed to that the applied gate voltage would partly appear across the SiN_x layer and partly across the semiconductor. The field-effect channel mobility measurement demonstrated that the SiN_x insulator shows no obvious effect on the 2DEG mobility.

For optimizing the normally-off MISHFETs, the normally-off MISFETs with self-aligned-gate (SAG) were adopted. And the SAG and the conventional gate (CG) were fabricated to confirm the feasibility of the SAG gate. The good ohmic contact of 1.45 Ω·mm contact resistance was obtained by the low-temperature ohmic technique. By employing the SiO_2 as the insulator layer, the V_{th} is close to 2 V in SAG device. Due to the difference of gate structure in SAG and CG device, the high channel resistance owing to the non-applied voltage region of p-GaN in CG device was discussed. It means that the SAG structure is the more advanced to achieve the good performance in normally-off MISFETs with p-GaN cap layer. Further, based on the low temperature ohmic process, a normally-off MISHFETs with SiN_x insulator layer and gate-first process was fabricated. Due to the 50 nm thickness, the gate swing and the output current density are enhanced

to 16 V and 47 mA/mm, respectively. And the Good pinch-off characteristics with threshold voltage of 2.0 V and a field-effect mobility of 1500 $cm^2V^{-1}s^{-1}$ were achieved. And the gate leakage current was remarkably suppressed. The low-temperature ohmic process also exhibits a capability of solution to alleviate the gate degradation during the high-temperature annealing in a gate-first process. Final, the interface state is analyzed, it indicates that the MISHFETs structure still has the issues that need to be optimized.

§6.2 Suggestion for future works

1. Further optimize the interface between p-GaN and insulator.

2. Find other suitable materials to further increase the threshold voltage and device performance.

Publications

Scientific Papers

1) **Taofei Pu**, Xiao Wang, Qian Huang, Tong Zhang, Xiaobo Li, Liuan Li & Jin-Ping Ao, “Normally-off AlGaN/GaN Heterojunction Metal-Insulator-Semiconductor Field-Effect Transistors with Gate-First Process,” ***IEEE Electron Device Letters***, vol. 40, no.2, Feb. 2019, pp. 185-188, doi:10.1109/LED.2018.2889291.
2) **Taofei Pu**, Qian Huang, Tong Zhang, Jiang Huang, Xiaomin Li, Liuan Li, Xiaobo Li, Lei Wang & Jin-Ping Ao, “Normally-off AlGaN/GaN Heterostructure Junction Field-Effect Transistors with Blocking Layers,” ***Superlattices and Microstructures***, vol. 120, Aug. 2018, pp. 448-453, doi.org/10.1016/j.spmi.2018.05.063.
3) **Taofei Pu**, Xiaobo Li, Xiao Wang, Yuyu Bu, Liuan Li, and Jin-Ping Ao, “GaN Schottky Barrier Diodes with TiN Electrode for Microwave Power Transmission,” ***Material Scientific Forum***, accepted, Jan. 2019.
4) Tong Zhang, **Taofei Pu**, Tian Xie, Liuan Li, Yuyu Bu, Xiao Wang, and Jin-Ping Ao, “Synthesis of thermally stable HfO_xN_y as gate dielectric for AlGaN/GaN heterostructure field-effect transistors,” ***Chinese Physics B***, vol. 27, no.7, Jun. 2018, pp.078503, doi:10.1088/1674-1056/27/7/078503.
5) Xiaobo Li, **Taofei Pu**, Taiki Hoshi, Tong Zhang, Tian Xie, Shigeki Joseph Luke Fujiwara, Hiroshi Kitahata, Liuan Li, Sachio Kobayashi, Motoo Ito, Xianjie Li, and Jin-Ping Ao, "GaN Schottky barrier diodes with nickel nitride anodes sputtered at different nitrogen partial pressure," ***Vacuum***, vol. 162, Apr. 2019, pp. 72-77, doi.org/10.1016/ j.vacuum. 2019.01.030.
6) Xiaobo Li, Taiki Hoshi, Liuan Li, **Taofei Pu**, Tong Zhang, Tian Xie, Xinjie Li, Jin-Ping Ao, “GaN Schottky barrier diode with thermally stable nickel nitride electrode deposited by reactive sputtering,” ***Materials Science in Semiconductor Processing,*** vol. 93, Apr. 2019, pp. 1-5, doi.org/10.1016/j.mssp.2018.12.018.
7) Liuan Li, Jia Chen, Xin Gu, Xiaobo Li, **Taofei Pu**, Jin-Ping Ao, “Temperature sensor using thermally stable TiN anode GaN Schottky barrier diode for high power device application,” ***Superlattices and Microstructures***, vol. 123, Nov. 2018, pp. 274-279, doi.org/10.1016/ j.spmi. 2018.09.007.
8) Tong Zhang, Lei Wang, Xiaobo Li, Yuyu Bu, **Taofei Pu**, Ruiling Wang, Liuan Li, Jin-Ping Ao, “Positive threshold voltage shift in AlGaN/GaN HEMTs with p-type NiO gate synthesized by magnetron reactive sputtering,” ***Applied Surface Science***, vol. 462, Dec. 2018, pp. 799-803, doi.org/10.1016 /j.a psusc.2018.08.135.

9) Liuan Li, Xiaobo Li, **Taofei Pu**, Yang Liu, and Jin-Ping Ao, “Normally-off AlGaN/GaN ion-sensitive field effect transistors realized by photoelectrochemical method for pH sensor application”, **Superlattices and Microstructures**, vol. 128, Apr. 2019, pp. 99-104, doi.org/10.1016/j.spmi.2019.01.018.

Conference Presentations

1) **Taofei Pu**, Tong Zhang, Lei Wang, and Jin-Ping Ao. Enhancement-Mode GaN-Based HEMT With a P-type GaN Cap Layer, ***2017 9th International Symposium on Advanced Plasma Science and its Application for Nitrides and Nanomaterials/10th International Conference on Plasma-Nano Technology & Science***, March 1~5, Nagoya, Japan.
2) **Taofei Pu**, Xiao Li, Xiao Wang, Yuyu Bu, Liuan Li, & Jin-Ping Ao, “GaN Schottky barrier diodes for microwave power transmission,” ***2018 IEEE MTT-S International Wireless Symposium (IWS)***. IEEE, 2018.
3) Xiaobo Li, **Taofei Pu**, Taiki Hoshi, Tian Xie, Liuan Li, Xianjie Li, Shigeki Joseph Luke Fujiwara, Hiroshi Kitahata, and Jin-Ping Ao Nickel Nitride Gate AlGaN/GaN HFETs with Low Gate Leakage Current, ***The 2018 International Workshop on Nitride Semiconductors (IWN 2018)***, kanazawa, Nov. 2018.
4) Li Xiaobo, Zhang Tong, **Pu Taofei**, Hoshi Taiki, Xie Tian, Li Xianjie and Jin-Ping Ao, GaN Schottky Barrier Diode with Nickel Nitride Electrode, ***The 2018 Asia-Pacific Conference on Silicon Carbide and Related Materials (APCSCRM2018)***, Beijing, Jul. 2018.

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2) Wide energy bandgap electronic devices[M]. World Scientific, 2003.
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