Graphene stacked junction diode for terahertz emission

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Abstract

Graphene is one of the most prosperous materials for the diode in terahertz emission, the properties of graphene in terahertz technology promise in enabling novel technologies for the convergence of electronics and photonics. Owing to the recent development of heterostructure fabrication technology using materials composed of two-dimensional atomic crystals, creation of new functional devices consisting of graphene tunnel diodes has become possible.

In this thesis, sandwiched stacked graphene junction diode structure composed of graphene/ structured water/ graphene was fabricated using direct bonding technology. The epitaxial graphene samples were prepared on a 4H-SiC (0001) semi-insulative substrate with dimensions of 10 mm × 10 mm using an infrared rapid thermal annealer (SR-1800). The Hall effect, Raman and Scanning probe microscope (SPM) measurement are used for graphene samples to know graphene surface condition. The water layer structure is fabrication though treated in DI water for 15 min that to cover it with an atomically thin structured water layer as a barrier. We successful got 4 stacked graphene junction diodes both the Fowler–Nordheim (FN) phenomena and Direct tunneling (DT) phenomena are observed. We demonstrated and analyze graphene/ structured water/ graphene junction diode though Current-Voltage (*I-V*) characteristics and Fowler–Nordheim tunneling(FNT) tunneling model for parameters calculation. Based on FN-plot junction diode data analysis, the thickness of the water layer barrier of graphene junction diode is obtained less than 1nm. This very thin barrier provides possible for high current and large power graphene junction diode.

Keyword

Graphene, Semiconductor devices, Junction diode, Tunnel junction.

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1. Introduction

1.1 Graphene introduction

Graphene is a two-dimensional material formed by carbon atoms [1-2]. In 2004, graphene is first been produced by Andre Geim et al. at the University of Manchester [3]. Graphene is a zero bandgap semiconductor, in which the electrons act like massless Dirac fermions and have high mobility (100.000 $cm^2/V \cdot S$). Besides, the Fermi energy level is changed in Graphene by applying the electric field, that lead change of hence the electron and hole concentration [4~6]. Accordingly, this material can play a functional role in the electronic and optoelectronic devices [7~9].

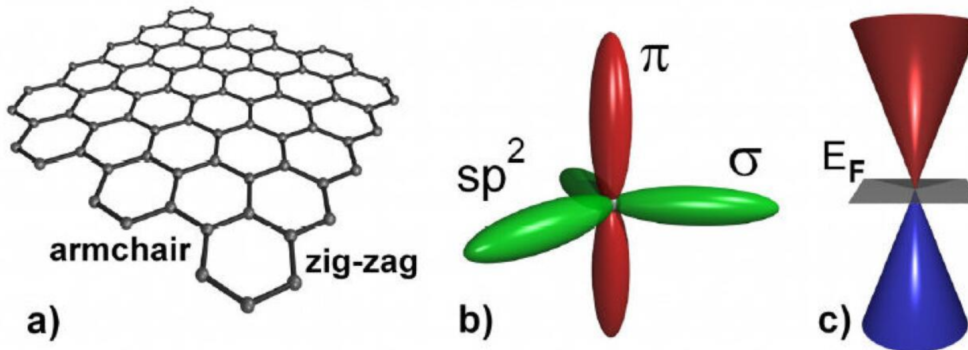

Fig. 1 (a) Schematic of a graphene crystallite with characteristic armchair and zig-zag edges. (b) Schematic of electron σ− and π−orbitals of one carbon atom in graphene [10]. c) Band diagram of graphene at k = 0.

Graphene is a two-dimensional (2D) material consist of sp^2 hybridized carbon atoms arranged in a 2-dimensional honeycomb crystal lattice with a bond length of 1.42 Å. The carbon atom has four valence electrons, three of these electrons participating in σ-bonding with its closest neighbors created honeycomb structure [11]. In Fig. 1, fourth valence

electrons occupy an orbital perpendicular to the one-dimensional (1D) sheet creating delocalized π-bonding, which could create a two-dimensional electron gas (2DEG) with high mobility [10,12].

Due to the carbon active chemical principles, carbon has abundant allotropes such as three-dimensional carbon structure graphite and diamond are the first carbon to be discovered and widely Applied to human life [13,14]. Graphene also is considered as a basic building block for 0D fullerenes, rolled into 1D nanotubes or stacked into 3D graphite in Fig. 2. The observation of graphene can be traced back to the 1960s. In 1986, this single layers of graphite first been named graphene by Boehm et al [15]. However, this material has once been considered not exist because strictly 2D crystals were thermodynamically unstable [16,17]. Until 2004, Novoselov. K. S. et al. made single-layer graphene first been exfoliated by mechanical exfoliation, it became one of the most exciting research materials [18].

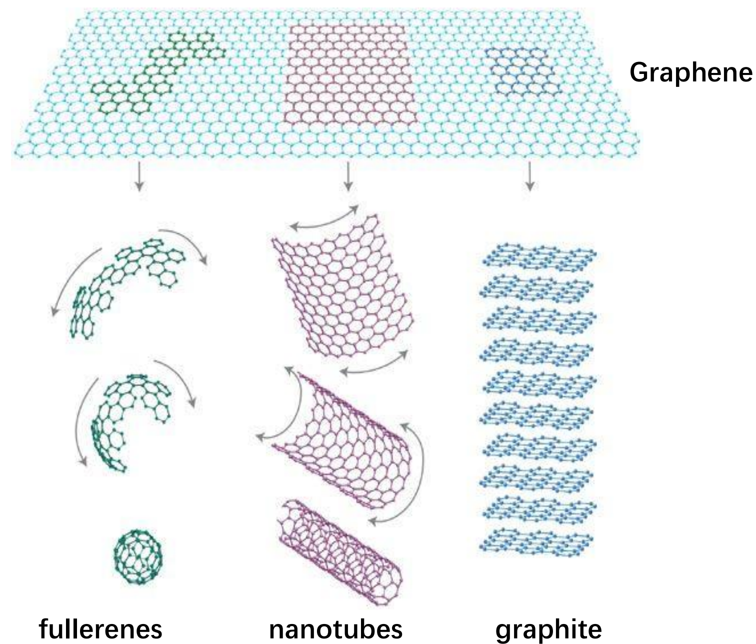

Fig. 2 Graphene is a 2D building material for carbon materials of all other dimensionalities. It can be wrapped up into 0D buckyballs, rolled into 1D nanotubes or stacked into 3D graphite [15].

1.2 Graphene principles and measurement

1.2.1 Graphene properties

The excellent abilities of graphene-based on graphene unique band structure characteristics, the zero bandgaps of graphene make it be the highest characteristic mobility material that is known could exist at room temperature.

Graphene single layer sheet carbon atom structure make it become the thinnest material known in the world. It's also the strongest material, a single flake will exhibit a large breaking strength of ≈40 N/m due to the absence of slip planes associating the fracture strength of graphene with the strong bonding of c–c in a hex ring [19]. Graphene is also very pliable with a Young's modulus ≈1.0 TPa and an elastic strain of up to 20% [19], the theoretical specific surface area can reach to 2630m^2/g [20], high thermal conductivity of ≈5000 W/mK [21] and its optical transmittance is about 97.7% [22].

1. **Zero Bandgap**

Graphene as a zero bandgap semimetal, the valence and conduction bands are cone-shaped and meet at the K points of the Brillouin zone in Fig.3. The zero bandgaps of graphene lead large-area graphene channels devices cannot be switched off which not suitable for logic applications. However, the scientist tries to modified graphene band structure. There are three ways for open bandgap: by constraining graphene in one dimension to form graphene nanoribbons, by biasing bilayer graphene and by applying strain to graphene.

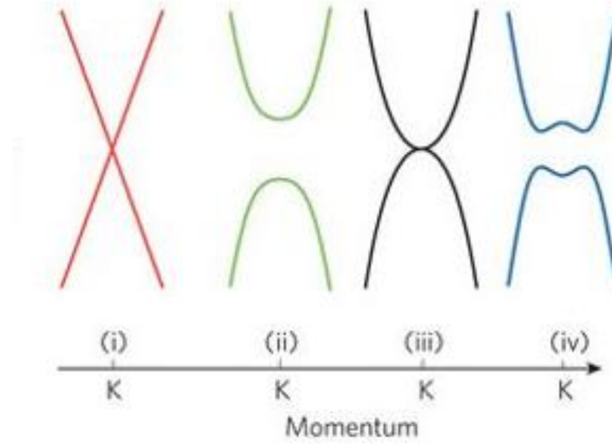

Fig. 3 Band structure around the K point of (i) large-area graphene, (ii) graphene nanoribbons, (iii) unbiased bilayer graphene, and (iv) bilayer graphene with an applied perpendicular field. Large-area graphene and unbiased bilayer graphene do not have a bandgap, which makes them less useful for digital electronics [23].

2. High Mobility

The high mobility of graphene occurs due to electron delocalization and weak electron-phonon interaction, that making graphene became an ideal material for electrical applications requiring high mobility and fast response times.

The high carrier mobility of graphene at room temperature is about 10,000-15,000 cm^2/Vs are routinely measured for exfoliated graphene on SiO_2 covered silicon wafers [24,25], and upper limits have been suggested between 40,000 to 70,000 cm^2 /Vs [25,26]. The mobility is 200,000 cm^2/Vs at a carrier density of 10^{12} cm^{-2}, 10×10^6 times greater than copper [27,28]. For large-area graphene grown on nickel and transferred to a substrate, mobility greater than 3,700 cm^2/Vs has been measured.

For epitaxial graphene on silicon carbide, the mobility depends on graphene grown on SiC substrate silicon face or carbon face. Although graphene grown on the carbon face has higher mobility (values of ~5,000 cm^2/Vs [29], compared with ~1,000 cm^2/Vs

graphene grown on silicon face [29,30]), but single layer and bilayer graphene could easier get on silicon face, which makes the silicon face graphene growth more suitable for electronic applications.

3. Optical transition

The optical properties of graphene become unique on account of the linear band structure, zero band-gap and strong interaction of Dirac Fermions with electromagnetic radiation. Graphene absorbs over a wide spectral range, and this is contributed from interband and intraband optical transitions. The absorption of graphene from visible to near-infrared region is modeled by interband transitions and it is frequency independent, described by fine structure constant [31,32]. The optical response in the far-infrared region is due to the intraband transitions or free carrier absorption [33]. Direct photon absorption is not possible by intraband transition due to the momentum mismatch. To conserve momentum, phonon scattering occurs, followed by a population inversion of free carriers near the K-point. The conductivity from free carrier absorption shows a Drude like frequency dependence [34]. The far infrared response can be tuned to terahertz range by plasmonic excitations of charge carriers [35]. Plasmon assisted light absorption is not allowed in graphene because of the large momentum mismatch between the photons and plasmons [36]. However, plasmon excitations can be activated by electrostatic gate coupling and engineering graphene nanostructures [37].

1.2.2 Four-point probes measurement method

Four-point probes measurement is an electrical impedance measuring technique that uses separate pairs of current-carrying and voltage-sensing electrodes to make more accurate measurements than the simpler and more usual two-point probe measurement. Four-point probe measurement is used in some ohmmeters and impedance analyzers, and in wiring for strain gauges and resistance thermometers. Four-point probes are also used to measure sheet resistance of thin films (particularly semiconductor thin films) [38].

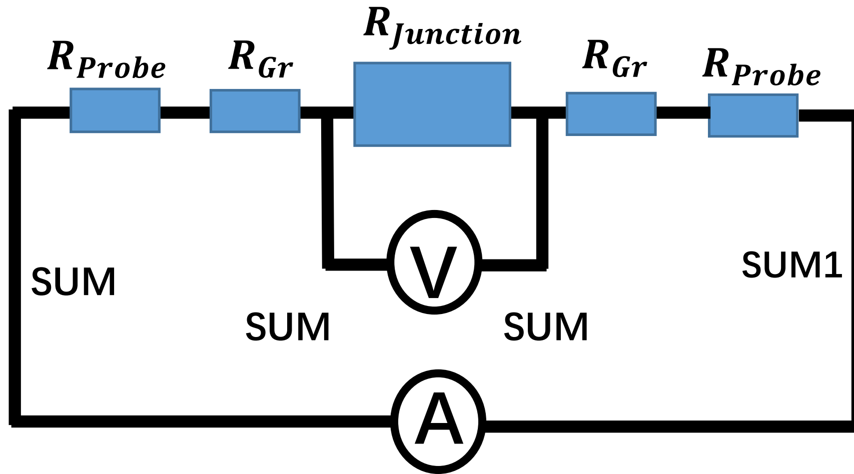

Fig.4 Four-point probe measurement schematic diagram of stacker graphene junction diode.

When four-point probe measurement is used, the current is supplied via a pair of force connections (current leads). These generate a voltage drop across the impedance to be measured according to Ohm's law V=IR. A pair of sense connections (voltage leads) are made immediately adjacent to the target impedance so that they do not include the voltage drop in the force leads or contacts. Since almost no current flows to the measuring instrument, the voltage drop in the sense leads is negligible.

It is usual to arrange the sense wires as the inside pair, while the force wires are the outside pair. If the force and sense connections are exchanged, accuracy can be affected, because more of the lead resistance is included in the measurement. The force wires may have to carry a large current when measuring very small resistances, and must be of adequate gauge; the sense wires can be of a small gauge. It is common to provide 4-wire connections to current-sensing shunt resistors of low resistance operating at high current.

In this thesis, *I-V* characteristic is a measurement though Agilent 4156C, which shows the circuit diagram in Fig.4. Four-point measurement of resistance between voltage sense connections 3 and 4. Current is supplied via force connections 1 and 2. The difference voltage between SUM3 and SUM 4 is the electric potential difference for stacked graphene junction.

Fig.5 Photograph of *I-V* measurement instrument of Agilent 4156C.

1.2 Growth of epitaxial graphene

Since 2004, single-layer graphene been obtained through exfoliation [3], a rapidly increasing list of production techniques has been developed to enable graphene's use in commercial applications. Graphene can be produced in a variety of ways, such as exfoliation, epitaxial, nanotube slicing and carbon dioxide reduction. Among these methods, epitaxy graphene has the advantages of films can be grown on various crystalline surfaces, atomic lattice of the substrate facilitates in orientationally registering the carbon atoms of the graphene layer, chemical interaction of the graphene with the substrate can vary from weak to strong. In epitaxy graphene method, thermal decomposition of silicon carbide and chemical vapor deposition (CVD) graphene produce are the most common graphene produce method today. In this part, thermal decomposition of silicon carbide and chemical vapor deposition (CVD) graphene method will be introduced in detail.

1.2.1 Thermal decomposition of silicon carbide

A silicon carbide crystal is composed of Si and C alternatingly bonded in tetrahedral

coordination in Fig.14. The realization of the potential of SiC for electronics can be dated back to the discovery of electroluminescence in 1907 by using SiC [39], which can be seen as an early version of a light emitting diode (LED). For application in electronics, the reliable production of high quality SiC crystals is necessary. Important milestones were the Lely growth process of SiC crystals in 1955[40], the seeded sublimation growth by Tairov and Tsvetkov in 1978 [41], the possibility to grow single crystal SiC on Si substrates invented by Matsunami et al. in 1981[42]. For today, the size of commercially SiC wafers is 4 inch (100mm) in diameter and 6-inch (150mm) wafers will be done soon.

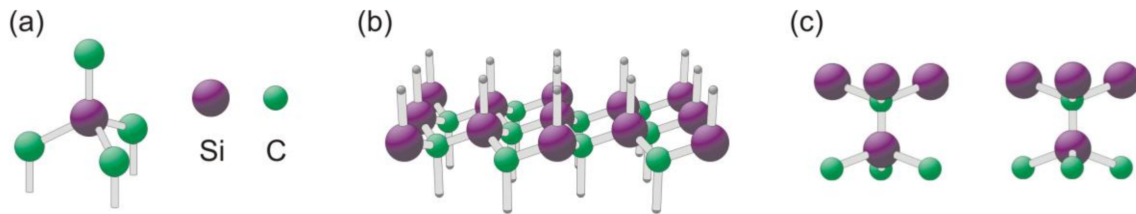

Fig.6 (a) Si-C tetrahedron with sp3-hybridized silicon and carbon atoms, (b) hexagonal SiC bilayer as the basic building block of the SiC crystal structure, (c) Si-C tetrahedra bonded in identical orientation (left image) and rotated by 60◦ with respect to each other (right image) leading to cubic (zinc blende) and hexagonal (wurtzite) SiC crystal structures. The images are adapted from Ref [43].

In tetrahedral structure, each Si atom is bonded with four C atoms in SiC in Fig.14 (a). In SiC the bond length between the Si-Si bond length (2.35 Å) and the C-C bond length (1.54 Å) which amounts to 1.89 Å. The covalent bonds have an ionic contribution of 12% because of the higher electronegativity of C. In Fig.6, a layer of planar hexagonal symmetry is formed by linking the tetrahedra together and each element is exclusively positioned in either the upper or the lower sublayer. The interlayer distance is 1.89 Å which equals the SiC bond distance.

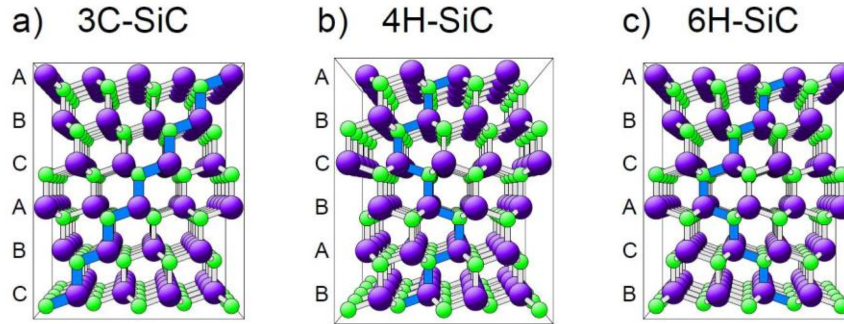

Fig. 7. Crystal structure of different SiC polytypes displayed parallel to the $(11\bar{2}0)$ plane: (a) zinc blende structure (cubic 3C-SiC), (b) hexagonal 4H-SiC and (c) hexagonal 6H-SiC.

The cubic zinc blende SiC crystal structure in Fig.7 gives the most common polytypes for introduction. Fig.7(a) is characterized by an identical orientation of all bilayers in the crystal. Figs.7(b) and 2(c) is the crystal structure for a 4H polytype consisting of slabs of two and a 6H polytype consisting of slabs of three identically oriented bilayers, respectively.

Silicon carbide (SiC) is a highly resistive material, with the advantages of not shunt the current flow in graphene and already available in the form of large-diameter wafers lead it to be one of the most likely avenues to graphene-based electronics. The graphitization of SiC by Si sublimation during high-temperature vacuum annealing was demonstrated as early as the 1960s [44] and has recently been refined [45].

Thermal decomposition of silicon carbide

Although the surface of the SiC substrate for graphene growth has well-defined orientation and lattice fits well but vacuum graphitization ordered substrate surface into a rough(Fig.8(c)), highly corrugated landscape (Fig. 8(d)). This disorder not only hinders further processing but also limits device performance by scattering carriers flowing in the active graphene layer.

For graphene fabrication, if a system cannot be brought to its most favourable morphology because the necessary microscopic processes the detachment, diffusion and reattachment of surface atoms are suppressed. An 80-year-old technology had revived by Emtsev and others, this technology was originally developed to extend the life of

incandescent filaments[46]. When silicon carbide (SiC) suffer high temperatures (>1100 °C) under low pressures reduces it to graphene in Fig.8(a). Fig.8 shows the surface during graphitization of Si-face SiC. Not like normal fabrication in vacuum, sample laced in an unreactive argon atmosphere at nearly ambient pressure._The dense cloud of gas molecules hinders the transport of Si atoms away from the SiC surface, reducing the overall sublimation rate and allowing an increase in graphitization temperature by several hundred degrees. Though this process for samples growth, the large smooth surfaces obtained, the length of flat substrate terraces that reach tens of micrometers and several micrometers in width, and are separated by steps (Fig. 8(d)). The carbon layer grown on this surface now consists primarily of monolayer graphene, with narrow bilayer (and occasional trilayer) stripes at the terrace edges.

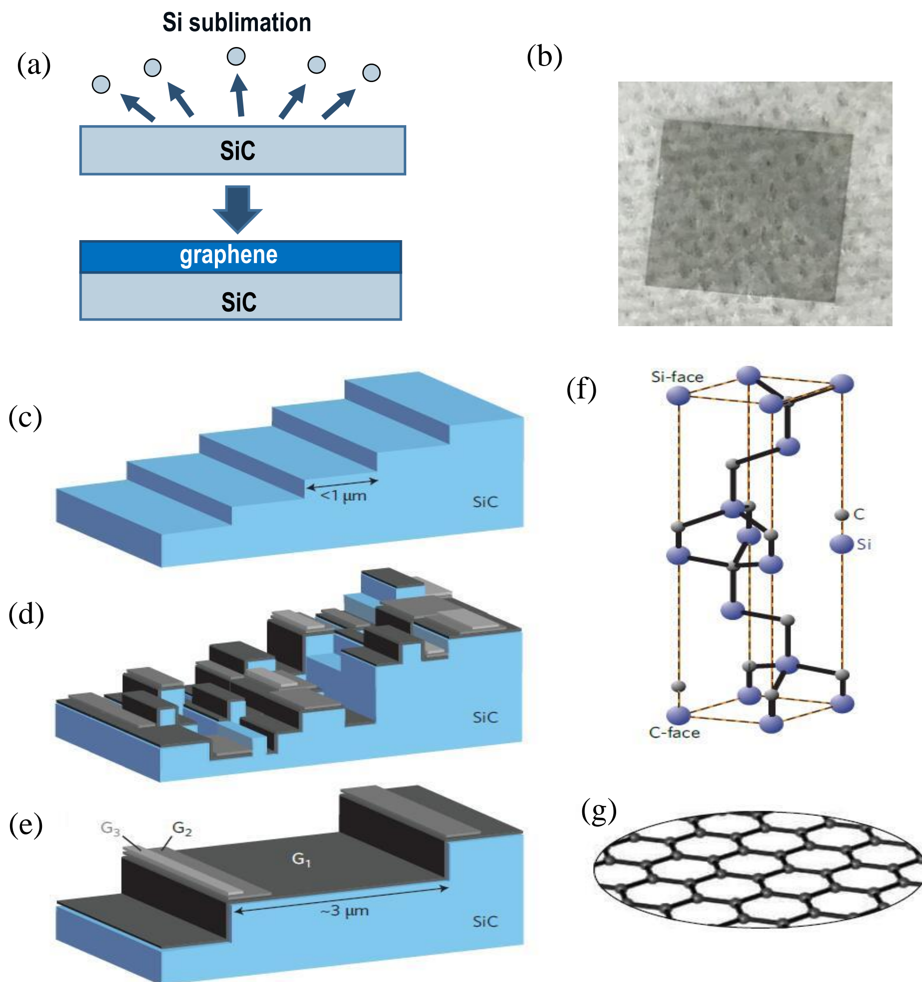

Fig. 8 (a) Pyrolysis of SiC for epitaxial graphene. (b) Sample photograph of Graphene with SiC substrate (c) SiC starting surface with a staircase of flat terraces and atomic steps. (d), Unit cell of 6H-SiC. (e), Schematic morphology of vacuum-graphitized SiC. (f), Morphology obtained in high-pressure argon. The surface termination is predominantly monolayer graphene, G1 (g), with narrow stripes of bilayer (G2) and trilayer (G3) graphene near the upper edge of the substrate steps [47].

In 2008, C. Virojanadara et.al reported the graphene layer condition which fabrication by thermal decomposition on SiC(001) substrate. The measurement of SiC (001) is by ARPES, LEED, and LEEM [48,49].

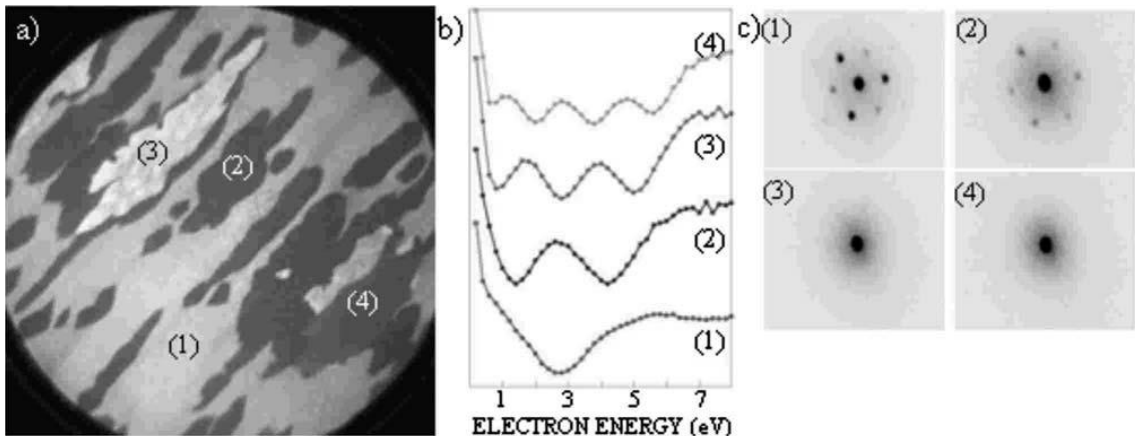

Fig.9 (a) LEEM image from a second sample grown ex-situ on which thicker graphene layers were grown. (b) Electron reflectivity spectra extracted from the four representative areas (1) - (4) corresponding to graphene of 1–4 ML thick, respectively. (c)Micro-LEED collected at E=53.3 eV from the four different areas [49]

The graphene by thermal decomposition of silicon carbide could get single-layer graphene, two layers graphene and $6\sqrt{3}$. In the same year, K. V. Emtsev et.al through the experiment of angle-resolved valence band photoelectron spectroscopy, soft x-ray induced core-level spectroscopy, and low-energy electron diffraction. Thermally induced growth of graphene on the two polar surfaces of 6H-SiC is investigated with emphasis on the initial stages of growth and interface structure [50].

In this thesis, graphene samples were produced by the decomposition of 4H-SiC, Fig.10 shows the graphene step structure of 4H-SiC decomposition.

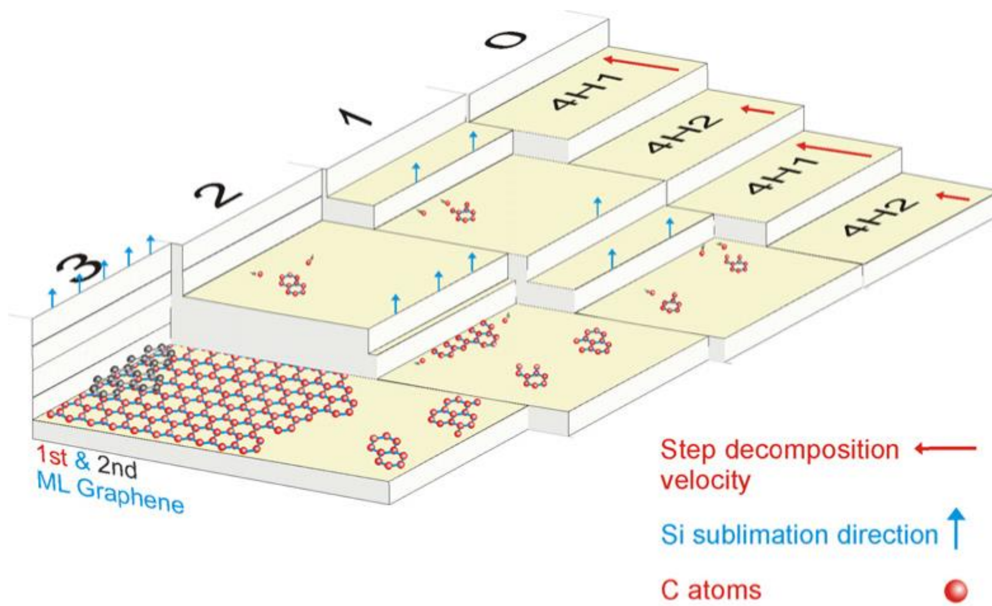

Fig.10 Schematic depiction of the formation process of epitaxial graphene via sublimation of Si from the SiC surface. On 4H-SiC, stage 0-steps with one Si–C bilayer height and different terrace decomposition energies (red arrows). Stage 1-sublimation of Si atoms from the edge of steps and an ML graphene formation. Stage 2-merging two Si–C bilayers and extending the graphene layer along the step edge (red hexagonal network). Stage 3-source of C atoms increasing after four Si–C bilayer bunching, and a second graphene layer formed on the first ML (black hexagonal network).

Fig.11 is the surface topography of graphene by thermal decomposition of SiC, (a) 13 × 13 graphene lattice lies above the 6R3 reconstructed SiC surface. The small and large black circles represent R3 and 6R3 lattices, respectively. The green, yellow, and gray spheres represent C of graphene and Si and C in SiC, respectively. The large black circles represent the 6R3 lattice. The bulk lattice constant we used for SiC is 3.073 Å [51], while that for graphene is 2.456 Å [52]. It is obvious that the 13x13 graphene (31.923 Å) matches the 6R3 lattice(31.935 Å) quite well. On the other hand, the 2x2 graphene (4.9 Å) does not match the R3 structure (5.34 Å) (small black circles).

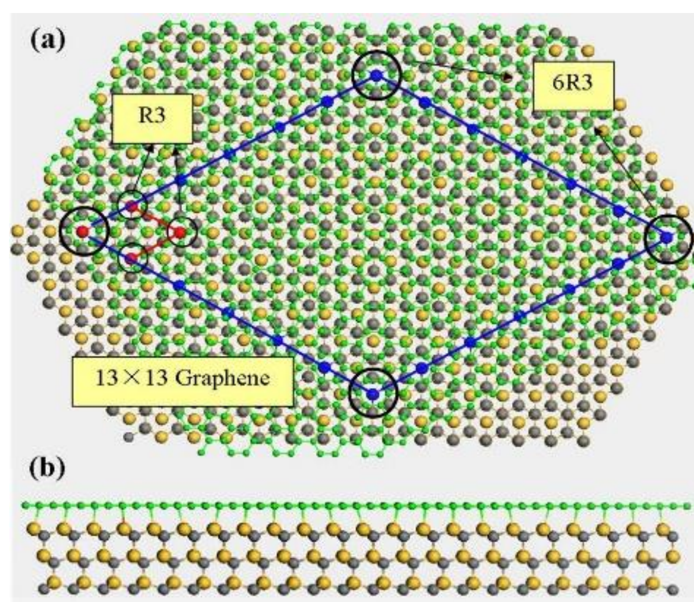

Fig. 11 Schematic (a) top view and (b) side view of a graphene layer on SiC (0001) surface. The green, yellow, and gray spheres represent C in graphene, Si in SiC, and C in SiC, respectively. The SiC surface was after 6R3 reconstruction and a 13x13 graphene lattice lies on above it. The small black circles represent the R3 lattice, while the large black circles represent the 6R3 lattice. The top and side views schematic diagram of graphene on the SiC (0001) surface[53].

The equipment for thermal decomposition of SiC

Consider about the SiC thermal decomposition method require the temperature highly than 1200 ° C for Si atom detached from the SiC substrate, and uniform graphene layer in need an inert gas atmosphere for heating, these led the temperature need higher than 1600 ° C. And graphene could be obtained in a narrow temperature band, the time for form atom layer is very short, that made a temperature rise fast and temperature control equipment is needed. For our group, an infrared heating device RTA SR1800 (Rapid Thermal Annealing) is used for the experiment. Based on near-infrared illumination could generate heat, using reflection realize sample heater.

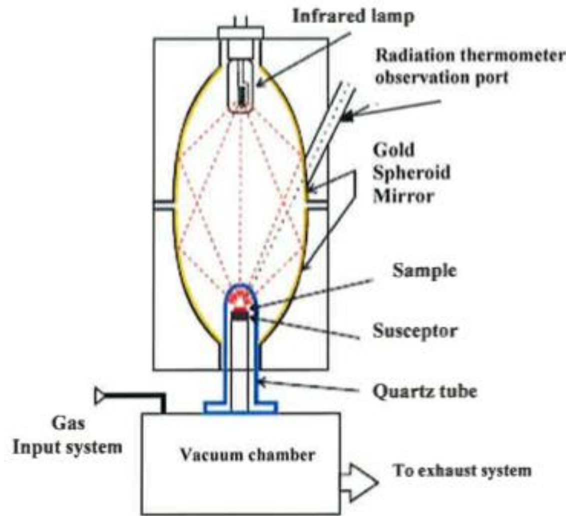

Fig.12 Infrared focus heating system schematic.

In this thesis, our graphene samples were fabricated by thermal decomposition of SiC. The face of the SiC used for graphene formation, silicon- or carbon-terminated, highly influences the thickness, mobility and carrier density. For our graphene samples, we adopt heating SiC for epitaxial graphene. The graphene samples were prepared using an infrared rapid thermal annealer (Thermo Riko SR-1800) in Fig. 13. The starting material was 4H-SiC (0001) semi-insulating substrate of size 10 mm × 10 mm, cut using the stealth-dicing technology. The substrate was subjected to thermal decomposition at 1640°C ~1660 °C in Ar environment (100 Torr) for five minutes, for the epitaxial graphene growth of samples.

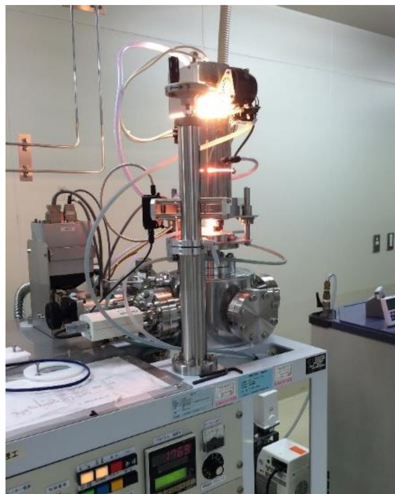

Fig. 13 The photograph of Thermo Riko SR-1800 for graphene-graphene samples growth.

1.2.2 Synthesis of graphene by chemical vapor deposition (CVD) method

The graphene preparation always from mechanical exfoliation of graphite [3], chemical vapor deposition (CVD), epitaxial growth on SiC surfaces [54-55,30] and reduction of graphene oxide [56-57]. CVD has the advantages of inexpensive, transferrable and it has the ability to produce high quality and large-area graphene films [58,59]. Typical CVD graphene growth uses gaseous hydrocarbons at elevated temperatures as the carbon source, such as methane, ethylene (at 1000°C) [60~64] and acetylene (at 650°C) [65]. Graphene been prepared of CVD first reported in 2008 and 2009 with Ni and Cu substrates [66,67].

For preparing large-area, high-quality monolayer graphene uses copper as catalyst substrate is a popular method [58]. Because of solubility of C atoms in Cu adsorption process on Cu surface is low that offering a way of growing monolayer graphene [67-68].

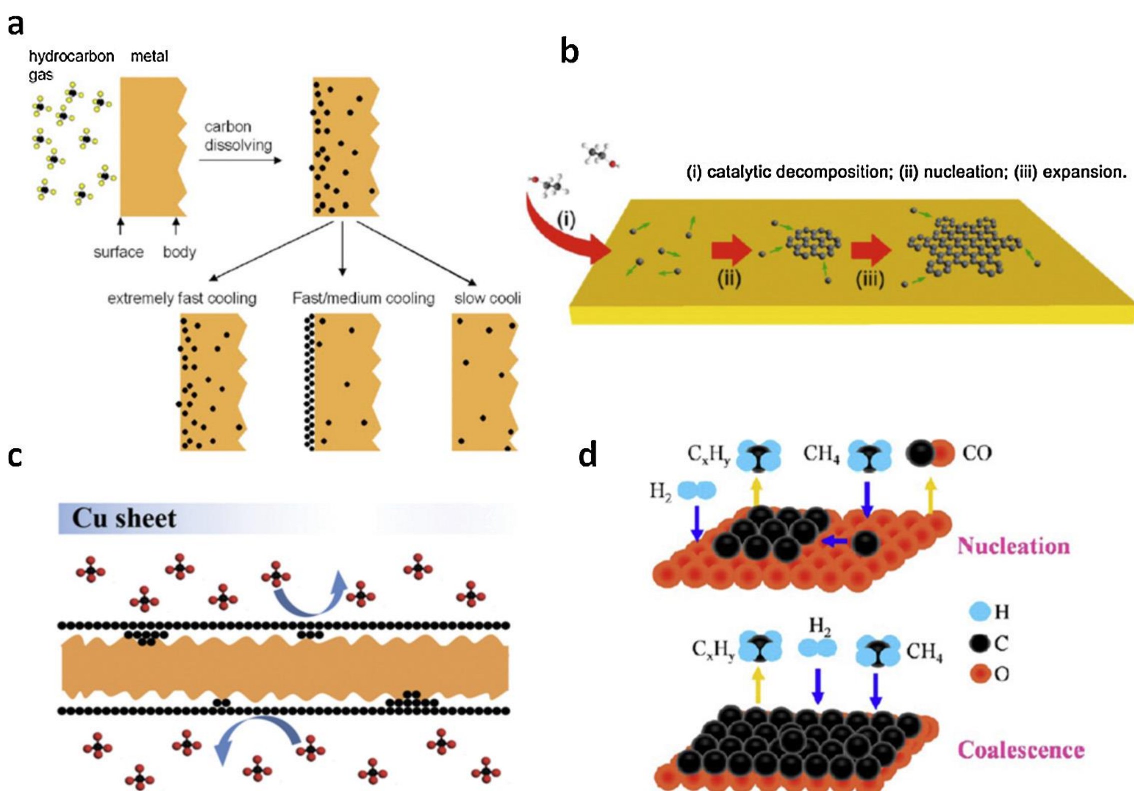

Fig. 14. Schematics of CVD graphene grown on (a) Illustration of carbon segregation at metal surface. (b) Cu foil, (c) Cu enclosure, and (d) sapphire. Adapted with permission from Ref [66] [69-

71].

In 2008, an approach to synthesizing high-quality graphene by surface segregation and substrate transfer is reported. Synthesized several layers of graphene on Ni substrates by a surface segregation process with controlled cooling and transferred them to glass substrates by wet etching. Electron microscopy and Raman spectroscopy measurement show that the graphene films synthesized with medium cooling rates have high quality crystalline structure and well-controlled thicknesses [66].

In 2009, a growth large-area graphene films of the order of centimeters on copper substrates by chemical vapor deposition using methane is first reported. Most of the single-layer graphene, only a small percentage (less than 5%) area having few layers, and are continuous across copper surface steps and grain boundaries. The dual-gated field-effect transistors fabricated on silicon/silicon dioxide substrates showed electron mobilities as high as 4050 square centimeters per volt per second at room temperature [67].

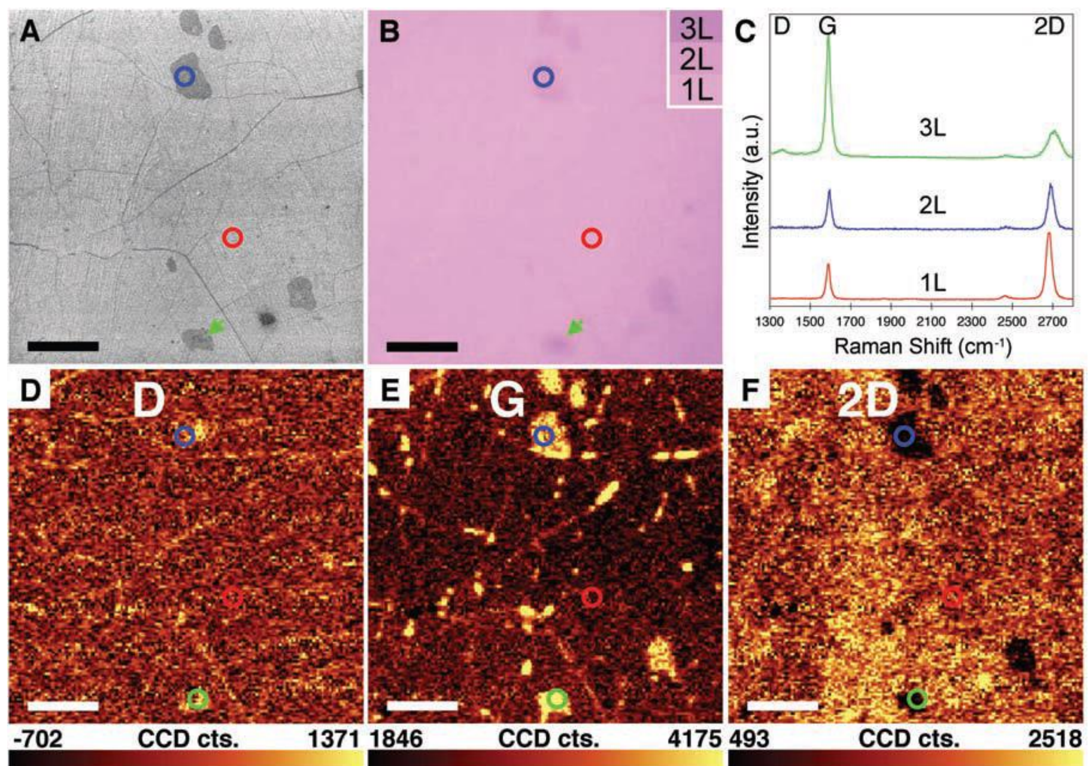

Fig. 15. (A) SEM image of graphene transferred on SiO_2/Si (285nm thick oxide layer) showing

wrinkles, as well as two-and three-layer regions. (B)Optical microscope image of the same regions as in (A). (C) Raman spectra from the marked spots with corresponding colored circles or arrows showing the presence of one, two, and three layers of graphene. (D to F) Raman maps of the D (1300 to 1400 cm^{-1}), G (1560 to 1620cm^{-1}), and 2D (2660 to 2700 cm^{-1}) bands, respectively [67].

1.3 Graphene characterization technology

Graphene is a material of atomic thickness which was popular for electronic device fabrication. For this reason, the characteristic measurement of the graphene sample for further fabrication is necessary, for example, Atomic and Electrostatic Force Microscopy and Raman spectroscopy. In the following, few most common characterization techniques for graphene layers are introduced briefly [72].

1.3.1 Hall effect measurement of graphene samples

Hall effect measurement is wildly used in the electronics industry for basic materials and device research. For example, Hall effect been sued for graphene carrier mobility measurement in Fig.10 and sample type determining [73]. By forcing both a magnetic field perpendicular to the sample and a current through the sample, that Hall voltage (V_H) been measured. In order to get mobility, transverse current been obtained though combination of the current flow (I) and the magnetic field (B), resulting potential (V_H) is measured across the device, both the sample thickness (t) and its resistivity (ρ) are also required for accurate measurements. By using four-point probe, the resistivity can be determined calculated though formula with these five parameters (B, I, V_H, t, and resistivity).

$$\mu H = \frac{|V_H t|}{BI\rho} \quad (1)$$

Because Hall voltages are typically quite small (millivolts or less), as is the measured van der Pauw resistivity, the right measurement and averaging techniques are critical to obtaining accurate mobility results when using this formula.

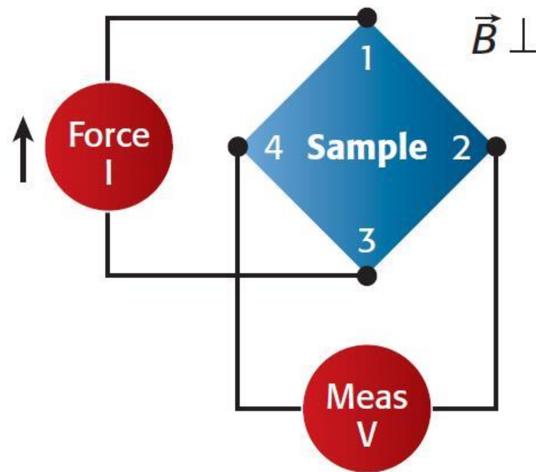

Fig.16 Measuring principle of Hall effect voltage [73].

1.3.2 Raman spectroscopy measurement of graphene samples

The first time for Raman scattering observed is in 1928, by C.V. Raman [74-75], and Raman spectroscopy measurement applicate for materials is in the 1940s. An incident laser beam is shine to de material, according to the different peak of spectrum that reflect from materials, the information about the photon properties of the crystal or the vibrational properties of the molecule will be obtained [72].

1. Raman spectroscopy technology

Raman scattering is based on the analysis of light matter interaction [76], that is, absorption, emission, or scattering of a photon. There are two explains of this phenomenon. For the classical interpretation, radiation is considered as an electromagnetic wave and the matter as an assembly of independent classical rotors and vibrators. From a macroscopic point of view, light scattering consists of a deviation of light from its straight trajectory (original direction of incident light). Molecules scatter light because the electric field of the incident light wave forces the electrons within the molecule to oscillate (see Fig.17), producing oscillating electric moments leading to the reemission of radiation in all directions [77].

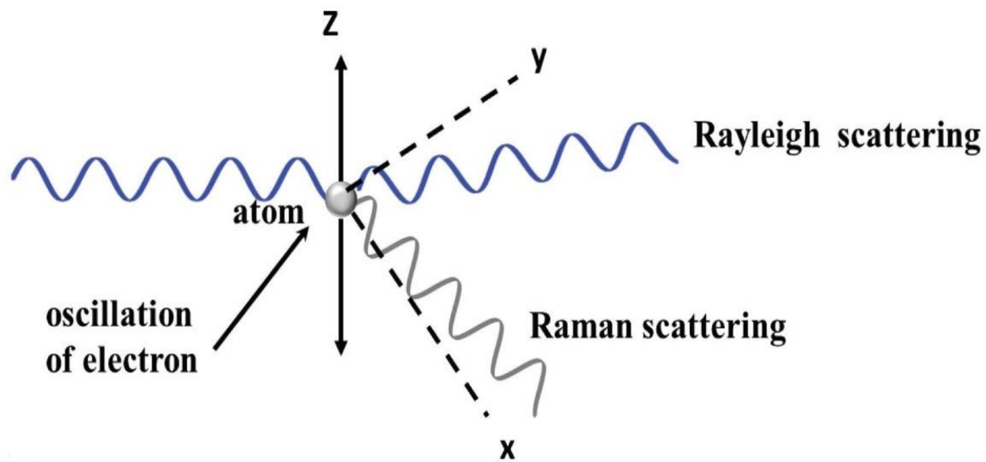

Fig. 17. Light scattering produced by the interaction of the incident light's electric field and the molecule electrons.

2. Dispersive Raman spectrometer

For Raman spectrometer, reflector and the optical lens are one of the most important components which cannot be substituted. The Raman components included Excitation source, Sample illumination systems, and collection optics, Wavelength selectors and separators, Detector and Recording device.

A microscope is integrated into a conventional Raman spectrometer, enabling both visual and spectroscopic measurements in Fig. 18. For different types of Raman equipment, the focusing and collection optics of the scattered radiation are identical. Except for analysis of a single point, these spectrometers allow mapping and imaging measurements.

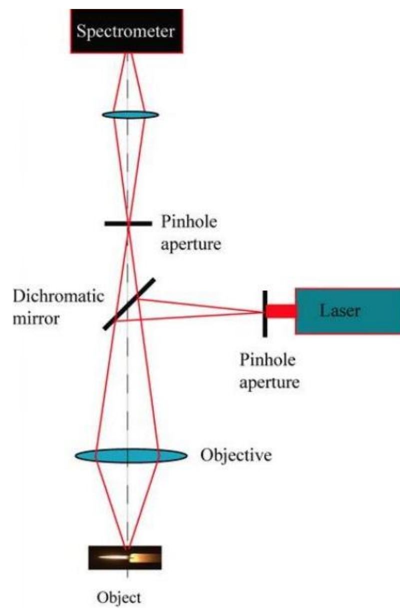

Fig.18. Descriptive scheme of the main components of a Raman micro-spectrometer [78].

Raman spectroscopy has the advantages of fast, nondestructive, and high-resolution for material characterization of graphene materials. Epitaxial graphene on SiC substrate has interacted with the SiC, which may have an effect on its electronic properties. Due to the interaction of epitaxial graphene with the SiC substrate, a bandgap of ~0.26 eV was observed by angle-resolved photoemission spectroscopy.

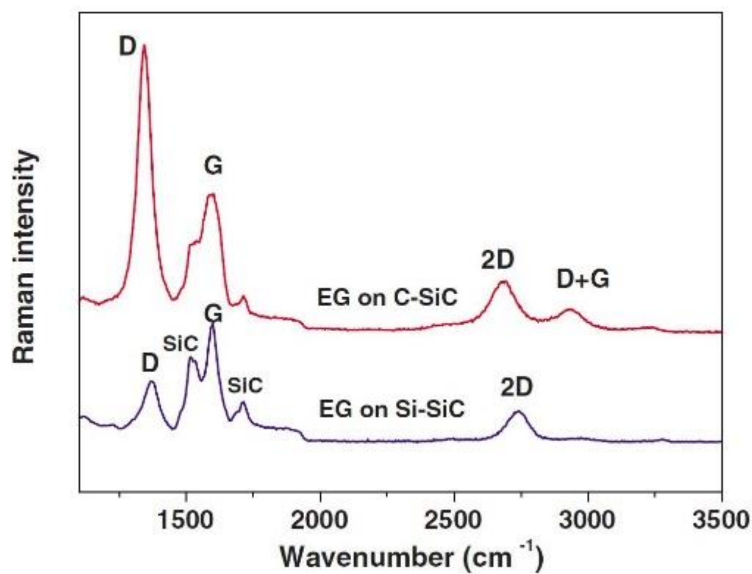

Fig. 19. Raman spectra of EG grown on Si-terminated SiC (Si-SiC) and C-terminated SiC (C-SiC) [79].

For graphene measurement, it could provide information of stacked graphene layer, the atomic structure of graphene edges, disorder and defects and stacking order between different layers. Raman spectroscopy result response though curve peak, Fig.19 is the introduce of intrinsic Raman spectrum(IRS) of epitaxial graphene on SiC substrate. Graphene has three main features in its Raman spectrum, called the D, G, and 2D (also called G') modes. As shown in Fig. 19, they appear at about 1350, 1583 and 2700 cm [72].

In this thesis, a Raman spectrometer(u-Raman) is been used for graphene condition measurement in Fig.20.

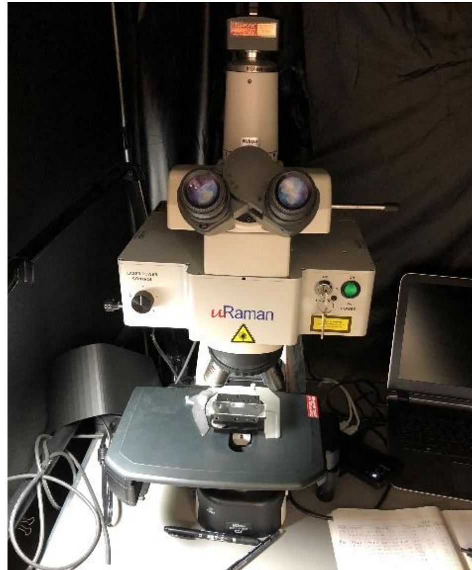

Fig. 20 Raman spectrometer for graphene measurement.

1.3.3 Scanning probe microscope (SPM) measurement for graphene samples

Scanning probe microscope (SPM) is a microscopy branch of surfaces forms images use physical probe scans the specimen. SPM provides a straight forward identification of graphene domains with various thicknesses on the substrate where topographical determination is hindered by adsorbates and SiC terraces. Dynamic Force Microscopy (DFM) is a common measurement in SPM, the cantilever is oscillating while it approaches the sample surface. The force between probe and sample is reflected by

cantilever amplitude change and maintained to be constant while scanning and observing the sample surface.

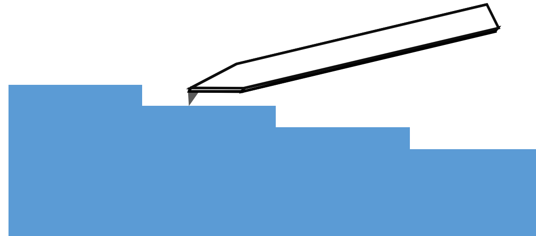

Fig. 21 Schematic diagram of scanning graphene surface by SPM.

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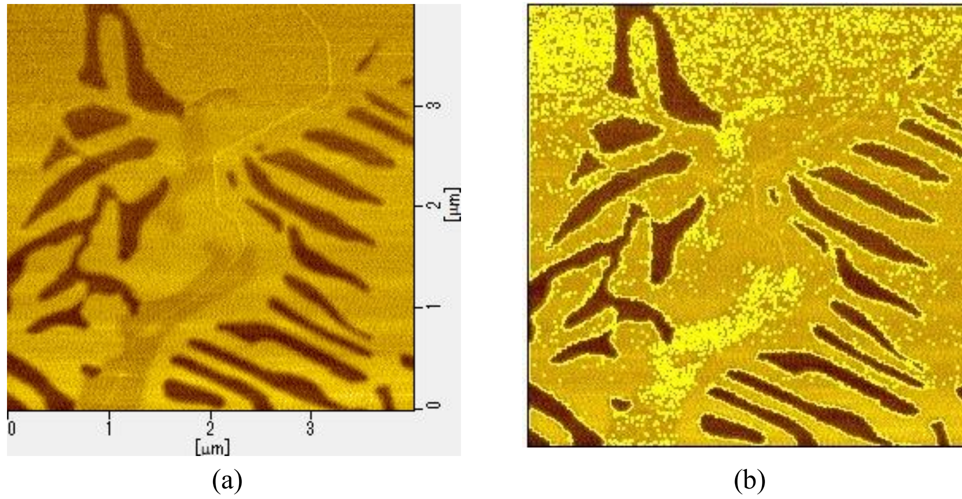
Fig.22 The photograph of SPA400/Nanonavi SII-NT for graphene samples measurement

Graphene stacked on SiC substrate surface after epitaxial growth that leads graphene surface roughness. Graphene surface will leave empty hole after DI water treated cause the roughness surface of graphene by thermal decomposition of silicon carbide, but this feature could be used for water layer cover rate calculation. A software called image J is being used for single-layer graphene coverage rate calculation. In Fig.23, though proportion of different layer graphene area, the single graphene coverage rate could calculate. The full area of SPM image is 16μm^2, the single-layer graphene coverage area

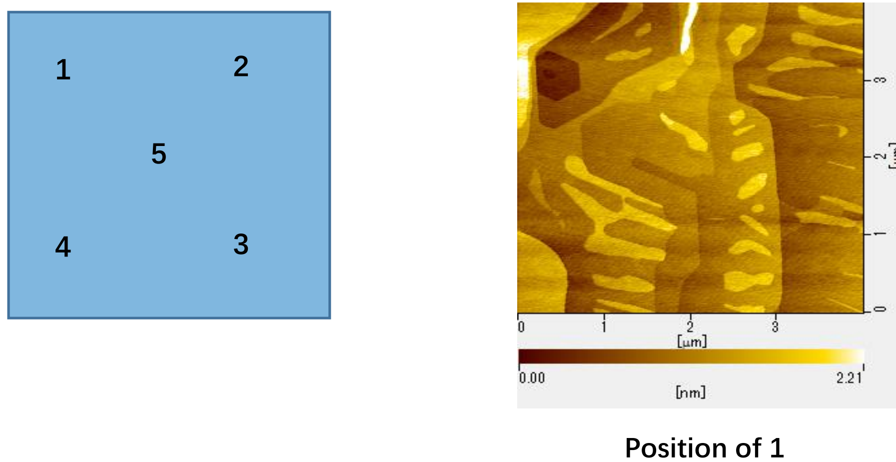
is about 13.177μm^2 and the single graphene coverage rate is about 82.36%, which is high coverage with single-layer graphene sample.



(a) (b)

Fig.23. (a)The Phase imaging of graphene sample L20. (b) is the image processing of (a) for single-layer graphene coverage rate.

Fig.24 is the SPM image of sample L19 with five points, which could infer all the graphene on SiC substrate. In this experiment, SPM measurement also takes the 5 points to confirm graphene on SiC substrate, the graphene layer is clearly observed.



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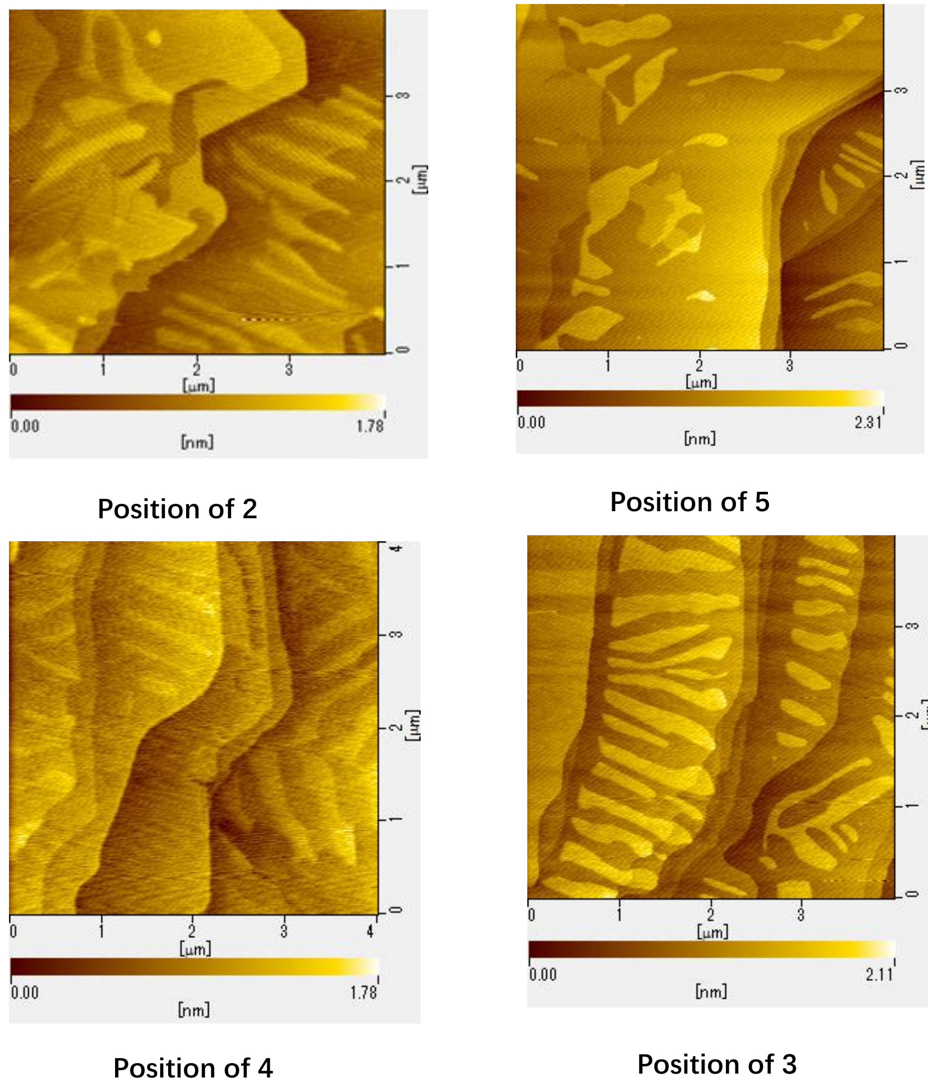


Fig.24 SPM graph of graphene L19 before the experiment.

1.4 Graphene application

Since single-layer graphene been reported in 2004[3], graphene become one of the most popular candidate material for research. The prominent of graphene principles lead graphene have applications include lightweight, thin, and flexible electric/photonics circuits, solar cells, and various medical, chemical and industrial processes enhanced or enabled by the use of new graphene materials. In graphene application, the most brilliant

scientific achievements are in medicine sensor and electronic devices.

For medicine, Graphene has effect on accelerating the osteogenic differentiation of human mesenchymal stem cells without biochemical inducers was found in 2011 [80]. Graphene biosensors were being used by biology researchers as a protein binding sensor platform has been reported in 2016. [81] In the same year, uncoated graphene can be used as neuro-interface electrode without altering or damaging properties was related. Graphene electrodes in the body are significantly more stable than electrodes of tungsten or silicon because of properties such as flexibility, bio-compatibility, and conductivity. For sensors, due to the stability of graphene in air and biological fluids, graphene became an attractive material for use as a biosensor [82]. A graphene circuit can be configured as a field-effect biosensor by applying biological capture molecules and blocking layers to the graphene, then controlling the voltage difference between the graphene and the liquid that includes the biological test sample. The biosensor is the first available for sale in various type of fabricated graphene sensors [83].

The excellent properties of high carrier mobility and low noise of graphene have stimulated much interest for applications in new generation novel functional electronic devices, such as graphene as the channel in a field-effect transistor [84], vertically stacked junction diode.

1.4.1 Graphene junction diode

Diode is a semiconductor device with two terminals, typically allowing the flow of current in one direction only. Junction diode is a kind of semiconductor diode, include p–n junction diode and Schottky diode. Due to graphene properties and ease of manipulation, graphene offers the possibility of integration with the existing semiconductor technology for post-silicon electronics and sensing devices. Since 2004, single-layer graphene been observed, the scientist focused on the more complex graphene transistors. Studies of the past few years have demonstrated that graphene can form junctions with 3D or 2D semiconducting materials which have rectifying characteristics and behave as excellent

semiconductor diodes. Here graphene p–n junction diode and graphene Schottky diode will before introduce respectively.

Graphene P-N junction diode

For P-N junction diode, it usually made of crystal semiconductor silicon, but germanium and gallium arsenide are also being reported for fabrication. Though doping to semiconductor materials, negative charge carriers (electrons), n-type semiconductor region is created. Another positive charge carriers (holes), a p-type semiconductor region is also being created. When the N-type and P-type materials are attached together, a momentary flow of electrons occurs from the N to the P side resulting in a third region (depletion region) between the two where no charge carriers (neither electrons nor holes) are present. The boundary between n-type and p-type regions, called p–n junction, where is the action of the diode. When higher electrical potential is applied to P side (the anode) than to the N side (the cathode), electrons are being allowed flow through depletion region. Instead, electrons flow been stopped in the opposite direction.

The team of Sung Kim el. report fabricate and characterize of a vertical-type graphene p-n junction with two terminals. The symmetric rectifying behavior is an important characteristic of vertical junctions, which is showing on/off ratio of ~10^3 under bias voltages below ± 10 V without gating at higher n doping concentrations, which have the prospect for practical device applications [85].

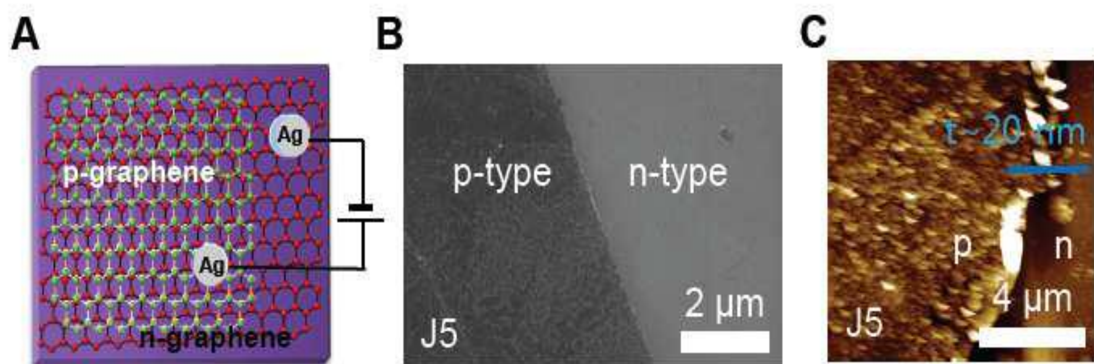


Fig. 25 (A) A schematic and (B, C) SEM/AFM images of a typical graphene p-n vertical junction where the doping times of the p and n layers are 5 and 4 min, respectively.

Graphene Schottky diode

Schottky diode is another type of junction diode also known as Schottky barrier diode or hot-carrier diode which is a semiconductor diode formed by the junction of a semiconductor with metal. The feature of tunable Schottky barrier height makes the graphene/semiconductor junction a great platform for the study of interface transport mechanisms as well as for applications in photo-detection, high-speed communications, solar cells, chemical and biological sensing, etc.

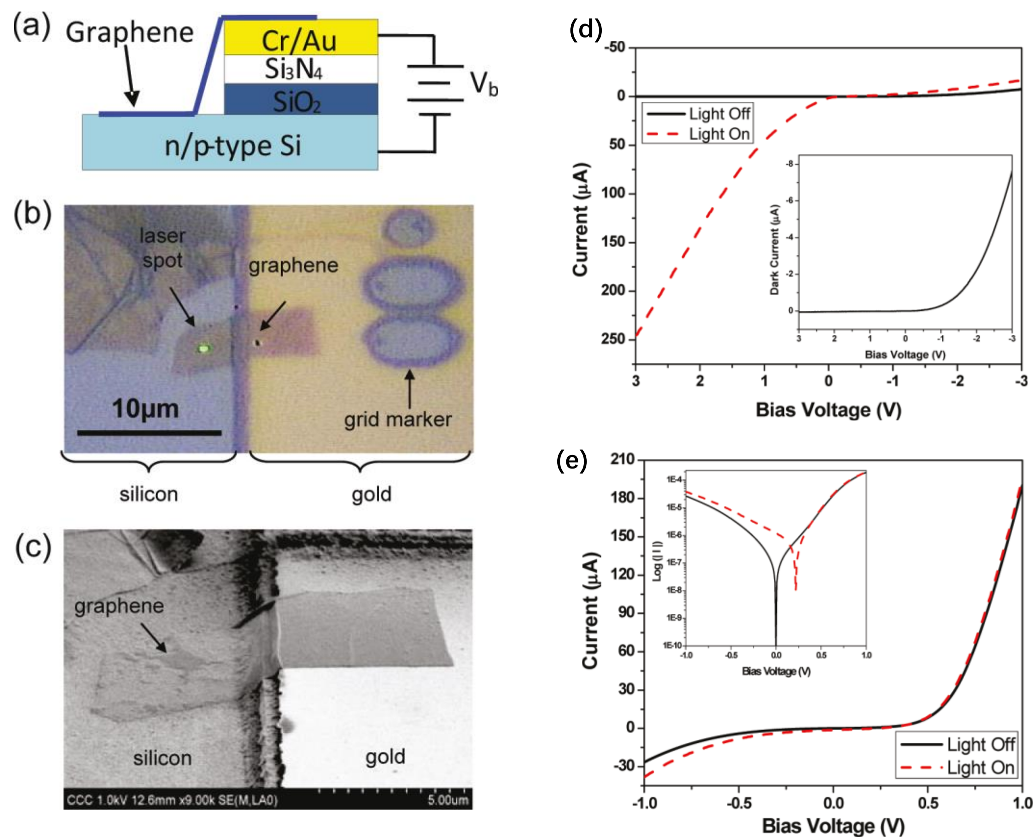


Fig. 26 (a) Schematic diagram (b) optical micrograph, and (c) SEM image of graphene on n-type silicon Schottky diode. (d) Current-voltage characteristics of graphene on n-Si device with and without illumination. The inset figure shows current on a log scale. (e) Current-voltage characteristics of graphene on p-Si Schottky diode with and without illumination. Inset shows the enlarged dark current-voltage characteristics [86].

A graphene-silicon Schottky diode by depositing mechanically exfoliated graphene

on top of silicon substrates is been reported by Chun-Chung Chen el. in Fig.26. The *I-V* characteristics show the rectifying diode behavior with barrier energy of 0.41 eV on n-type silicon and 0.45 eV on p-type silicon at the room temperature. The *I-V* characteristics measured at 100, 300, and 400 K indicate that temperature strongly influences the ideality factor of graphene-silicon Schottky diodes. Ideality factor does not depend strongly on the number of graphene layers. The optical transparency of the thin graphene layer allows the underlying silicon substrate to absorb incident laser light and generate a photocurrent. Spatially resolved photocurrent measurements reveal the importance of inhomogeneity and series resistance in the devices.

1.4.2 Graphene application for field-effect transistors

The ambipolar behavior and nano-electronic conductance is the advantage of graphene for the application of electronic devices, especially for graphene-based field-effect transistors. Graphene field-effect transistors (GFETs) take the typical FET device and insert micron-size graphene channel tens between the source and drain. The main GFETs device structures include bottom-gated, top-gated, double-gated, and suspended structure, etc. [87]. For bottom-gated GFETs, highly doped Si with 300nm thickness SiO_2 as gate insulator always been chosen for substrate. The graphene layer is fabricated by mechanically exfoliating method or chemical vapor deposition(CVD) method and lithography is used for pattern transfer. The drain and source(D/S) electrodes preparation by electron beam evaporation and lift-off process. The first bottom-gated GFETs fabricated with graphene films prepared by mechanical exfoliation of small mesas of highly oriented pyrolytic graphite by Novoselov's team in Fig.26[24,87]. Fig.26 shows exfoliating graphene film and AFM image, including a good structure and a single layer behavior.

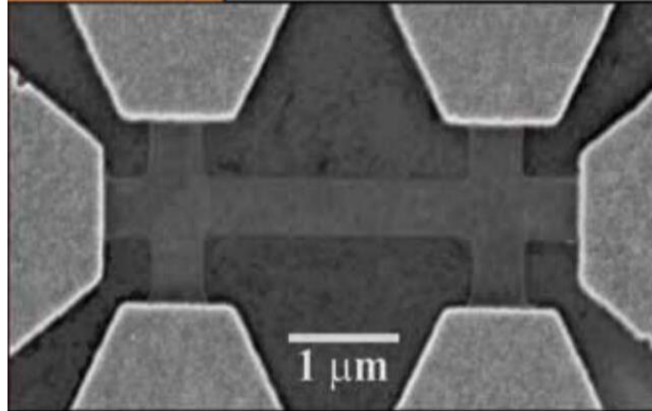


Fig.27 Scanning electron microscope image of Schematic view of the device in.

Top-gate graphene FETs are generally more flexible in terms of circuitry, but experimental results show that the top gate GFETs mobility is lower than the bottom-gate GFETs. The reason is the top gate, more scattering source induced by additional top-gate insulator. Another reason is damage of graphene in the preparing processing of the top-gate structure. This reasoning lead keeps graphene have good mobility became one of the important parts of top-gate GFETs fabrication. An Al_2O_3 as top-gate dielectric was reported by Seyoung Kim as shown in Fig.28[88].

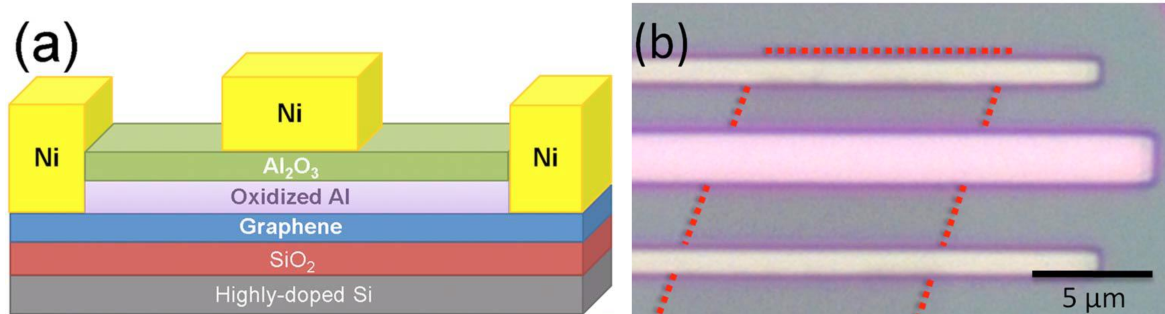


Fig.28 (a) Schematic of the dual-gated graphene FET structure. (b)Optical microscope image of a graphene FET.

Since the graphene carriers are scattering of charged impurity and surface polar phonons, the mobility of graphene is greatly reduced. For graphene intrinsic mobility

measurement, the suspended graphene transistor is derived. Graphene and substrate is not contact directly that lead scattering mechanisms associated with the substrate could be overcome. In 2008, K. I. Bolontin el. reported mobility in excess of 200,000 cm^2 /Vs at electron densities of ~2×10^{11} cm^{-2} by suspending single-layer graphene [89]. The fabrication of suspended graphene transistor is same as back-gated GFETs, SiO_2 substrate is etched by etching liquid after suspended structure fabricated. Graphene in the channel region is suspended been shown in Fig.29.

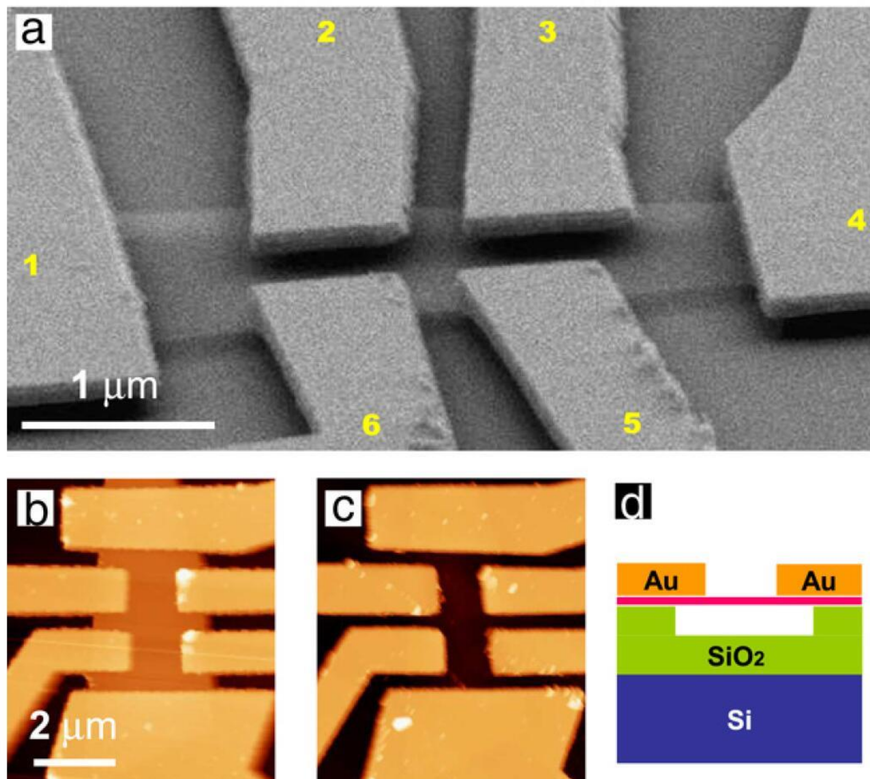


Fig.29 Suspended graphene Based field transistor (GFETs). (a) SEM image of a typical suspended six-probe graphene device. (b) and (c) AFM image of the suspended device. (d) Device schematic, side view. Degenerately doped silicon gate (blue), partly etched SiO_2 (green), suspended single-layer graphene (pink) and Au/Cr electrodes (orange).

1.4.3 Vertically stacked graphene tunnel transistor

In tunnel junction, electrons are transported through a thin insulating barrier, from one electrode to the other, and this thin insulator material has a performance impact of junction. Therefore, research on barrier material become attended to that lead atomically thin two-dimensional materials such as hexagonal boron nitride (h-BN) and molybdenum disulfide (MoS_2) were utilized as tunneling barrier [90-96].

Here we introduce a few atomic layers thick h-BN barrier resonant tunneling in Fig.30 from L. Britnell et al. in 2013, which have potential applications for high-frequency and logic devices [90]. A resonant tunneling device in which carriers tunnel through tens of nanometers thick boron nitride barrier layer sandwiched between two graphene electrodes across which a bias voltage is applied.

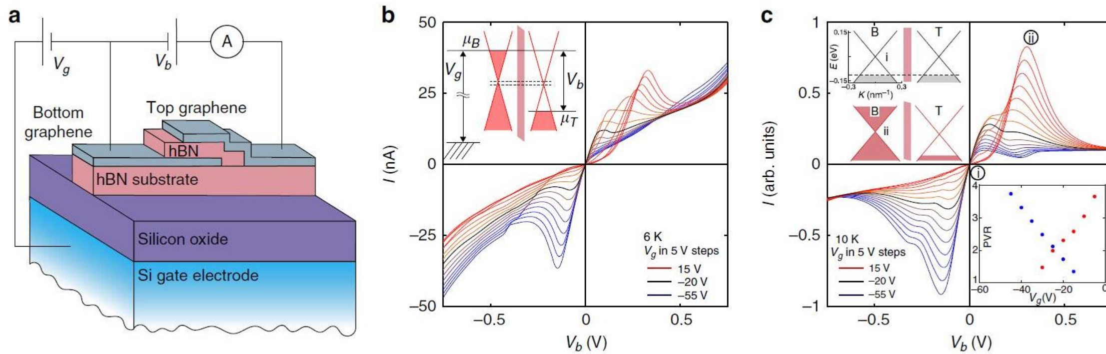


Fig. 30 Graphene-BN resonant tunneling transistor. (a) Schematic diagram of the devices. (b) Measured current-voltage characteristics of one device at 6 K. The h-BN barrier is four atomic layers thick, as determined by atomic force microscopy and optical contrast [91]; (c) Theoretical simulation of device A obtained by using the Bardeen model and including the effect of doping in both graphene electrodes.

The material of molybdenum disulfide (MoS_2) is also one of popular candidate of barrier material. A new generation of vertical field-effect transistors (VFETs) with MoS_2 (5–7 layers of MoS_2 (~ 2.5–4 nm)) tunneling barrier was reported in 2013[92] by Woo Jong Yu et al., though sandwiching few-layer MoS_2 as the semiconducting channel

between a monolayer graphene sheet and a metal thin film, on-off ratio>10^3 and a high current density of up to 5000A/cm^{-2} at room temperature. The ability to simultaneously achieve a high on-off ratio, a high current density and a logic function in such vertically stacked multi-heterostructures can open up possibilities for three-dimensional integration in future electronics.

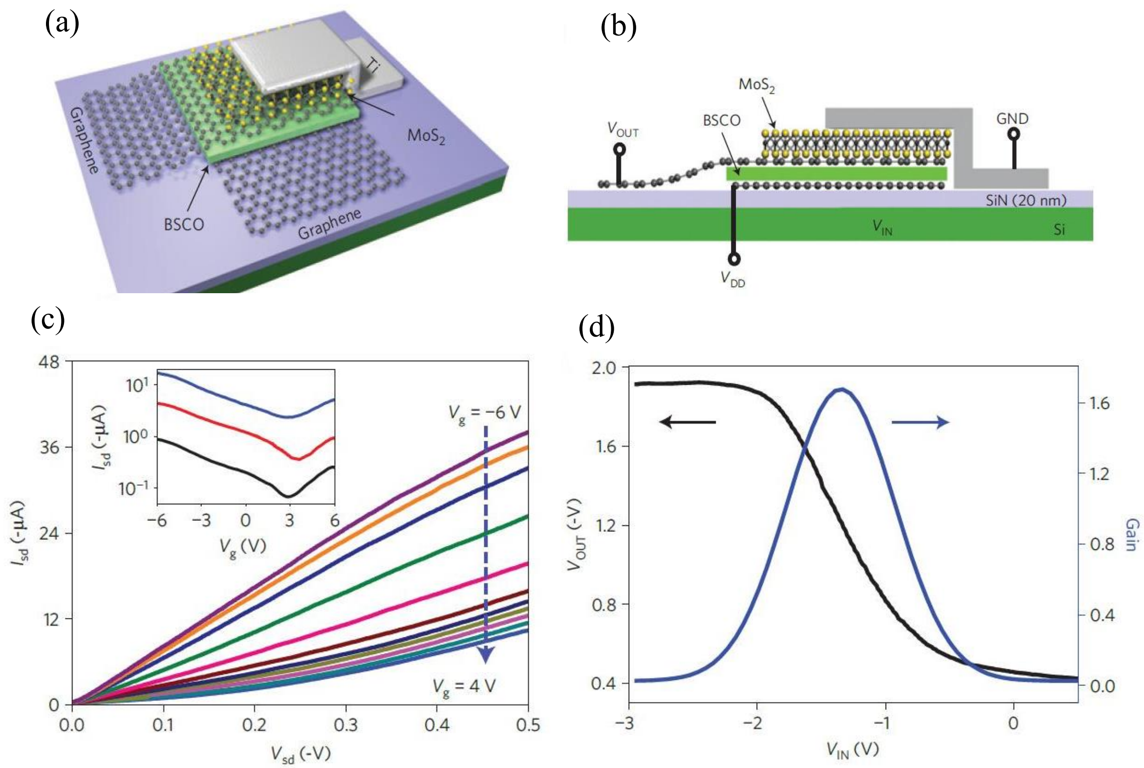


Fig. 31 Schematic illustration of the vertically stacked graphene–MoS_2–metal FETs. (a), A schematic illustration of the three-dimensional view of the device layout. (b) a schematic illustration of the cross-sectional view of the device, with the graphene and top metal thin-film functioning as the source and drain electrodes, and the MoS_2 layer as the vertically stacked semiconducting channel. (c) the output characteristic of this FET. (d) The inverter characteristics from vertically stacked p- and n-type VFETs.

2. Terahertz Technology

2.1 Introduce of terahertz technology

The terahertz(THz) waveband is between the microwave and infrared wavebands. The frequency range is being defined as 0.1-10 THz (wavelength is 30-3000um), and the photon energy is 0.4-40meV. In certain cases, the frequency range is extended to 0.1-30THz [97]. As shown in Fig. 32, terahertz wave coincides with the millimeter wave in the low frequency band and coincides with the infrared light in the high frequency band, which is a transition region from electronics to photonics. Due to the lack of effective terahertz emission and detection technology, terahertz waves were not widely developed and utilized until the 1980s [98].

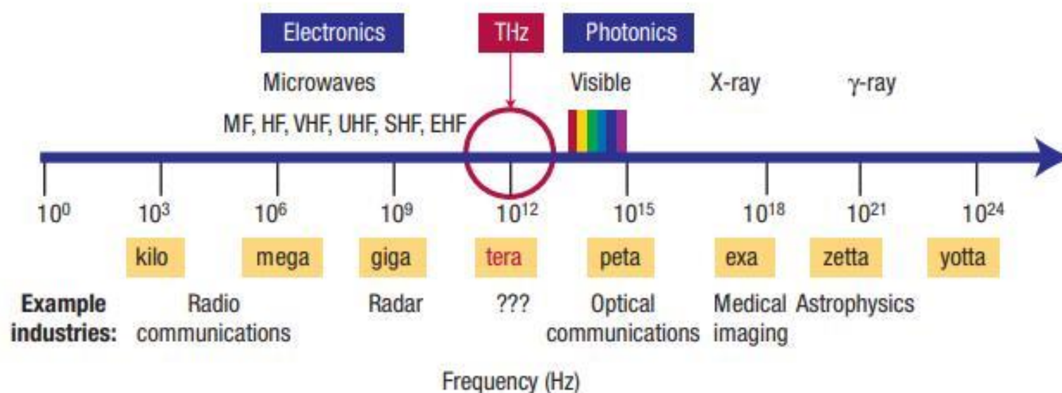


Fig. 32 The electromagnetic spectrum. The development of efficient emitters and detectors within each of the spectral regimes has resulted in the birth of numerous industries. The search for potential applications of THz radiation is steadily intensifying as materials research provides improved sources and detectors (graph from Bradley Ferguson) [99].

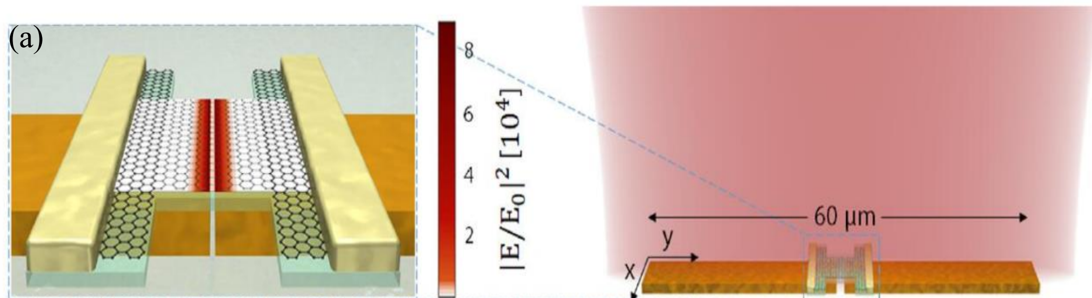
In the 1980s, D. H. Auston et al. successfully produced a photoconductive antenna (PCA) for terahertz emission and detection at Bell Labs. This discovery is the foundation for the rapid development of terahertz [100]. In 1989, Ch. Fattinger et al. used ultrafast dipoles to obtain diffraction-limited terahertz waves, thereby achieving 100cm distance

transmission [101]; In 1992, Zhang et al. use coherent techniques of electro-optic materials got terahertz wave [102]; In 1995, Wu et al. use free-space optical sampling technology to achieve ultra-wideband too Hertz detection [103]. From the 1990s to the beginning of the 21st century, the development of terahertz science has been spurred until the emergence of the terahertz time-domain spectrum concept, which has pushed terahertz technology from laboratory research to commercial applications [104].

2.2 Graphene application for terahertz

In the terahertz regime, graphene is also one of the most prosperous materials in modulating the propagation properties of the terahertz wave. One way to realize such modulation is to apply external voltage on the graphene–insulator–graphene structures, so that the Fermi level in graphene could be tuned accordingly and thus the optical conductivity due to the intraband transition process or free carrier absorption [105-110]. However, graphene-based terahertz modulators have seldom been studied under the simultaneous influence of both the external voltage bias and optical pump excitation.

A terahertz radiation novel detector dipolar antenna with a gap of ~100 nm is reported in 2019[111]. A p-n junction in a graphene channel is created, where the photoresponse is created. The noise-equivalent power of 80 pW at room temperature, a response time below 30 ns (setup-limited), a high dynamic range (linear power dependence over more than 3 orders of magnitude) and broadband operation (measured range 1.8–4.2 THz, antenna-limited).



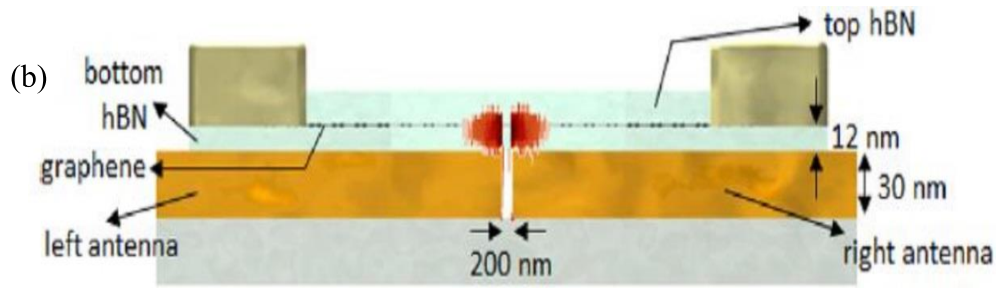


Fig.33 (a) Schematic representation (right; not to scale) of the antenna-integrated p-n junction device and a zoom of the central part of the THz PTE detector (left; to scale), consisting of an "H-shaped" graphene channel, contacted by source and drain electrodes. (b) Side view of the device design, with the superimposed color map again indicating the normalized power profile as in panel a. The region where the field is strongly enhanced by the antenna overlaps with the central part of the graphene channel.

In 2015, graphene-silicon hybrid film active diode for the terahertz waves is reported. The diode transmits terahertz waves when biased with a positive voltage while attenuates the wave under a low negative voltage, which can be seen as an analogue of an electronic semiconductor diode. In this graphene-silicon hybrid film active diode, we obtain a large transmission modulation of 83%, which have applications in designing broadband terahertz modulators and switchable terahertz plasmatic [112].

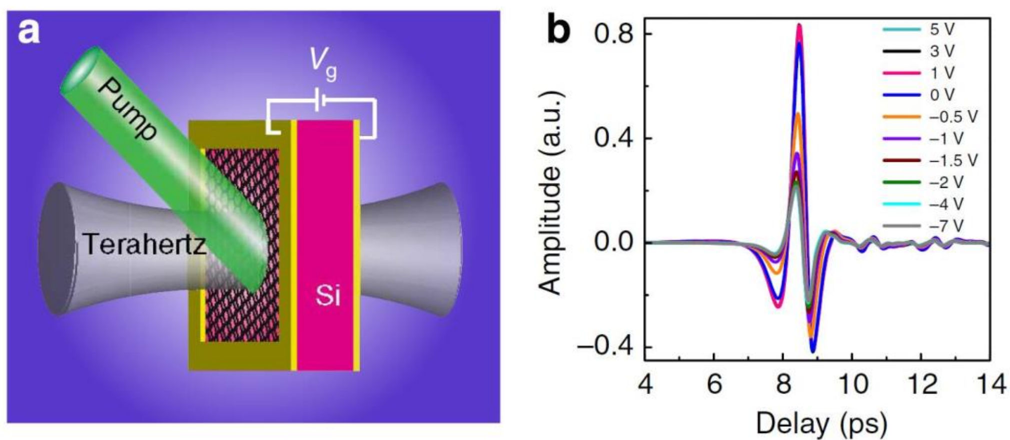
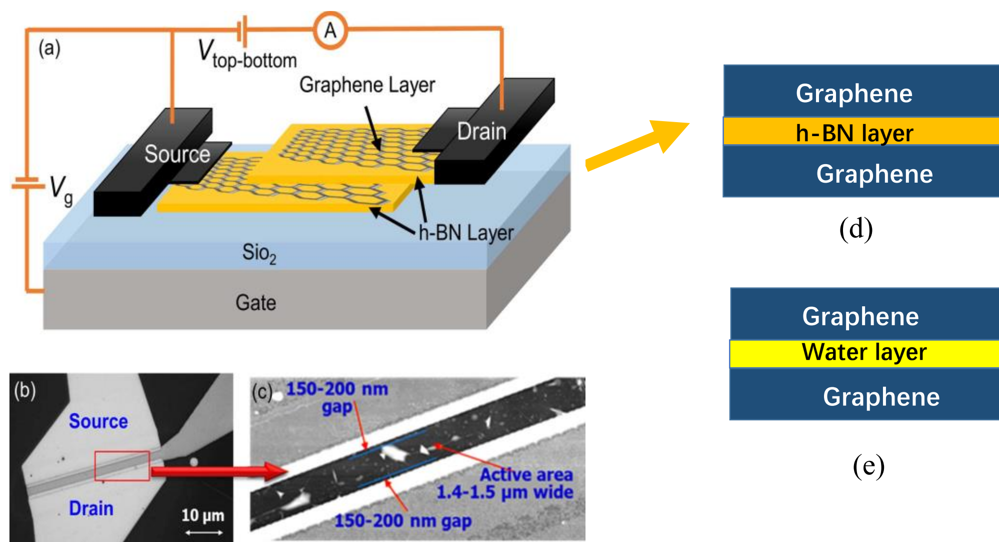
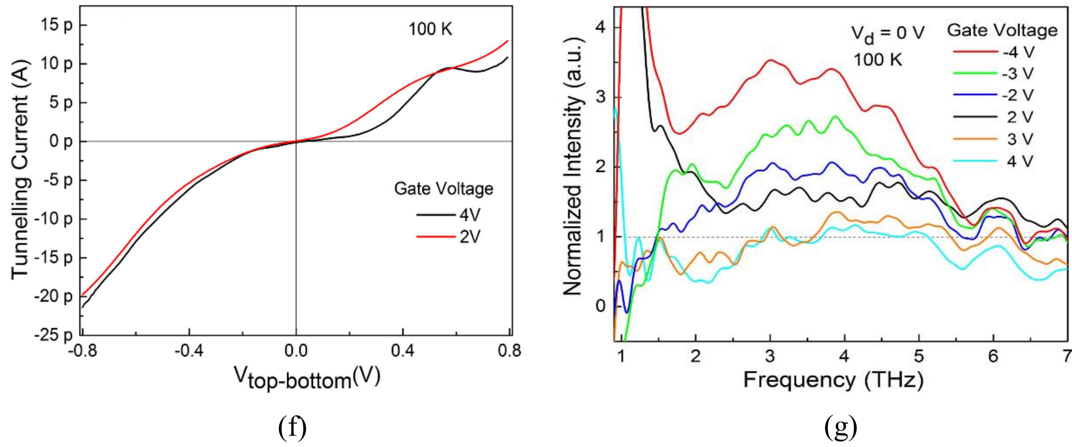


Fig.34 Experimental design and normalized time-domain signals. (a) Illustration of the GSTD sample. The double-layer graphene on the silicon substrate was photo-excited with green light and

biased with voltage Vg. (b) Normalized terahertz time-domain signals at various gate bias voltages under a photoexcitation power of 280mW [112].

The first double graphene layered (GL) heterostructure for Terahertz emission was reported in 2016 by Deepika Yadav et.al of a graphene /h-BN / graphene GFET structure. For our junction diode is a graphene /structure water /graphene structure that speculate have application prospect in THz emission. In Deepika Yadav et.al research, a thin hexagonal-boron nitride tunnel barrier layer sandwiched between two separately contacted GLs. In this double-graphene layered (DGL) heterostructures, resonant tunneling and negative differential resistance are expected when the two graphene band structures are perfectly aligned. In the case of small misalignments demonstrate that the photon-absorption/emission-assisted non-resonant and resonant-tunneling causes all excess charges in the n-type GL to recombine with the holes in the p-type GL giving rise to an increased measured dc current.





(f) (g)

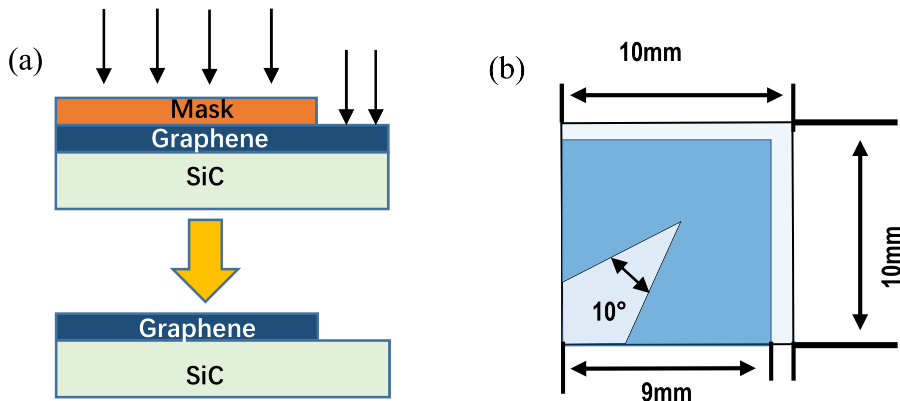
Fig.35 (a) The schematic of the fabricated DGL device. (b) SEM image of the device showing the position of the source and drain electrodes (light gray), the active area of the device (dark gray) and the SiO2 substrate (black) when viewed from top. (c) A zoomed SEM image showing active area of the device to be 1.4–1.5μm wide. (d) The junction structure of graphene/ h-BN/graphene GFET structure. (e) The junction structure of graphene/ structure water /graphene junction diode in this thesis. (f) Measured I–V curves of device at 100 K exhibiting weak NDCs. (g) Measured emission spectra at different gate bias voltages at drain bias of 0 V at 100 K [113].

3. Preparation for Graphene Stacked Junction Diode

In this chapter, stacked graphene junction diode fabrication will introduce from acrylic molds design. The experiment result of Current-Voltage characteristic, Direct tunneling (DT) phenomena, and Fowler-Nordheim tunneling (FNT) phenomena result also will introduce as comparative analysis. Based on both DT and FNT phenomena are observed in junction diode, which means the insulator water layer sandwiched between graphene samples is very thin, the thickness of this water and other parameters are calculated in experiment result analysis.

3.1 Graphene samples etching

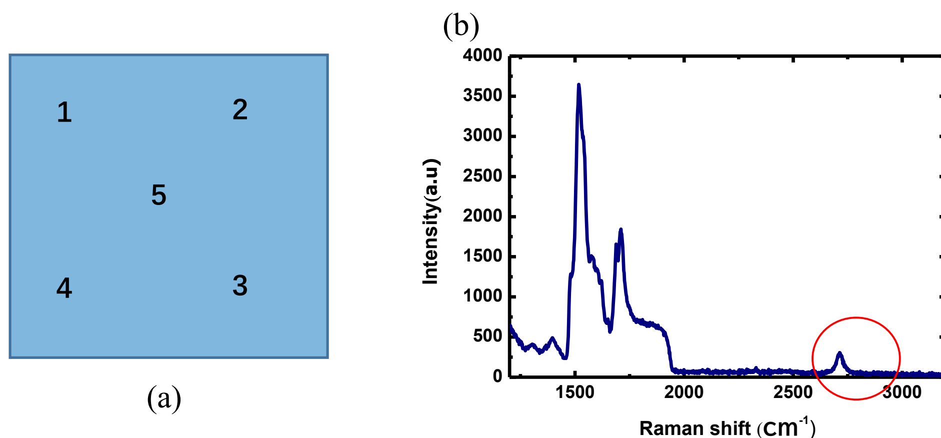
In the experiment, junction diode A is fabricated based on two graphene samples with patterning etching. The etching function is based on the bombardment of ions which are accelerated onto the substrate attracted by the negatively charged substrate. For the first junction diode, Junction A, before constructing the stacked junction, ion etching been used for graphene sample etching which could keep the graphene contact region with high-quality graphene (Remove edge region graphene that has damage potentially). The samples were patterned to limit the square junction region, by employing stencil lithography. The plastic film was patterned using laser machine placed on the sample surface and the samples were subjected to ion etching to remove the uncovered graphene on the SiC through E-1030 HITACHI ion sputter in Fig.36 (c).



(c)

Fig. 36 (a) shows the process of graphene sample etching. (b) Graphene sample patterned design. (c) is the etching equipment E -1030 HITACHI ion sputter for this experiment.

In our experiment, Raman is used to confirming surface morphology, in Fig.37(a), and the Rama measurement is point for measurement. If we want to know all the surface condition 5 points test is necessary. Here for a graphene sample from point 1 to 5 are the area for measurement. The Raman measurement result is given in Fig.37 that could confirm graphene is covered on SiC substrate. Here we give two graphene samples Raman measurement results of one junction for representing. Fig 37. is the Raman shift measurement result of sample L19 in Junction A.



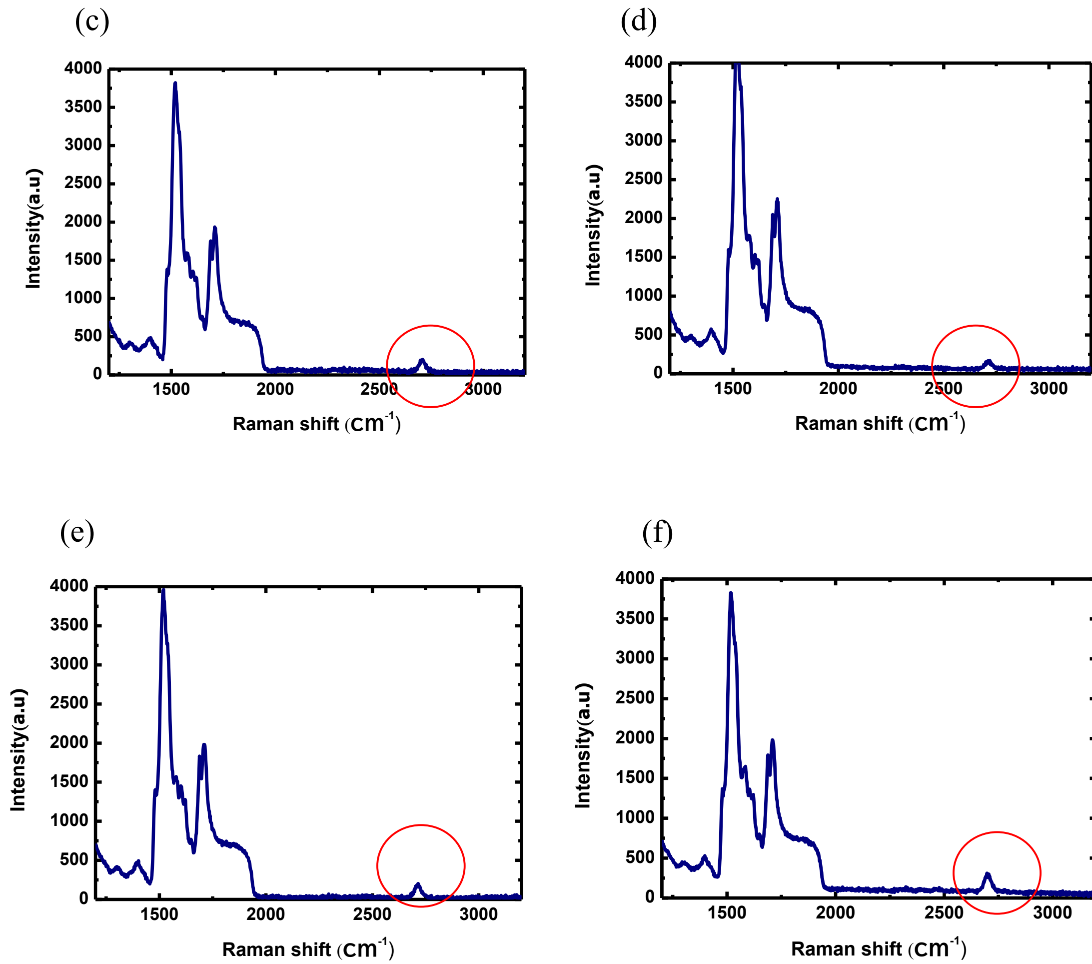
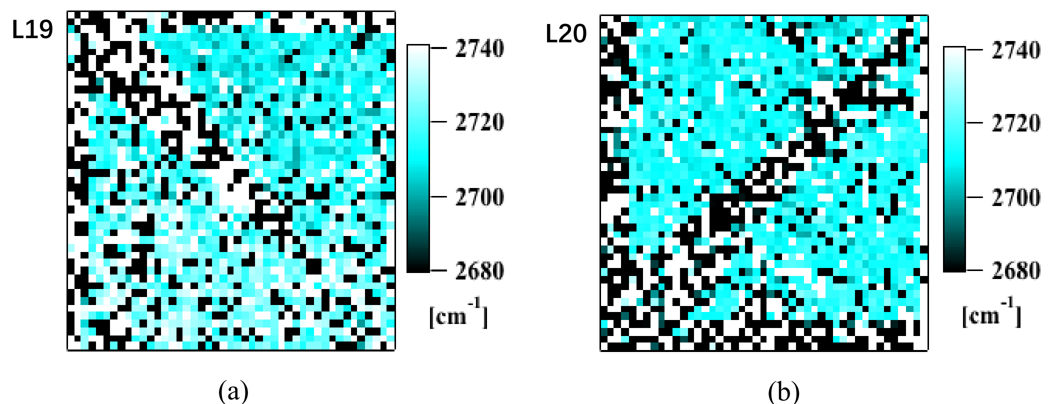
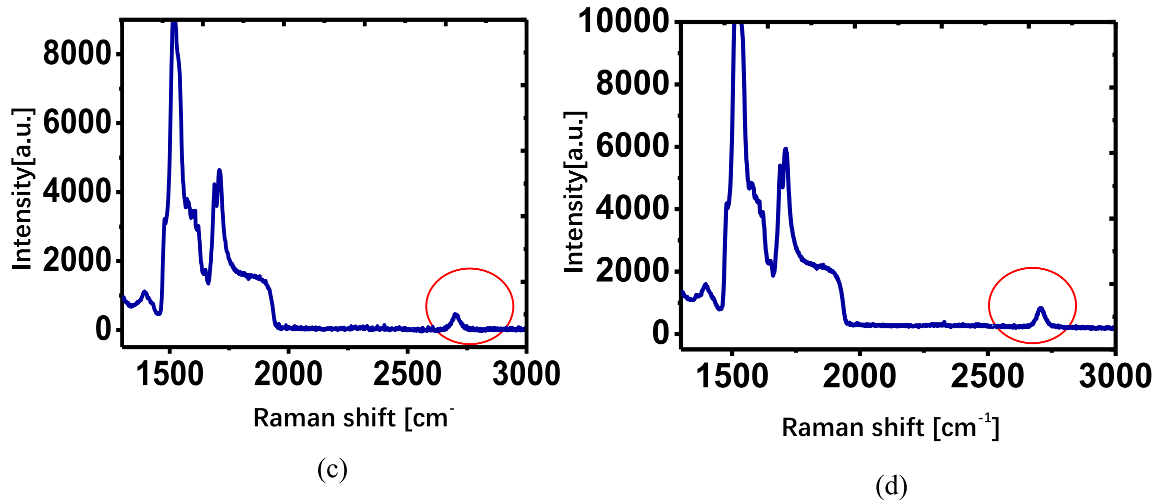


Fig. 37 (a) is the measurement location diagram of Raman spectroscopy, (b)~(f) is sample L19 Raman result, from point 1 to 5 and the red cycle is graphene peak near 2700 cm^{-1}.

Raman mapping is an effective means for full sample surface measurement, in Fig.38 (a) and (b) etching pattern is observed from Raman mapping image.





(c)

(d)

Fig.38 (a) and (b) are the 2 D peak Raman mapping of graphene sample L19 and L20 for Junction A.(c)and (d) are the Raman shift result of L19 and L20, respectively.

3.2 Acrylic molds design and fabrication

In graphene stacked junction diode fabrication, we design different types of acrylic molds for junction diode comparative analysis. For junction diode A, a pair of 50mm size acrylic molds were used for fixing graphene samples, the middle hole is for graphene junction region observation. And four screws of M 0.5 are designed for contact to the connecting wire. Graphene samples are sandwiched between the acrylic molds and electronic principles are measurement though metal screws. The four points of A, B, 1, 2 is the place of metal screws contact conductor for *I-V* characteristic measurement. Though the circular region in the middle of acrylic molds, the temperature of junction region could measurement through thermographic camera.

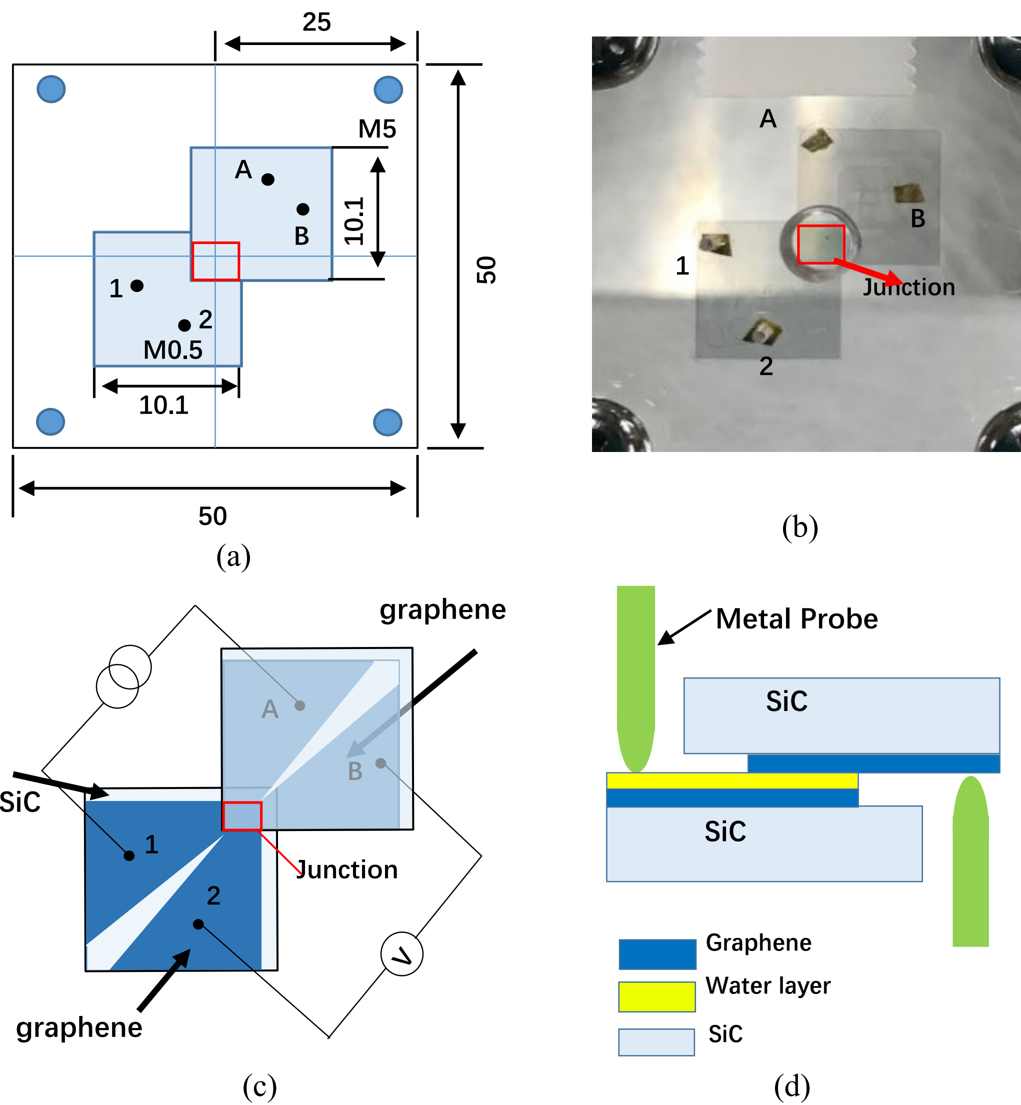


Fig.39 (a)The schematic of acrylic molds design for junction A. The four black dots are the hole for metal screws, which for a connecting wire. (b)Photograph acrylic molds of junction A. (c) Structure charts of tunnel junction A for ion-beam sputter treated graphene samples. (d) Cross-sectional schematic of water layer barrier junction, the water layer covers graphene surface and metal probes are used for measurement.

In acrylic molds design of junction diode A, two samples were stacked in a face-to-face manner as shown in Fig. 39(c). The dark blue region is graphene and light blue region is SiC substrate after graphene removed. Four contact probes with gold sheets as contact materials were placed on the surfaces of the graphene samples. Two electrodes (1 and 2)

were connected to sample L19 and the other two electrodes (A and B) were connected to sample B. Sample L19 was immersed in DI water for 15 min to form the structured water layer on the graphene surface. The sample L19 and sample L20 were stacked each other in a face-to-face manner. The schematic of the stacked junction is shown in Fig.39(d). After bonding, the thickness of water layer should be not uniform because of the roughness of the sample surface. The distance of molds was controlled by four screws at corners of molds. The electrical measurements of the junctions were performed by a four-terminal method at room temperature under atmospheric conditions.

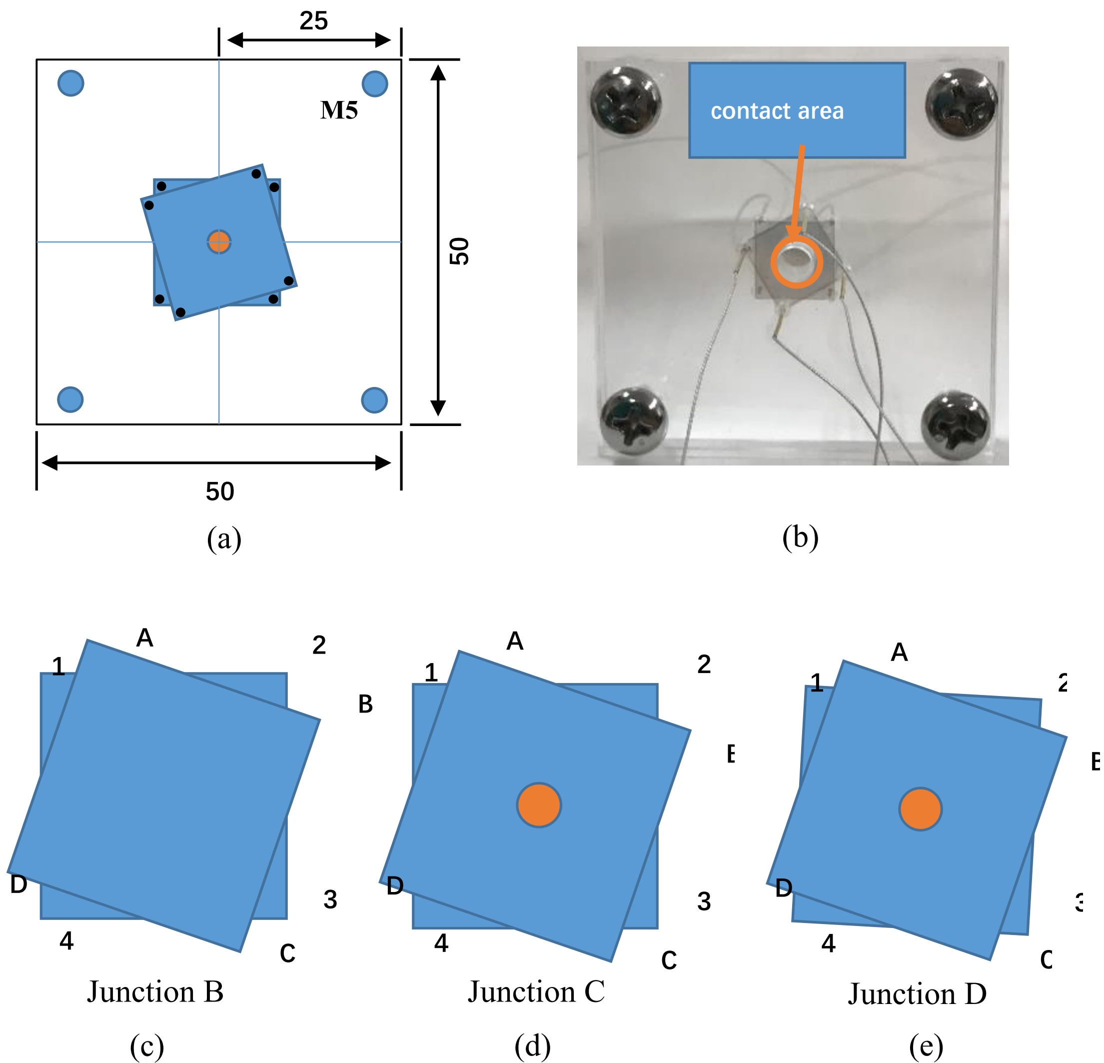


Fig. 40 (a) The design schematic of stacked graphene junction diode B, C, D. (b). The photograph of graphene tunnel junction device. (c) The schematic diagram of junction diode B. (d) The schematic

diagram of junction diode C, the middle cycle is a hole for graphene samples condition observation. (e) The schematic diagram of junction diode D.

In junction diode design of B, C, D, without etching graphene samples tunnel junction diode is design for high power junction diode. For this reason, a larger contact area junction diode was designed in Fig.40. The absence of negative differential conductance (NDC) of Current-Voltage(*I-V*) characteristic is an important criterion for determining whether graphene crystal orientation is consistent [114-115]. In order to observe NDC at low enough energies, graphene samples required aligned at sufficiently low energy (or gate voltage) so that their crystal axes are parallel. Consider about graphene crystal orientation, two graphene samples been stacks with 30-degree. There are two possibilities for graphene crystallographic axes are parallel, one is 'zig-zag' and the other is 'armchair,' but they cannot be distinguished well via optical micro zoom-scope observation [116]. When both the top and bottom GLs are aligned with the zig-zag edges or armchair edges, the misalignment could be very small (~1°or less), but the cases of one side with the zig-zag and the other with the armchair give rise to large misalignment(~30°). A pair of 50mm size acrylic molds were used for fixing graphene samples, the middle hole is for further research for junction power measurement. And this eight probes design is convenient for two-probe and four-probe measurement.

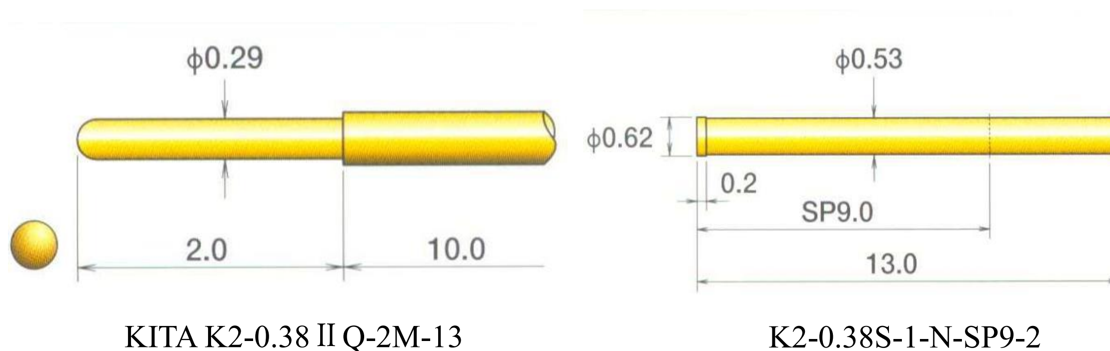


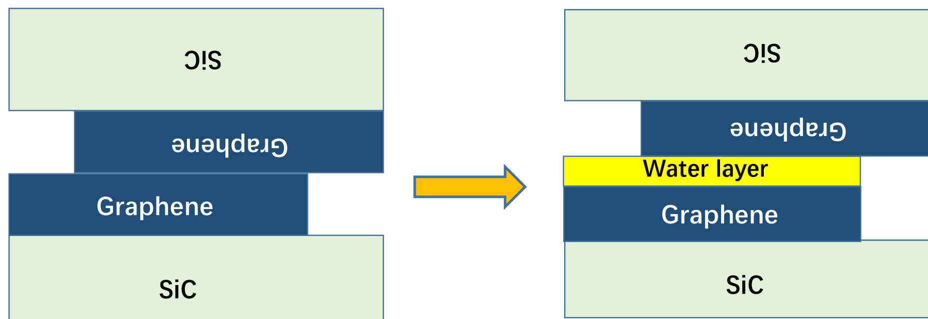
Fig. 41 The schematic of probe and lead for tunnel junction *I-V* measurement from KITA.

For better contact of graphene and probe, how to ensure probes contact with graphene

surface is needs to solve. For this reason, a type of scalable probe is applied in this experiment. The KITA K2-0.38 II Q-2M-13 probes and K2-0.38S-1-N-SP9-2 lead been chosen for junction measurement in Fig.23. The flexibility is the advantage of these probes, that could make sure the probes contact with graphene samples without the effect of screws. For this 8 probe design for measurement, the 2 probes test and 4 probes test could more convenient than junction A design which only has two screws on etch graphene sample.

3.3 The structure water layer fabrication on the graphene surface

In order to get water layer on the graphene surface, we let sample L19 immersed in DI water for 15 min to form structured water layer on the graphene surface. After formed structure water layer, two graphene samples been stacked with each other by face to face that lead water layer sandwiched between graphene samples. In Fig.42, this process is being shown by schematic, water layer interlayer between graphene samples in junction diode.



(a)Before water treat by pure water (b)After water treat by pure water.

Fig.42 The process of the structured water layer on graphene surface based on SiC substrate.

The topographic SPM image of the graphene surface after DI water treatment in Fig.43. The step-terrace structures originating from the SiC crystallography can be

observed. The lower terraces are covered by bilayer graphene with island-like structures. In the upper terraces, monolayer graphene is dominant. In the monolayer graphene region, hole structures are observed. The depth of the hole corresponds to be the thickness of the structured water layer formed by DI water treatment. The measured thickness of the water layer is approximately 0.46 nm, as shown in the cross-sectional profile of Fig. 43(a).

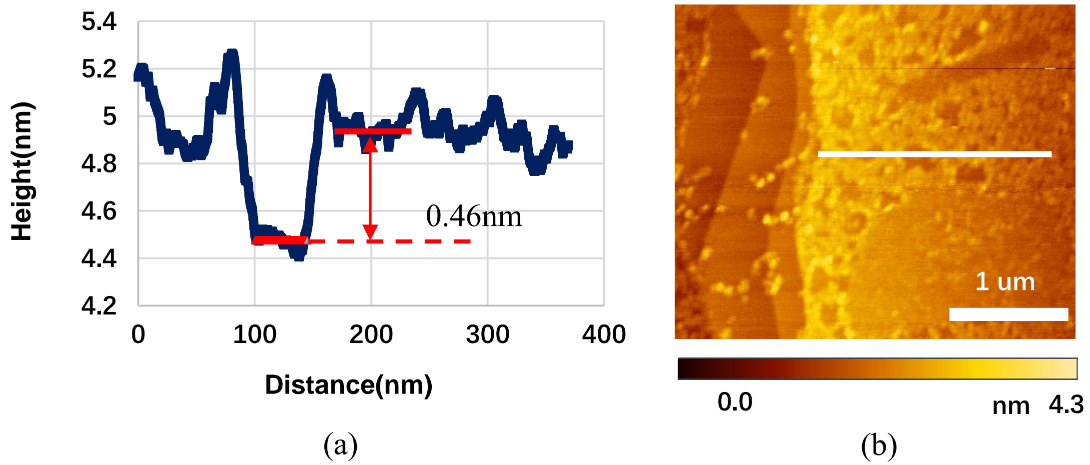


Fig. 43 (a) The thickness of water layer on graphene surface (b) Water treated graphene sample surface.

4. Electrical properties and analysis of stacked graphene junction diode

4.1 Current-voltage characteristic of graphene stacked junction diode

4.1.1 Electronic characteristics of graphene stacked junction diode A

The *I-V* characteristics of Junction A for graphene-graphene direct contact junction (without tunnel barrier) are shown in Fig.44(a). For stacked graphene junction diode, before the water layer structure is fabricated on graphene surface (graphene-graphene junction), the contact condition of two graphene samples is ohmic contact. But when the water layer as a tunnel barrier between tow graphene samples, the junction contact condition turns to tunnel junction (graphene/ water /graphene junction) in Fig.44(a) and (b).

Because the results of both two-terminal and four-terminal measurements were linear, it could be inferred that both the graphene-graphene and graphene-probe junctions established ohmic contacts. Before structure water layer fabricated graphene samples contact is ohmic contact also could be verified by Fig.44(a). The resistance of the graphene-graphene junction was 30.1 kΩ and the graphene-probe junction was 135.45 kΩ. After DI water treatment of one sample (sample A), the zero-bias resistance of the stacked junction increased drastically to approximately 1.3 GΩ. As shown in Fig.44 (b), non-linear *I-V* characteristics were observed. The semi-log plot of the *I-V* characteristics, shown in Fig.44(c), that the dynamic range of current change reached the sixth order of magnitude. The dI/dV curve of the stacked graphene junction with the water layer barrier is shown in Fig.44(d). The conductance is constant around zero voltage. This result suggests that the DT phenomenon may be observed in the low-electric-field region and will be discussed later.

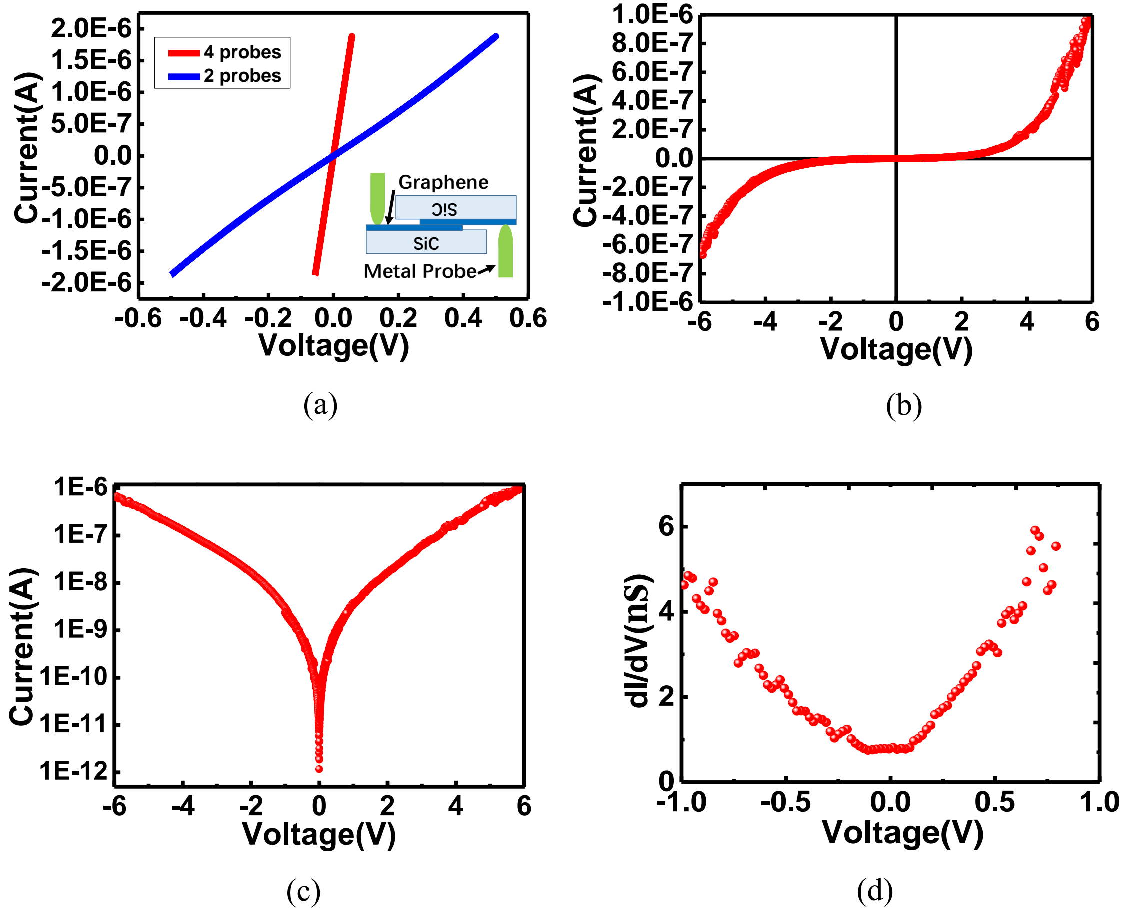


Fig. 44 (a) Current-voltage (*I-V*) characteristic curve of junction diode under different voltages at room temperature. The curve is for a graphene-graphene contact junction without a water barrier (before water treatment). Both two-terminal and four-terminal measurements show linear characteristics, which indicates that this junction without water barrier is an ohmic contact junction. (b) *I-V* Characteristics of graphene/ water barrier/ graphene tunnel junction. A non-linear curve is observed after introducing a water barrier to the junction. (c) Semi-log plot of this graphene/ water barrier/ graphene tunnel junction. (d) Differential conductance (dI/dV) curve of vertically stacked graphene junction with water barrier.

4.1.2 Electronic characteristics of graphene stacked junction diode B

Junction B is consisting of graphene samples P33 and P34 (both N-type), structured water layer is being sandwiched between these two graphene samples which form a graphene/ water layer/ graphene junction structure. For structure junction B, four-probe measurement is used for *I-V* measurement the same as junction A. The sheet resistance of samples is 4.55×10^{2} Ω/□ for sample P33 and 5.6×10^{2}Ω/□ for sample P34, respectively. Sheet carrier density is $1.58\times10^{13}cm^{-2}$ and $1.20\times10^{13}cm^{-2}$, respectively. The same as junction A, structured water layer is fabricated for tunnel barrier, number P34 graphene samples were water treated for 15 min for structure water layer on graphene surface. If the water layer is being structured, graphene surface will have covered with a water layer insulator material which lead us assume that water layer could be barrier material between graphene samples of tunnel Junction B. In Fig.45(a), 2 probes and 4 probes measurement result without water layer is shows here, which observed as straight line for ohmic contact characteristic.

A semi-log plot is a way of visualizing data that are related according to an exponential relationship. One axis is plotted on a logarithmic scale. This kind of plotting method is useful when one of the variables being plotted covers a large range of values and the other has only a restricted range the advantage being that it can bring out features in the data that would not easily be seen if both variables had been plotted linearly. Fig. 45(b) is *I-V* characteristics for junction B after DI water treatment of one sample (sample P34), the zero-bias resistance of the stacked junction increased drastically to approximately 0.65 MΩ. In Fig.45(b), a typically non-linear *I-V* characteristics curve was observed that is one feature of the tunnel junction. The semi-log plot of the *I-V* characteristics, shown in Fig.45(c), that the dynamic range of current change reached the third order of magnitude. The dI/dV curve of the stacked graphene junction with water layer barrier is shown in Fig.45(d). The conductance is constant around zero voltage with a large region compare with Junction A. This result suggests that DT phenomenon may

be observed in the low-electric-field region and will be discussed later.

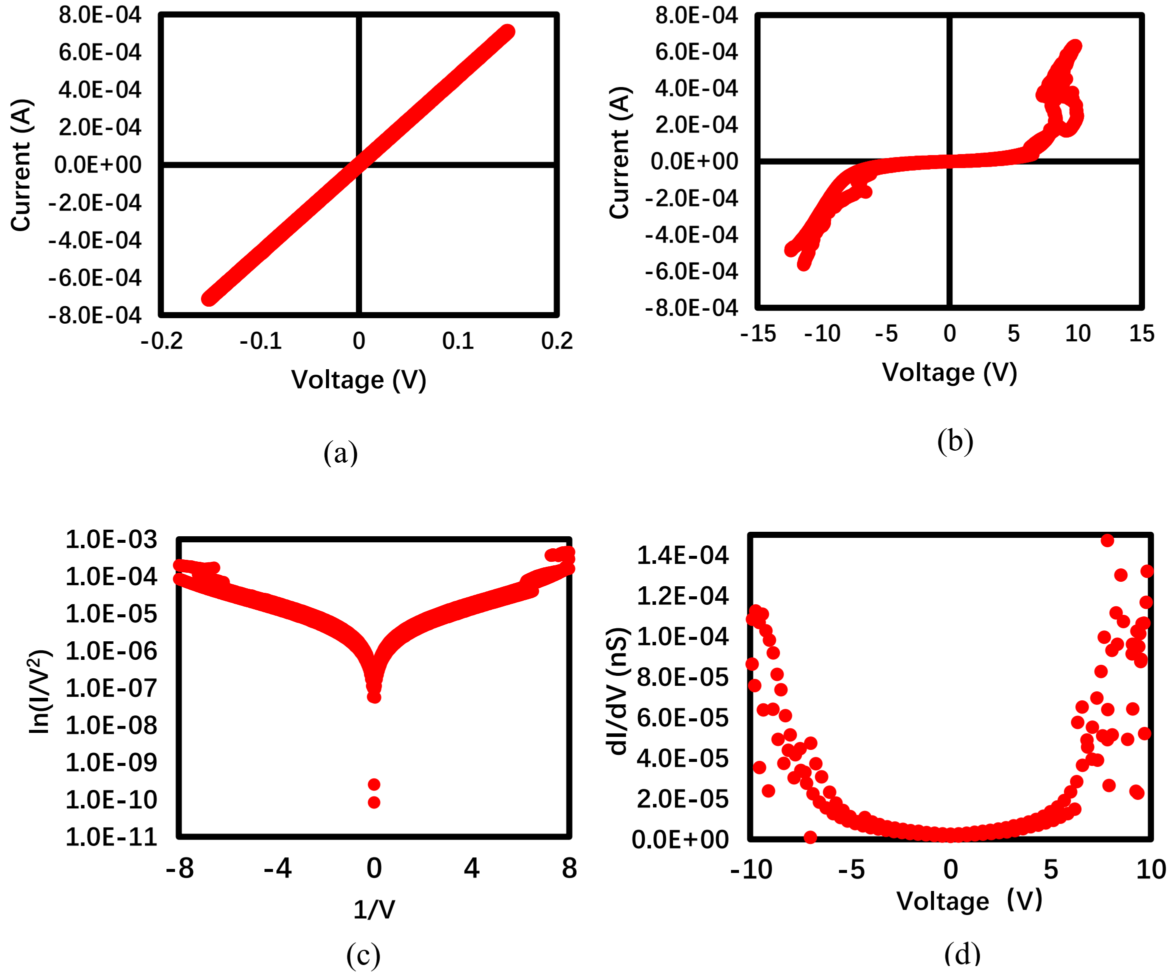
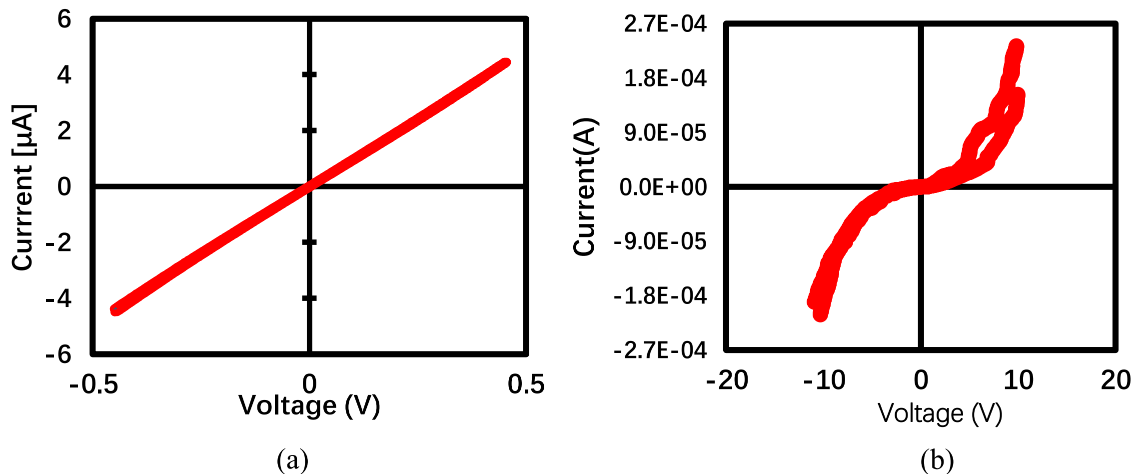


Fig. 45 (a) *I-V* curve of for a graphene-graphene contact junction without water barrier (before water treatment), the measurement result shows linear characteristics for ohmic contact. (b) *I-V* Characteristics of graphene/ water barrier/ graphene junction B at room temperature with different voltages. A non-linear curve is observed after fabricated a water layer insulator barrier to the junction. (c)Semi-log plot of junction B.(d) The dI/dV plot of junction B.

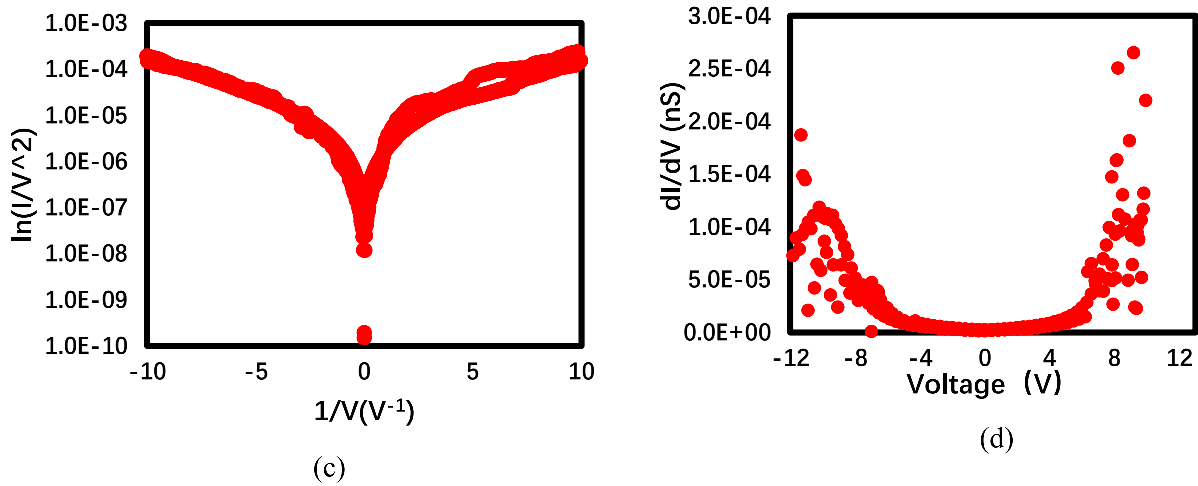
4.1.3 Electronic characteristics of graphene stacked junction diode C

Different with junction B, junction C and junction D have a hole in the middle of acrylic molds which is at the top middle of graphene samples junction region where the junction contact region most likely to appear. The middle hole on the acrylic molds is designed for the future research which is about junction power measurement by infrared camera to get relationship of power and time for Terahertz application. In junction C, the water layer insulator material is sandwiched between graphene samples P31 and P19 (both N-type) for *I-V* measurement.

In Fig.46(a), the *I-V* characteristic without structure water layer is observed as a straight line, which means this is an ohmic contact for graphene- graphene junction diode. This I-V characteristic is used for comparison with (b) junction diode *I-V* characteristics. Fig.46 (b) is the *I-V* curve with asymmetric behavior of junction D, the reason for this asymmetry is the work function difference between samples P19(water treated) and P31. Fig.46 (c) is the semi-log curve of graphene/ water layer /graphene junction diode, a semi-log plot is always used in narrow data feature describes. From this graph, the zero Voltage resistance could be reflected clearly about 0.43MΩ. Fig.46(d) is the dI/dV graph, the liner principle near-zero voltage is conforming to the relationship in DT phenomena *I-V* characteristic which could explain junction D is a tunnel junction with DT phenomenon is observed.



(a) (b)



(c)

(d)

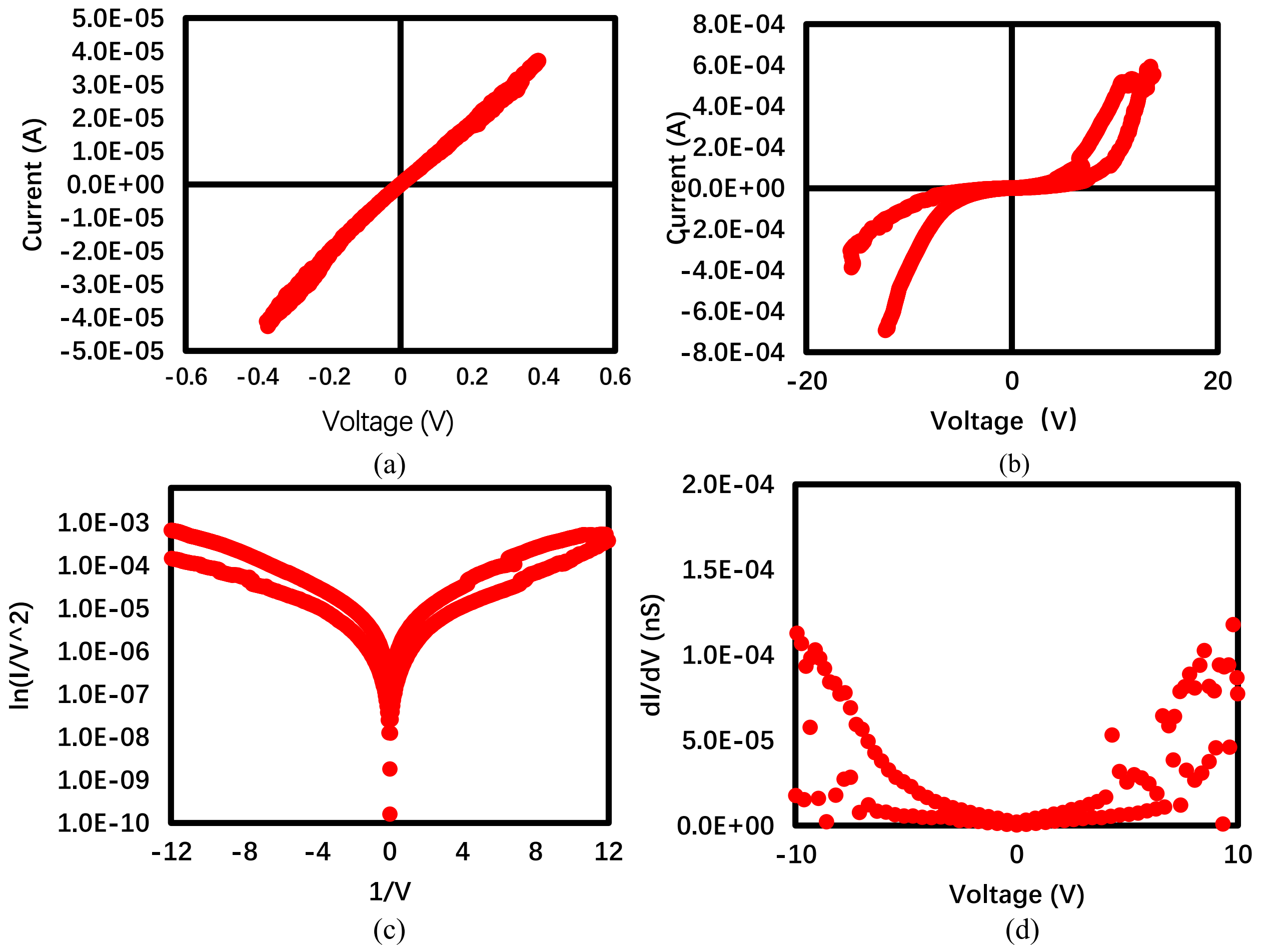
Fig.46 I-V characteristic of junction C (a) A liner *I-V* relationship for ohmic contact before structure water layer fabricate. (b) a typical nonlinear *I-V* curve with structure water layer of graphene /water layer /graphene junction. (c) semi-log plot for junction C. (d) dI/dV plot of graphene tunnel junction diode C. Near zero voltage, the curve present liner characteristic which is same as the current and voltage relationship in Direct tunneling (DT) phenomena. Based on this linear I-V relationship in (d), Direct tunneling (DT) phenomena is verified in this junction diode that only appear in very thin barrier material tunnel junction.

4.1.4Electronic characteristics of graphene stacked junction diode D

For junction diode D, in the middle of acrylic molds also have a hole for graphene junction region observe. The two graphene samples numbers are Q42(water treated for structure water layer) and M18. For Q42 sheet resistance is 9.36×10^{2} Ω/□, Carrier mobility is 417 cm^2/Vs. For M18, sheet resistance is 3.59×10^{2}Ω/□, Carrier mobility is 575 cm^2/Vs. Hall effect measurement gives samples Q42 sheet carrier density 9.41×10^{13} and 1.63×10^{13} before fabricate structure water layer. Because DI water treatment act as p-type dopant, the asymmetry in the *I-V* characteristics are attributed to the work-function difference. After graphene sample been water treated, the junction diode is fabricated in clear room to keep graphene samples clear. The 4-points probe measurement is used here

for *I-V* characteristic measurement.

In Fig.47(a), the graphene-graphene junction diode *I-V* curve is being presented, the approximate straight line shows *I-V* liner relationship in junction diode without water layer barrier material that in sharp contrast with water layer barrier. Fig.47(b) is the *I-V* curve from junction diode D with water layer insulator barrier material. This curve is consisting of a forward region and backward region for current measurement. The water treatment work function different because sample Q42 is by water treated doping, water doping make the carrier density changed. The Fig.47(c) is the semi-log plot of junction D, that the dynamic range of current change reached the sixth order of magnitude. Fig.47(d) is the dI/dV plot of this graphene/ water layer /graphene junction diode. The linear relationship near-zero voltage conforms to the DT phenomena, which means this water layer barrier is thin enough for a graphene tunnel junction diode.



(a) (b)

(c) (d)

Fig.47 (a) A four-terminal measurements graph for junction diode D without water layer. The linear *I-V* characteristics indicate this junction an ohmic contact junction. (b) *I-V* characteristic curve of junction diode Dunder different voltages at room temperature. (c) semi-log plot for junction diode D. (d) dI/dV plot of graphene stacked junction diode D.

In the *I-V* curve, the work function of the sample after water treated will be slightly larger than sample without water treated, because the slope of negative region is smaller than that of positive region. In these four stacked graphene junction diodes, the barrier thickness estimated from the FNT equation is larger than the measured thickness of the water layer in Fig. 43(a), which corresponds to a few layers of water molecules [113]. The thickness of water layer before direct bonding was almost constant to be 0.46 nm as shown in Fig.43. After bonding, the thickness of water layer should be not uniform because of the roughness of the sample surface. The electron emission dominantly occurred at the thickness higher barrier region. In this case, the evaluated thickness of structured water layer thickness larger than the average thickness. As shown in *I-V* curve, asymmetric behavior is observed in the *I-V* curve. The cause of this asymmetry can be attributed to the work function difference between samples without water treated and water treated sample. The difference of current in the backward (negativity bias) region and the forward (positive bias) region in *I-V* curve reflects on the difference of slop in FN-plot.

4.2. Theoretical calculations graphene junction diode

4.2.1 Tunneling phenomena of a graphene junction diode

With very thin two-dimensional materials as a barrier in stacked graphene junctions were reported recently, which make it possible to observe Direct tunneling (DT) and Fowler-Nordheim tunneling (FNT) phenomenon. In junction A, both DT and FNT are observed, which means the water layer barrier thickness is very small. Based on the fitting curve of FNT plot, the thickness of the insulator material water layer could be calculated

while work function could calculate from carrier density from Hall effect.

Direct tunneling (DT) phenomena

Direct tunneling refers to no resonant tunneling that occurs when the applied bias is less than the barrier height. In the low-electric-field regime, the carriers in graphene can be transferred to the other graphene sample through the tunneling barrier by DT, which is shown in the schematic of Fig.48 [117-121].

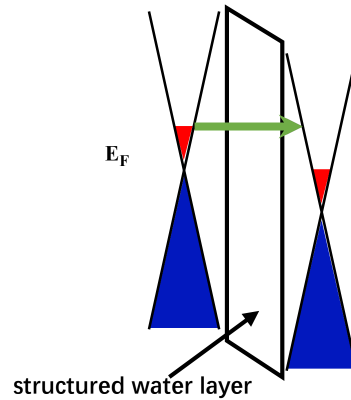


Fig.48 Energy band diagrams of the vertically stacked graphene tunnel junction of Direct tunneling (DT).

In 1963, Simmons presented Current-Voltage Relationship for a Generalized Barrier, provides a simple way to model the current-voltage behavior of a molecular junction is as an arbitrary tunnel barrier within the Simmons approximation [122,123]. We can rewrite this equation as,

$$I_{DT} = \frac{A_{eff} q^2 \sqrt{m_{eff} \Phi_B} V}{d} \exp\left(\frac{-2d\sqrt{m_{eff} \Phi_B}}{\hbar}\right) \quad (2)$$

where d is the barrier width, Φ_B is the work function, ħ is the reduced Planck's constant, A_{eff} is the contact area, q is the electronic charge and m_{eff} is the effective electron mass. In the DT regime, the tunneling current is proportional to the bias voltage, as expressed in the following equation,

$$I \propto V\, exp\left[\frac{-2d\sqrt{2m_e\Phi_B}}{\hbar}\right] \quad (3)$$

As shown in Fig. 44(d), the electrical conductance around zero bias has a constant value that conforms to the *I-V* proportionality relationship in Eq. (3). This result indicates that the structured water layer on graphene is thin enough to observe the DT phenomenon clearly.

Fowler-Nordheim tunneling (FNT) phenomena

For FNT tunneling, when the bias voltage applied to the junction barrier is large, the shape of the barrier-region potential becomes triangular, and the tunneling mechanism changes from DT to FNT, as shown in Fig.49(b) [118-121].

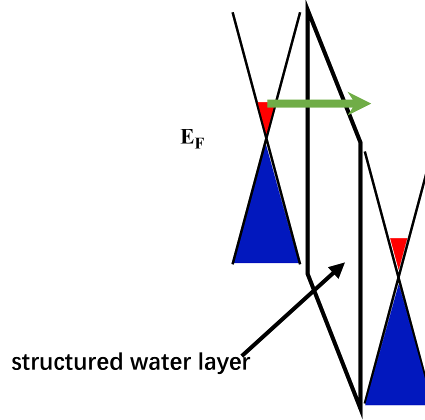


Fig. 49 Energy band diagrams of the vertically stacked graphene tunnel junction of Fowler-Nordheim tunneling (FNT).

On increasing the bias voltage, the tunneling phenomenon changes from DT to FNT. As shown in the FN plot of Fig. 50, linear regions appear at high electric fields for both the negative and positive biased regions. The tunneling current in the FNT regime can be expressed as: [122-126]

$$I_{FNT} = \frac{A_{eff}q^3V^2}{8\pi\Phi_B d^2 m_{eff}} \exp\left(\frac{-4d\sqrt{m_{eff}\Phi_B^3}}{3\hbar qV}\right) \quad (4)$$

The tunneling current in the FNT regime can be expressed as:

$$I \propto V^2\, exp\left[\frac{-4d\sqrt{2m_{eff}\Phi^3}}{3\hbar qV}\right] \quad (5)$$

where d is the barrier width, Φ_B is the work function, ħ is the reduced Planck's constant, A_{eff} is the contact area, q is the electronic charge and m_{eff} is the effective electron mass.

$$ln\left(\frac{1}{V^2}\right) = A - B\frac{1}{V} \quad (6)$$

$$A = \ln\left(1.541433968 \times 10^{-6}\frac{A_{eff}}{m_{eff}\Phi_{BV}d^2}\right) \quad (7)$$

$$B = 6.830887844d\sqrt{m_{eff}\Phi_{BV}^3} \quad (8)$$

It is possible to estimate *d* from the slope of the FN plot, which corresponds to the exponential component of Eq. (4). To evaluate *d*, the work function value Φ_{BV}, and the effective mass of the electron m_{eff} should be assumed. Because the graphene on the SiC substrate is strongly electron-doped, the work function of our graphene sample will be smaller than that of undoped graphene [127]. From equation (4) and (8), we could get the relationship of B, Φ_{BV} and I.

4.2.2 Result analysis of graphene junction diode

In this experiment, both the FNT phenomena and DT phenomena are observed in these stacked graphene junction diodes. Based on the *I-V* characteristic of the graphene junction diode, the FN-polt are given in this part.

Graphene junction diode A consists of graphene sample L19(for water treated) and L20.The fitting equation for is y＝11.85849x-15.81951 and y＝-10.85553x-15.51726, respectively.

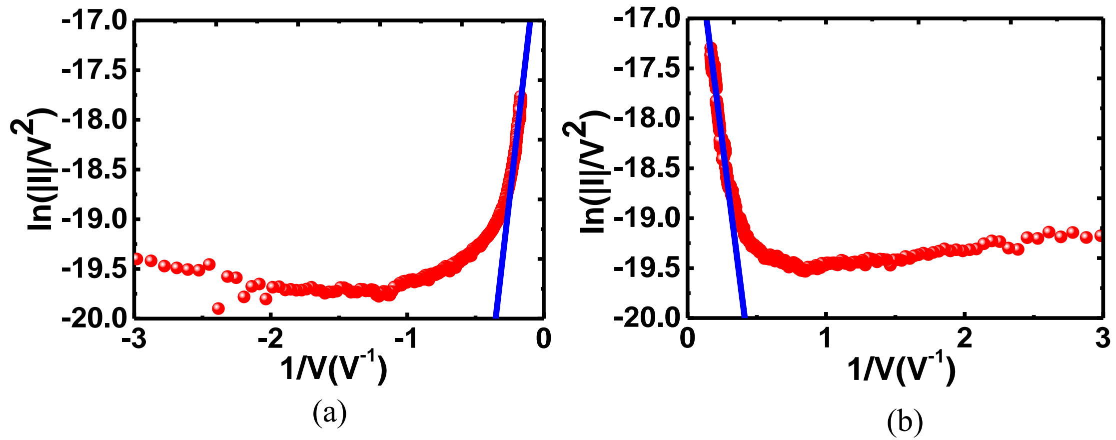


Fig.50 FN-plot of stacked graphene junction diode A (a) negative region FN-plot and fitting linear. (b) positive region FN-plot and fitting linear. Both FNT and DT are observed in these FN plots.

For stacked junction diode B, consist of graphene sample P33 and P34 (water treated) the fitting equations are y = 12.39x - 11.553 and y = -12.353x - 11.131.

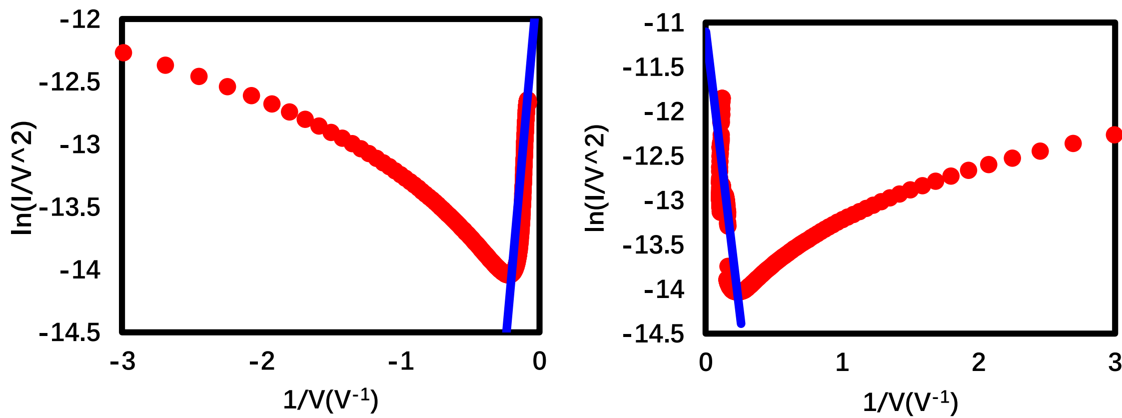


Fig. 51 FN plot of graphene stacked junction diode C with a fitting line. (a) negative region FN-plot and fitting linear. (b) positive region FN-plot and fitting linear for FN plot. Both FNT and DT are observed in these FN plots.

For graphene stacked junction diode C consists of sample P19(water treated) and P31. In Fig. 52 both FNT and DT are observed which means the water layer barrier is a very thin insulator material for this tunnel junction. The fitting equations of FN-polt are y = 8.3295x-12.579 and y = -7.8557x-12.681.

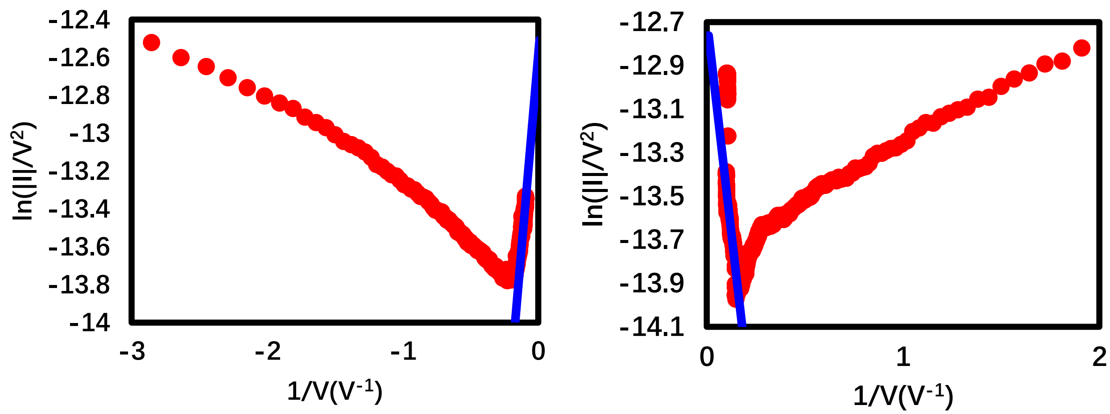


Fig. 52 FN-plot of graphene stacked junction diode C from *I-V* curve. (a) negative region FN-plot and fitting linear. (b) positive region FN-plot and fitting linear for FN plot. Both FNT and DT are observed in these FN plots.

For junction diode D, form fitting curve of FN-plot in Fig.53, the fitting equation are y =21.267x-12.165 and y = -20.962x-11.16, graphene junction diode consists of Q42(water treated) and M18.

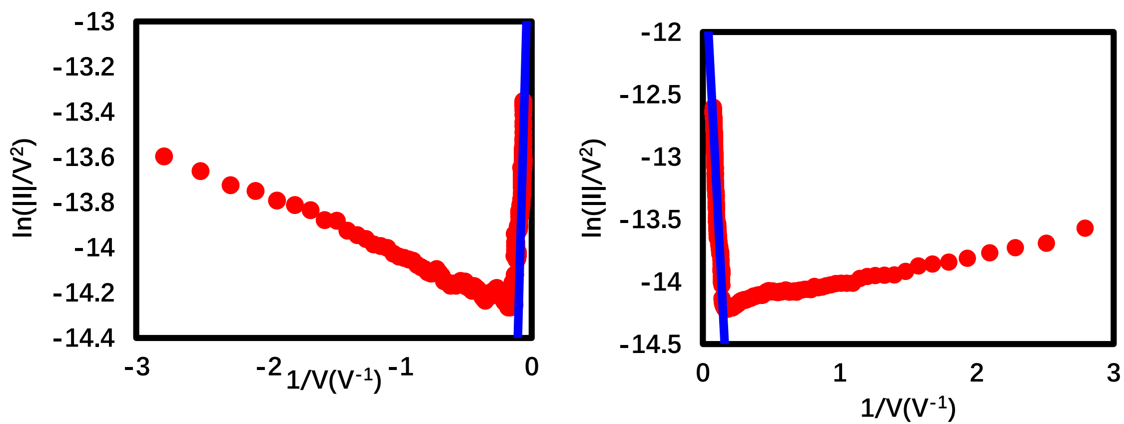


Fig.53 FN-plot of graphene junction diode D from *I-V* curve (a) negative region FN-plot and fitting linear. (b) positive region FN-plot and fitting linear for FN plot. Both FNT and DT are observed in these FN plots.

4.3 Discussion

From the equation (6)~(8) and fitting equation of FNT plot, unknown parameter water layer thickness d could be calculated which required work function value Φ_{BV}, effective electron mass m_{eff} and fitting value B in Eq.(8).

The Fermi level shift, ΔE_F can be expressed by the following equation [128,129].

$$\Delta E_F = \hbar \nu_F \sqrt{\pi n} \qquad (9)$$

The effective electron mass can be expressed by the following equation [130]:

$$m_c = E_F/{\nu_F}^2 = \sqrt{\pi \hbar^2 n/{\nu_F}^2} \quad (10)$$

where n is the carrier density of graphene, m_c is effective carrier mass and ν_F is the Fermi velocity, which is approximately 1.1×10^8 cm/s[131]. Through Eq. (10) with carrier density measurement from Hall effect, effective electron mass $m_{eff}(=\frac{m_c}{m_e})$ could calculate. In tissue thesis, the graphene samples for experiment is shown in Table 1.

	L19	L20	P33	P34
Sheet Resistance(Ω/□)	1.59×10^3	2.36×10^3	4.55×10^2	5.6×10^2
Carrier mobility(cm^2/Vs)	744	479	966	929
Sheet carrier density(cm^{-2})	5.48×10^{12}	6.04×10^{12}	1.58×10^{13}	1.20×10^{13}
	P19	P31	M18	Q42
Sheet Resistance(Ω/□)	5.1×10^2	1.27×10^3	9.36×10^2	3.59×10^2
Carrier mobility(cm^2/Vs)	1020	1248	417	575
Sheet carrier density(cm^{-2})	1.21×10^{13}	3.99×10^{12}	1.63×10^{13}	9.41×10^{13}
	Q62	Q63	Q67	M19
Sheet Resistance(Ω/□)	1.82×10^3	2.53×10^2	3.08×10^2	7.73×10^3
Carrier mobility(cm^2/Vs)	513	1934	1656	468
Sheet carrier density(cm^{-2})	6.97×10^{12}	1.56×10^{13}	1.23×10^{13}	7.61×10^{12}

Table 1. The Hall effect measurement result of graphene samples that been used for graphene junction diodes.

In the last part, for graphene sample without water treated the work function could calculate with Eq. (9) by assuming the work function of pristine graphene to be 4.56 eV [127]. Through Eq. (9) and graphene carrier density from Hall effect, the work function for graphene samples without water treated could calculate in Table 2 and 3. The effective electron mass m_{eff} could be calculated based on carrier density and Eq.(10).When Φ_B is calculated from carrier density, the thickness d could obtained with m_{eff}.

Forward positive region	Junction diode A	Junction diode B	Junction diode C	Junction diode D
B	10.85553	12.353	7.8557	11.787
Sample No.	L20	P33	P31	M18
carrier density (Hall effect)	6.03951E+12	1.53943E+13	3.88058E+12	1.63E+13
ΦB	4.245	4.057	4.3	4.04
meff(calculation)	0.045842726	0.073189522	0.036746647	0.075312
meff	1	1	1	1
d	0.181701007	0.221303241	0.128974856	0.212498
meff	0.42	0.42	0.42	0.42
d	0.280370741	0.341478315	0.199012523	0.327891
meff	0.064	0.064	0.064	0.064
d	0.718236296	0.874777871	0.509817882	0.839970617

Table.2. The parameter for Forward positive region with different graphene junction diodes

Forward negative region	Junction diode A	Junction diode B	Junction diode C	Junction diode D
B	11.85849	12.39	7.7801	9.6303
Sample No.	L19	P34	P19	Q42
carrier density (Hall effect)	5.4805E+12	1.17028E+13	1.17E+13	9.41E+13
ΦB	4.53645437	4.065097043	4.471204	3.53
Carrier density (calculation)	3.37E+10	1.49E+13	4.79E+11	6.44E+13
meff(calculation)	0.003422513	0.07193742	0.012907	0.149717
meff	1	1	1	1

d	0.179670765	0.221303241	0.120468	0.212569
meff	0.42	0.42	0.42	0.42
d	0.277238009	0.341478315	0.185886	0.328002
meff	0.064	0.064	0.064	0.064
d	0.710211057	0.874777871	0.476191141	0.840254054

Table.3 The parameter for Forward negative region with different graphene junction diodes

In Table .3, these four graphene samples are water treated. Because water layer acted as a p-type dopant [132] that lead carrier density changed in carrier density (calculation). In tunneling barrier thickness d calculation, we choose three m_{eff} values as candidates. The ratio of effective mass m_e/m_0 under vacuum is 1, m_{eff} of typical insulator material Si to be 0.42 [133]., value 0.064 is based on graphene sample annealed carrier density calculation with Eq. (10). Consider with single water layer thickness larger than 0.25nm [134], tunneling barrier thickness of junction diode A, B, C, D are about 0.71nm, 0.87nm, 0.48nm, 0.84nm, respectively. Compare with h-BN layer (around 2–7atomic layers) barrier with 1 THz photon irradiation reported from Deepika Yadav et.al in 2016[113] and tens of nanometers thick h-BN barrier reported from L. Britnell et al. in 2013[90]. Our water layer barrier is thinner than these two reported barrier material, which could have large current for junction diode from FNT equation. In Deepika Yadav et.al research, a THz emitting graphene field-effect transistors with $7pW\mu m^{-2}$ output power is reported and active area of the device to be around 1.4–1.5 μm wide as shown in Fig.35. Consider about thinner barrier material offer large current for junction diode, we speculate this thin water layer barrier graphene stacked junction diode could have higher output power than $7p\ W\mu m^{-2}$. For measurement graphene junction diode power, in future research an infrared thermometer could use for measurement temperature to calculate tunnel junction power.

In this chapter, graphene /water structure /graphene junction diode is introducing from fabrication and *I-V* characteristic analysis. For fabrication, the acrylic molds designed for two graphene samples direct bonding with structure water layer been sandwiched between graphene samples. A 4-points measurement is used for *I-V*

characteristic of this tunnel junction, to realize require of steadily contact with graphene surface scalable probe is design for these junction diodes. The *I-V* curve of graphene/ structure water/graphene junction diode observed a typically nonlinear curve compare with without structure water layer *I-V* characteristic of linear. The asymmetric of *I-V* curve because of different work function of two graphene samples, which cause of water treated lead graphene effect of n-type dopant. The work function and effective electronic mass could calculate from carrier density, that leads water layer thickness also could have obtained. From the *I-V* curve, semi-log plot and di/dv are given for junction diode analysis. The linear relationship in dI/dV plot accord with *I-V* linear characteristic in DT equation, which proved this junction is tunneling junction.

5. Conclusion and future works

In this graphene stacked junction diode thesis, the first two chapters were introducing graphene electronic principles, application and Terahertz technology. Graphene has a widely application on electronic devices for new generation heterostructure such as FET, 2D material vertically stacked junctions and sensors. From chapter 3, graphene epitaxial growth and characterization method were explained which is the basic of graphene experiment. Characterization method is an important method for us to understand the condition of the graphene sample, SPM and Raman were help us see graphene surface directly. The junction diode design and fabrication, *I-V* characteristics, calculation of water layer thickness, contact area also been introduced in chapter 4 and chapter 5. Though measurement the power of graphene tunnel junction, the frequency of infrared from temperature increase could obtained which can prove this junction diode for terahertz emission. And the parameters like water layer thickness were also been offered by calculated.

This work presents the first ever observation of the tunneling phenomenon through a water barrier in stacked graphene junctions, which is significant for applications in resonant tunneling and terahertz emission. We successfully obtained four graphenes stacked junction diodes with very thin structured water layer (<1nm), this thickness is much smaller than some reported devices, which make us believers this water layer junction diode structure will have larger current and output power.

For future work, by comparing the barrier material thickness, we speculate graphene stacked junction diode with water layer barrier have a large power than some reported THz emission devices. In order to validate our speculation, the power measurement of this graphene junction diode is necessary. An infrared thermometer was introducing for power measurement, which will not damage of junction diode.

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Conference

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