Research on Interface State and Reliability of 4H-SiC MOSFETs with Thermal Gate Oxide

A dissertation submitted to
Tokushima University
in partial fulfillment of the requirements
for the degree of
Doctor of Philosophy

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September 2020

ABSTRACT

Silicon carbide (SiC) is a kind of IV–IV compound material with a wide bandgap and high critical (breakdown) electric field strength. The strong chemical bonding between Si and C atoms gives this material high hardness, chemical inertness, and high thermal conductivity. The ability of SiC to form silicon dioxide (SiO_2) as a native oxide is another important advantage for device fabrication. As a result of these properties, SiC has been developed as power metal–oxide–semiconductor field-effect transistors (MOSFETs) for high-power and high temperature electronics.

In a Si power MOSFET, the resistance of the drift layer cannot be neglected, but in a SiC power MOSFET, the drift layer resistance is nearly 100 times lower than that of a Si power MOSFET with the same blocking voltage, such as 1200 V. However, the channel resistance and the drift layer resistance are dominant factors in a SiC MOSFET when the blocking voltage is increased to 2–3 kV. When the blocking voltage is above 3 kV, the drift layer resistance of the SiC MOSFET becomes dominated, compared with that of a 600–1200 V Si power MOSFET. In addition, SiO_2 films can be directly grown on SiC substrates by conventional thermal oxidation, which is one of the advantages of SiC over other wide-gap semiconductors in device fabrication. Thermal oxidation of SiC has been believed to induce considerable interface defects at the SiO_2/SiC and near-interface traps. The interface defects not only reduce the channel mobility of SiC MOSFETs but also decrease the performance reliability.

According to the oxidation mechanism, it has been found that the oxidation reaction energy at the interface of SiO_2/SiC (3.12 eV) is larger than that at the interface of SiO_2/Si (1.23 eV). It is widely accepted that the oxidation temperature affects the oxidation rate. With an increase of the temperature, the interface reaction rate significantly increases while the diffusion rate decreases. For this problem, we confirmed that the optimal D_{it} was obtained for the sample oxidized at 1450^{o}C in the energy range 0.2–0.6 eV below the conduction band edge of SiC. However, there was a trade-off between D_{it} and reliability, the sample oxidized at 1250^{o}C showed the most reliable character of those tested. To ease the tradeoff between interface state and reliability, Argon (Ar) and Nitric oxide (NO) post oxidation anneal (POA) was research. During the further results, we found that the reduction of D_{it} is mainly attributing to NO annealing and higher temperature. However, due to the

introduction of N positive charge, the flat band voltage of the SiC-MOS capacitor devices drifts in the negative direction, which will form normally on SiC-MOSFETs. On the other hands, even though Ar annealing can keep the flat band voltage comparing with the as grown one, but it is proof to weekly improve the quality of oxide layer near the SiO_2/SiC interface and enhance the effect of NO annealing.

We also revealed that the interface state density near the conductance band reduces significantly when the annealing temperature reaches to 1300^{o}C or the annealing time extends to 120 min by further experiments. It is suggested that the interface state density reduces when the POA temperature was elevated or the POA time was extended. We also worked that the effects of NO annealing temperature and time on the reliability of 4H-SiC MOS gate oxide. And from the results of field-to-breakdown (E_{BD}) and charge-to-breakdown (Q_{BD}), find it is effectively improving the insulation properties and reliability of gate oxide by high temperature NO annealing.

Related studies have shown that controlling the macro stress of SiC materials and the local stress generated by defects is benefit on improving the interface characteristics of SiC devices, indicating that the mechanism of the thermal oxide reliability of SiC MOS devices revealed by stress research is necessary. Recently, research already has gradually focused on the process to the SiC material itself. It is expected to improve the interface problems of SiC MOS devices. In this paper, by commercial silicon carbide epitaxial material, the defects on the interface state and reliability of the gate oxide film are investigated. The effect of grinding-induced stress on interface state density of SiC/SiO_2 was investigated and also calculated by first-principle calculations, and the energy levels (E_0) of the samples related to the lattice constants of the SiC crystal, indicating that stress mainly affected the SiO_2/SiC interface. Furthermore, we studied the excessive compressive/tensile curvature, induced by stress/strain, decreased reliability of SiO_2 films, expressed by E_{BD} and Q_{BD} during dry thermal oxidation processes. We suggest that a “stress free” oxide film might be the best choice for SiC-MOSFET applications. These results will be useful for industrial applications of SiC and SiC-based devices and practical epitaxy wafer selection.

Keywords: 4H-SiC, Interface state, Reliability, MOSFETs, Thermal gate oxide.

CONTENTS

Chapter 1: Introduction

§1.1 Features of SiC MOSFET

In recent years, environmental issues and energy conservation and emission reduction issues have become increasingly prominent, and energy conservation, environmental protection and low-carbon development have gradually become a global consensus. Electric energy as the ultimate form of energy has been incorporated into people's daily life in large quantities. Increasing the utilization rate of electrical energy has become the most obvious method in energy saving, emission reduction and environmental protection, and reducing the energy consumption of core power electronic devices has become an urgent problem to be solved. Silicon carbide (SiC) material is one of the wide band gap semiconductor materials after Silicon (Si) and Gallium arsenide (GaAs) material, which is extremely superior Physical and chemical properties. In recent years, SiC power electronic devices have attracted much attention in the fields of wind power generation, new energy vehicles, motor drives, rail transit, wind power generation, etc. As shown in Figure 1-1, SiC power electronic devices are particularly used in high-voltage and high-power applications. It is expected to replace traditional Si-based power electronic devices to achieve high efficiency, energy saving and environmental protection, miniaturization and light weight of power conversion systems [1].

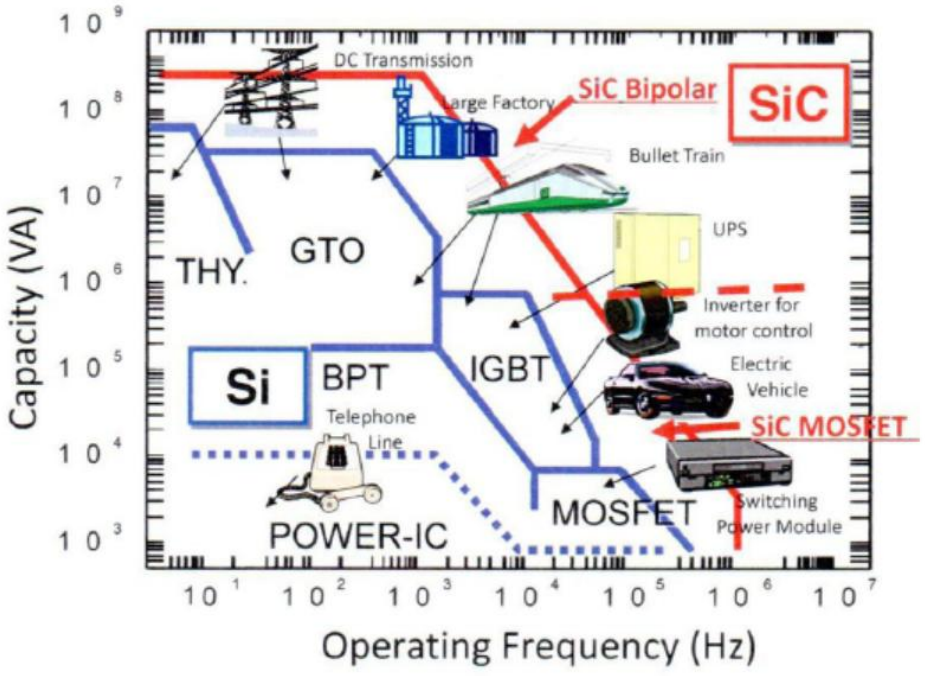


Figure 1-1. Excellent performance and application prospects of SiC power electronic devices

Table I-I shows the electrical properties of 4H-SiC materials compared with other materials. Compared with traditional Si materials, SiC has a wider band gap (3.26eV), higher thermal conductivity and greater the critical breakdown field strength. It has received extensive attention in high-power switching circuits and power system applications. In the field of high-voltage and high-power applications, the main goal of device design is to increase the break down voltage while reducing the forward resistance of the device as much as possible. Compared with Si materials, the critical breakdown electric field of SiC is increased to about 10 times. Therefore, in the case of the same doping concentration, the withstand voltage of the device can theoretically be improved by nearly 100 times [1]. And because of its higher thermal conductivity, carrier saturation rate and lower intrinsic carrier concentration, it has obvious advantages in the field of high temperature and high frequency application. The most outstanding performance advantages of SiC power electronic devices are its high voltage, large current, high frequency and high temperature operating characteristics, which can effectively reduce the power loss of power electronic systems.

Table I-I. Physical properties of various semiconductor materials

	Si	4H-SiC	GaN
Bandgap (eV)	**1.1**	**3.26**	**3.39**
Electron mobility ($cm^2/v \cdot s$)	1350	1000	1200
Critical electric field (MV/cm)	0.3	2.8	3
Thermal conductivity (W/cm・k)	**1.5**	**4.9**	**1.3**
Hetero junction	**Δ**	×	○

Silicon carbide (SiC) is a kind of IV–IV compound material with a wide bandgap and high critical (breakdown) electric field strength. The strong chemical bonding between Si and C atoms gives this material high hardness, chemical inertness, and high thermal conductivity. The ability of SiC to form silicon dioxide (SiO_2) as a native oxide is another

important advantage for device fabrication. As a result of these properties, SiC has been developed as power metal–oxide–semiconductor field-effect transistors (MOSFETs) for high-power and high temperature electronics.

Recently, most of the leading semiconductor device manufacturers in the industry in the world have made tremendous progress on the SiC-MOSFETs devices [2], as shown in Figure 1-2. At this stage, the vast majority of commercial SiC MOSFET products are designed with N-channel planar vertical structure, and many companies have launched a new generation of SiC MOSFET products. However, our actual dynamic and static temperature characteristic tests and a series of reliability test results show that the threshold voltage of SiC-MOSFET devices is less than the threshold voltage of traditional Si devices (3–5 V) due to the immature gate oxide manufacturing process and reliability design. When the SiC-MOSFET device is tested at high temperature (150^{o}C), the threshold voltage drops to close to 1 V. Also, when a negative voltage is applied, the threshold voltage will also drift in the negative direction. This makes the threshold voltage of the SiC-MOSFET device may be less than zero volts in extreme cases, and unexpected accidents may occur during the actual circuit control process.

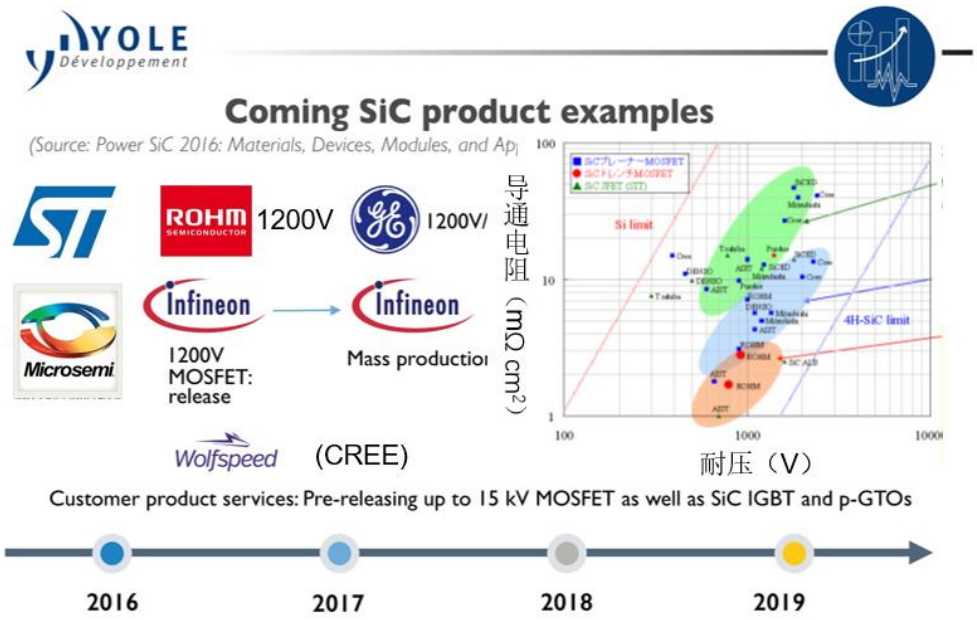


Figure 1-2. Global mainstream electronic device manufacturing SiC related product roadmap products

Compared with other wide band gap semiconductor materials such as gallium nitride (GaN), SiC materials are more widely used in SiC-MOSFET devices in the field of power

devices because of their properties that can be directly oxidized to SiO_2. However, compared with traditional Si materials, due to the additional presence of carbon, the SiC thermal oxidation process is very complicated. In the oxidation process, it is considered that Si and C are discharged into the oxide, resulting in a reduction in the interface reaction rate. Considering the Si and C atoms emitted from the interface and the oxidation process of C during the oxidation process, the oxidation reaction of SiC can be summarized as the processes of internal oxidation, surface oxidation, and element diffusion, as shown in Figure 1-3. [3]

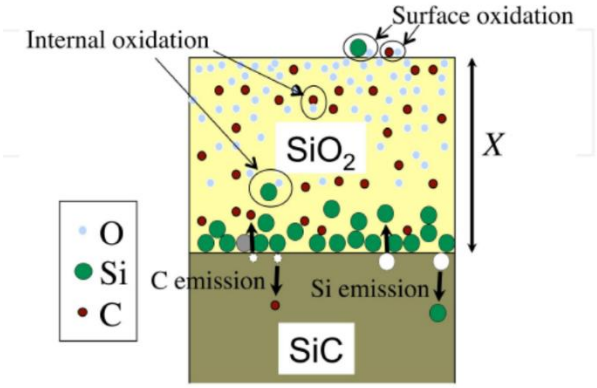


Figure 1-3. Schematic diagram of high temperature oxidation interface reaction [3]

The reaction equation of SiC oxidation can be written as:

$$SiC+(2-\nu_{Si}-\nu_C-\alpha/2)O_2\rightarrow(1-\nu_{Si})SiO_2+\nu_{Si}Si+\nu_C C+\alpha CO+(1-\nu_C-\alpha)CO_2 \quad (1\text{-}1)$$

Where α is the rate of CO production.

MOSFETs with a vertical structure can be divided into trench MOSFETs or planar MOSFETs. In conjunction with the development of high-voltage SiC diodes, the fabrication of vertical SiC switching devices began in the early 1990s. In 1993, a vertical 4H-SiC trench MOSFET was demonstrated by Palmour and co-workers as an important step towards high-power electronics. In 1997, the first planar double-implanted MOSFET using SiC with a blocking voltage of 760 V and a low on-resistance was reported by Cooper and co-workers. To avoid problems at the SiC MOS interface, especially in a high temperature application, a vertical junction FET (JFET) was developed, which led to the commercialization of SiC power JFETs in 2006. However, further improvement of the SiC MOSFET is required in terms of the high frequency switching performance and on-resistance reduction.

The on-resistance of a power MOSFET is naturally composed of source resistance, channel resistance, drift layer resistance, and substrate resistance in series. In a Si power MOSFET, the resistance of the drift layer cannot be neglected, but in a SiC power MOSFET, the drift layer resistance is nearly 100 times lower than that of a Si power MOSFET with the same blocking voltage, such as 1200 V. However, the channel resistance and the drift layer resistance are dominant factors in a SiC MOSFET when the blocking voltage is increased to 2–3 kV. When the blocking voltage is above 3 kV, the drift layer resistance of the SiC MOSFET becomes dominated, compared with that of a 600–1200 V Si power MOSFET.

Low channel mobility can limit the performance of a SiC MOSFET, which results in high channel resistance. To improve the channel resistance, the following methods have been used:

(i) Decrease the cell pitch

(ii) Reduce channel length

(iii) Enhance channel mobility.

Decreasing the cell pitch is an effective way to increase the current density, whereas the drift layer resistance increases as the spacing between p-wells becomes smaller. Shortening the channel length may reduce the on-resistance; however, one must be vigilant of the short-channel effect. In conclusion, the enhancement of the channel mobility by decreasing the interface state density of SiO_2/SiC is efficient, and will be described in the next subsection.

§1.2 Interface State Density, Reliability and the Flat-band Voltage

Silicon carbide (SiC) has been commercially accepted as an alternative semiconductor for high-voltage power and high energy-efficiency power MOS devices owing to its attractive properties, such as high breakdown field and high thermal conductivity. In addition, SiO_2 films can be directly grown on SiC substrates by conventional thermal oxidation, which is one of the advantages of SiC over other wide-gap semiconductors in device fabrication. Thermal oxidation of SiC has been believed to induce considerable interface defects at the SiO_2/SiC and near-interface traps. The interface defects not only reduce the channel mobility of SiC MOSFETs but also decrease the performance reliability.

According to the oxidation mechanism, it has been found that the oxidation reaction energy at the interface of SiO_2/SiC (3.12 eV) is larger than that at the interface of SiO_2/Si (1.23 eV). It is widely accepted that the oxidation temperature affects the oxidation rate. With an increase of the temperature, the interface reaction rate significantly increases while the diffusion rate decreases. Recently, we reported that a larger oxide thickness results in an increase in the total number of electron traps for the dry oxidation at a temperature ranging from 1200 to 1350^{o}C on 4H-SiC (0001). We found that a higher oxidation temperature leads to a much lower interface density by enhancing the CO ejection, which agreed well with Hijikata's results. However, nitrogen release might also be dominant at higher temperature, which could produce more nitrogen ions to decrease the interface density and the number of oxidation electron traps, which will be the focus of this study.

For the reduction of the effects of interface defects, various passivation techniques have been extensively investigated, such as annealing in ambient nitrous oxide (N_2O), ammonia (NH_3), or nitric oxide (NO). Post-oxide-annealing (POA) in NO is regarded as the most promising method to improve the interface quality, because it is able to effectively increase the channel mobility of SiC MOS and reduce the interface state density at the 4H-SiC/SiO_2 interface. However, it is unclear how the interface defects are reduced by nitridation. To determine the mechanism for the further reduction of the density of interface states (D_{it}) after NO POA, we consider that it is crucial to employ NO POA conditions suitable for the elimination of carbon precipitation or active oxidation at the interface because they are the most possible origins of these defects. However, in contrast with the Si/SiO_2 interface, the 4H-SiC/SiO_2 interface features a high D_{it} of 10^{13} $cm^{-2} \cdot eV^{-1}$, evaluated based on the differences between quasi-static and theoretical capacitances (C-ψ_s method) near the 4H-SiC conduction band, which limits the inversion channel mobility of 4H-SiC MOSFETs, as well as the reliability.

Unfortunately, the annealing of NO introduced the N element at the interface. Because it releases electrons, it is positively charged. In MOS devices, the flat band voltage of the capacitor is caused to drift in the negative direction. This causes the threshold voltage of the prepared MOSFET device to be negative, forming a normally-on transistor.

§1.3 Facing Challenges

Silicon carbide is a promising wide bandgap semiconductor material for high-voltage and low-loss power devices. The production of SiC SBD and power MOSFETs has commercial appeal. However, more information on the physical properties of SiC defects and devices needs to be obtained.

During oxidation process, it will be different due to the difference in oxidation temperature and oxygen partial pressure, as shown in Figure 1-4. The reaction at the SiC/SiO_2 interface is mainly divided into three stages. The most ideal area is the area where only silicon dioxide is produced after oxidation is the area of Region 2. In this interval, the oxidation temperature and oxygen partial pressure must be strictly controlled, but during the oxidation process, there are many uncertain factors, and it is difficult to control the oxidation conditions. When the oxidation temperature is too low and the oxidation is insufficient, it is easy to leave the C element at the interface (Region 3), which affects the quality of the gate oxygen and increases the interface state density. When the oxidation temperature is too high or the oxygen partial pressure is low, although the C element and the oxygen element generate CO and escape the oxide layer, at the same time, the Si element and the O element cannot generate a tight oxide and generate silicon monoxide, making the interface Oxygen vacancies (Region 1) are generated at the site, affecting the quality of the gate oxide layer [4].

Region 1：$SiC+O_2 \rightarrow SiO(g)+CO(g)\uparrow$；

Region 2：$SiC+3/2O_2 \rightarrow SiO_2+CO(g)\uparrow$；

Region 3：$SiC+O_2 \rightarrow SiO_2+C(S)$；

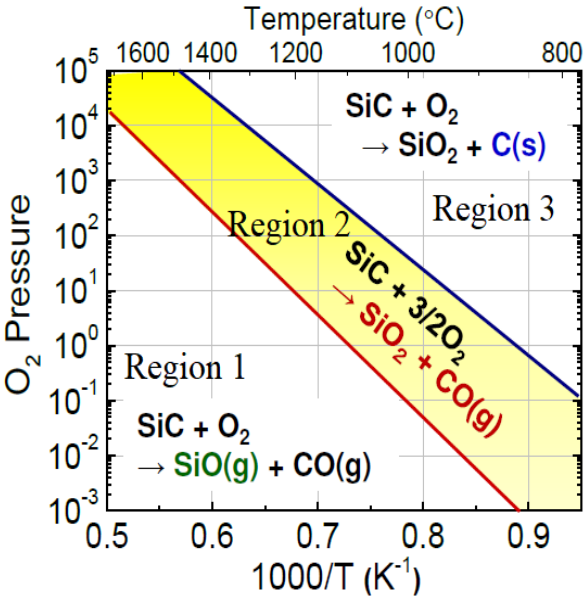


Figure 1-4. The relationship between SiC oxidation temperature and oxygen partial pressure [4]

The current mainstream process is post-oxidation annealing in atmospheres containing nitrogen gas such as NO, nitrous oxide (N_2O) or ammonia (NH_3). Some papers have proposed to use N_2O or direct oxidation in NO, but little improvement effect on the interface. At present, the interface nitriding technology of NO or N_2O is widely used in academic research and mass production of SiC power MOSFETs. However, the experimental results show that high density fast interface states are generated near the edges of the conduction band by nitriding annealing [5-6]. Although the density of slow interface states is significantly reduced by nitridation, the gate oxygen reliability problem is not significantly improved. The electrical characteristics of SiC MOSFET devices show that the reliability problems of SiC devices (high temperature operation, threshold voltage and high mobility, etc.) and the mechanism for these reliability problems have not been solved.

Recently, research already has gradually focused on the process to the SiC material itself. It is expected to improve the interface problems of SiC MOS devices. Related studies have shown that controlling the macro stress of SiC materials and the local stress generated by defects is benefit on improving the interface characteristics of SiC devices, indicating that the mechanism of the thermal oxide reliability of SiC MOS devices revealed by stress research is necessary.

To study the influence of stress on the reliability of the gate oxygen, we should proceed from the characteristics of the SiC material and the atomic layer structure of the SiC material. Figure 1-5 explains the typical characteristics of the wave function of the bottom of SiC conduction band. According to a recent first-principles report, the wave function of the conductive bottom of SiC is almost similar to that of nearly free electrons (NFE). The amplitude of the wave function of SiC conduction band is not on the atom, but is distributed between the SiC atoms like a free electron wave function in the internal space [5].

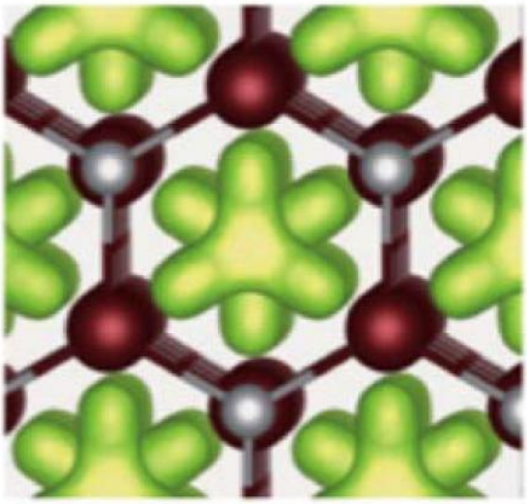


Figure 1-5. Wave function at the bottom of SiC conduction band [5]

As a special compound material with equal number of Si atoms and C atoms, SiC material is a typical homogeneous polymorphic material. It has been proved that there are more than two hundred and fifty allotrope materials. In the case of the same stoichiometric composition, SiC materials have different crystal structures, such as sphalerite structure, quartzite structure and rhombic structure, using C (cube crystal system: Cubic), H (hexagonal crystal system: Hexagonal), R (diamond hexagonal crystal system: Rhombohedra) represents respectively [2]. The number of Si-C layers in each stacking cycle indicating the direction of close packing can be used to accurately express a polytype, such as 3C (ABC), 4H (ABAC), 6H (ABCACB), etc., Figure 1-6 shows the atomic arrangement of several polytype structures [6].

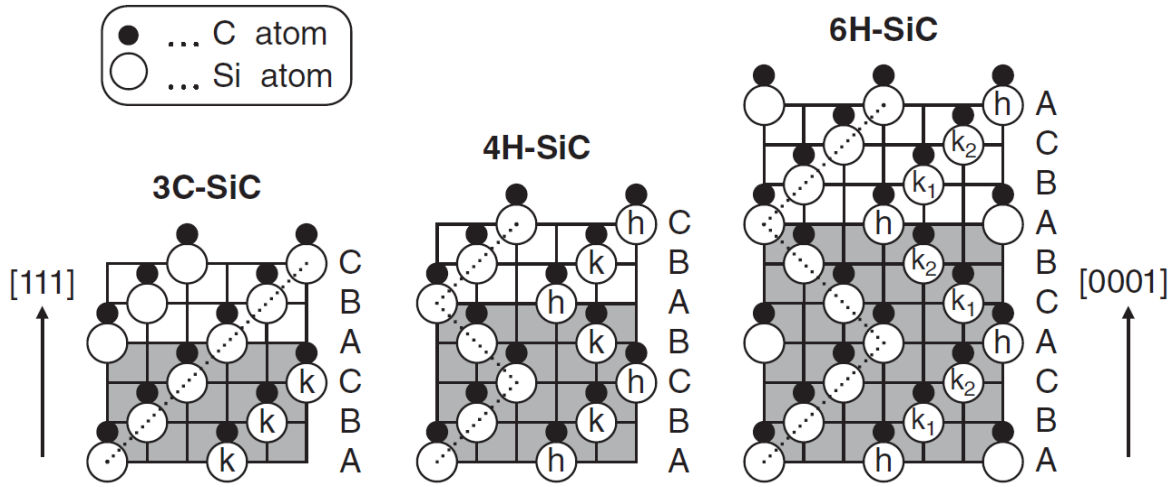


Figure 1-6. Common atomic arrangement of allotropes in SiC [1]

Depending on the arrangement of atoms, the band gap of SiC materials is also very different. This is because the state of the SiC conduction band with NFE characteristics is extremely sensitive to the shape change of the internal space, and the shape of the internal space depends on the SiC polytype. Figure 1-7 is a schematic diagram of the shape of the internal space of different SiC materials and the width of the band gap [5]. The shape of the internal space of 3C-SiC is straight and its length is infinite, but the shape of the internal space of 4H, 2H, 6H-SiC is Jagged. Therefore, the quantum confinement effect in 3C-SiC is inherently weak, resulting in a relatively low energy level of the NFE state and a small band gap [2]. However, in 4H-SiC, 6H-SiC or 2H-SiC, it is located inside the zigzag. The quantum confinement effect of the NFE state in space should become very large, which increases the energy level of the NFE state. Interface defects, stress and roughness will affect the NFE state, resulting in local changes in the conduction band energy, which will reduce the performance of the MOSFET, such as mobility.

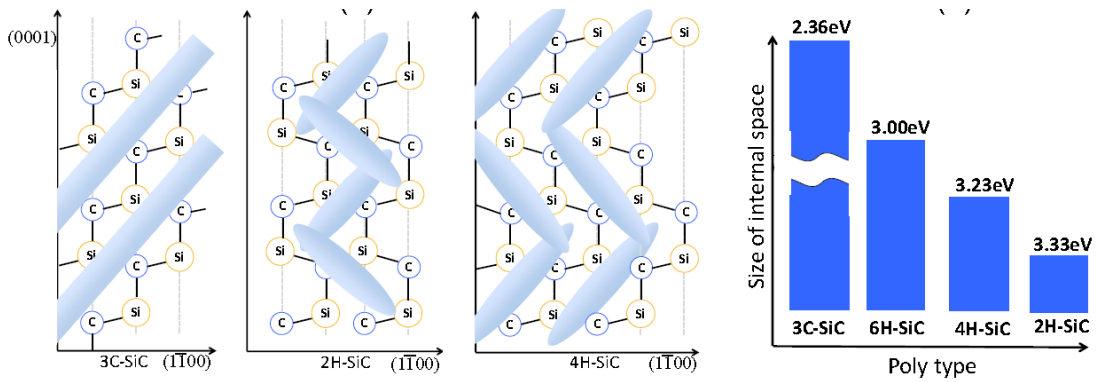


Figure 1-7. Schematic diagrams of the internal space shape of different SiC materials and the width of the band gap [5]

This can be seen from Figure 1-8, which is a schematic diagram of the energy bands of Si and SiC materials. Figure 1-8 (a) shows that Si is a typical covalently bonded semiconductor and the energy band of SiC is from the NFE state determine the band gap [4,5].

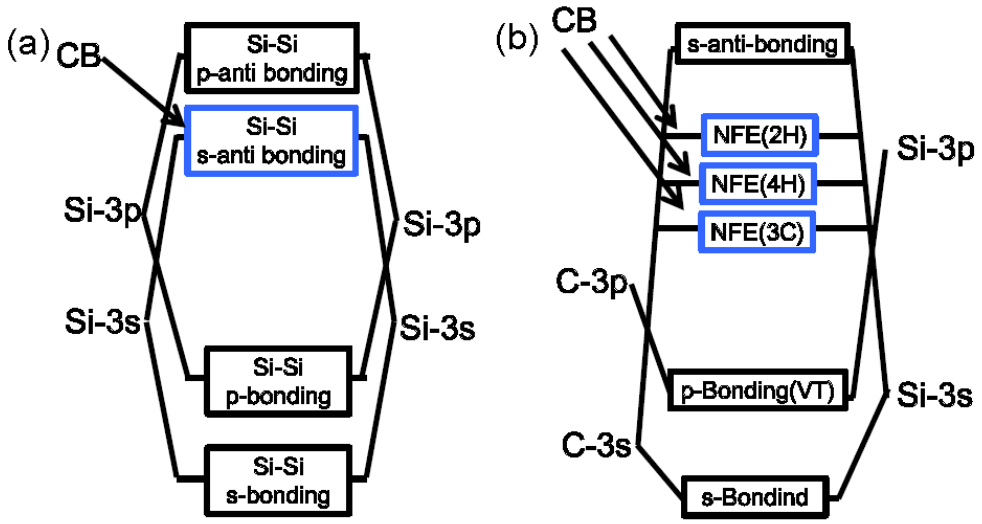
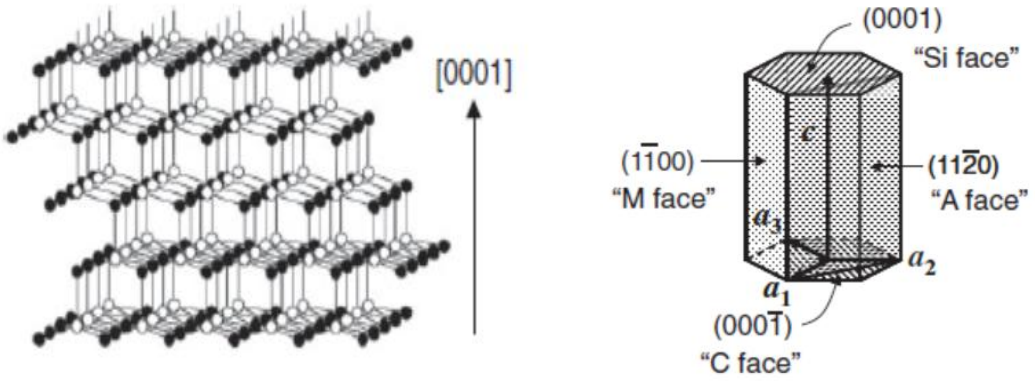


Figure 1-8. (a) Si (typical covalent bond semiconductor) (b) SiC (NFE state band gap) band diagram [5]

Among several common allotropic SiC materials in SiC, the currently commercialized SiC devices are mainly based on the growth of 4H-SiC epitaxial materials. This is due to the electrons of 4H-SiC materials compared to other structures of SiC materials, the mobility is high, the anisotropy is small, and the substrate material has good stability. The 3-D lattice structure of 4H-SiC is shown in Figure 1-9 (a). In the Si-C diatomic layer, Si atoms are light-colored atoms, C atoms are dark atoms, and the crystal surface is completely covered by the Si atom layer, called the silicon surface <0001>, the carbon surface is covered by the C atomic layer $<000\bar{1}>$ (C-face), and another frequently used crystal surface is the $<11\bar{2}0>$ surface (a-face). The hexagonal structure of 4H-SiC is shown in Figure 1-9 (b) [7]. 4H-SiC epitaxial material was mainly used in the research process of this project, and the experiment was carried out based on 4H-SiC <0001>.



（a）　　（b）

Figure 1-9. (a) 3-D lattice structure (b) schematic diagram of hexagonal structure of 4H-SiC [1]

The schematic diagram of the shape of the internal space and the state of the wave function space of 4H-SiC material are shown in Figure 1-10. The study of the wave function is an indispensable research content for studying stress [5, 8].

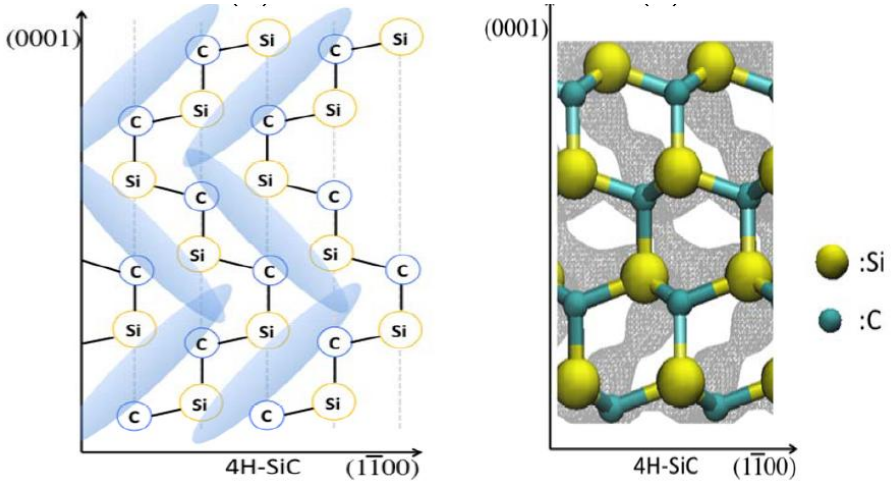


Figure 1-10. Schematic diagram of internal state space and wave function space state of 4H-SiC [5]

Recently, a few teams are studying this theme, but the related mechanism has not been revealed, such as University of Tokyo, Tohoku University, and Nagoya University. They have begun to study the relationship between stress and the interface characteristics of SiC MOS devices. Professor K. Shiraishi of Nagoya University proposed that the V_{th} instability of SiC MOS devices caused by stress changes caused by proton mobile ions Mechanism. Professor T. Kimoto suggested that the damage layer should be completely removed before

the CMP process. Because the damage layer has very large stress, it is composed of high-density lattice defects and deep-propagated micro-cracks, which play a key role in device reliability issues, the study of stress can guide us to control and select the epitaxial wafer and wafer curvature [6, 8].

§1.4 References

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Chapter 2: Influence of Oxidation Temperature and Atmosphere on the SiO_2/SiC Interface State and Reliability

§ 2.1 Ultrahigh-temperature Oxidation of 4H-SiC (0001) and Gate Oxide Reliability Dependence on Oxidation Temperature

The paper confirmed the SiC/SiO_2 interface state density obtained from the ultrahigh-temperature dry oxidation process on 4H-SiC Si-face (0001) at up to 1550^{o}C without any other passivating techniques. Our results were consistent with those of previous reports. Furthermore, we also considered the reliability of SiO_2, which is important for its practical application, by time-dependent dielectric breakdown measurements (TDDB). The optimal interface state density was obtained for the gate oxide formed at 1450^{o}C at E_C-E=0.2~0.6 eV, whereas the gate oxide was relatively the most reliable for the oxidation at 1250 ℃. It suggests that the effects of oxidation temperature of 4H-SiC (0001) had a trade-off between gate oxide reliability and SiC/SiO_2 interface properties.

§ 2.1.1 Introduction

Silicon carbide (SiC) is attractive for high-power electronic devices as its high energy efficiency, favorable thermal conductivity properties, and high breakdown electric field [1]. Furthermore, the ability to grow silica (SiO_2) by thermal oxidation as silicon (Si), makes the Si metal–oxide–semiconductor field-effect transistor (MOSFET) technology transferable to SiC despite the requirement of relatively high oxidation temperature [2-3]. However, in contrast to the Si/SiO_2 interface, thermal oxidation of SiC is believed to induce a high density of interface defects and near interface traps [4-5]. The defects and traps limit the channel mobility of SiC MOSFETs, resulting in an on resistance that is higher than theoretical value [6]. To minimize the effects of these interface defects and improve the reliability of SiC MOSFETs, post-oxidation annealing (POA) in NO_x, H_2, or forming gas had been widely investigated [7-8]. Even though NO_x annealing causes the interface state density (D_{it}) to decrease [7], the threshold voltage (V_{th}) drifts to the negative direction [9-11], which means that the MOSFETs might be easily turned on at 0V in the circuit application.

Therefore, a systematic investigation of the thermal oxidation reaction of SiC is important to the improvement of oxide reliability [12].

It is generally believed that carbon atoms will remains at SiC/SiO_2 interface at low oxidation temperature and the oxygen vacancy will be dominant for high temperature [13]. Therefore, it may be possible to reliably form gate oxide by carefully controlling the oxidation temperature to effectively remove carbon atoms and inhibit the decomposition of SiO_2 by only thermal oxidation [5, 14]. In previous reports, the lowest interface state density was obtained for the oxide formed at 1450°C [5]. However, the reliability of SiO_2 has not been investigated. In this study, we fabricate SiC MOS capacitors simply by controlling the thermal oxide temperature up to 1550℃ without any further passivating techniques. On the basis of value the SiC/SiO_2 interface state density, we especially paid attention to determine the reliability of SiO_2 by time zero dielectric breakdown (TZBD) and TDDB.

§2.1.2 Experimental

The starting substrates used in this study were 4° off-axis 4H-SiC (0001) wafers. They consist on a 350 μm-thick substrate (~1×10^{19} cm^{-3} n^+ type doped) covered with 12 μm-thick epitaxial layers (~8×10^{15} cm^{-3} n-type doped). First, wafers are cleaned in diluted Hydrofluoric acid (HF) followed by RCA cleaning. After wet cleaning, the wafers were introduced into an All-CVD SiC tube thermal oxidation system, followed by oxidation at 1200 to 1550°C in 1-atm in dry O_2 ambient, the oxidation temperatures and times are showed in Table I. The temperature was raised at a rate of 5°C/min in pure Ar to minimize the unwanted additional oxidation below 1200°C. Over 1200°C, the temperature was increased at a slower rate (<5 ℃/min) in Ar/O_2=0.99/0.01 until the target oxidation temperature was reached, O_2 gas was introduced in this stage in order to grow a thin oxide layer on the SiC surface to protect the device's characteristics from being affected by other gases. To accurately evaluate the effect of oxidation temperature on SiO_2/SiC interface and properties of SiO_2, the oxide film thickness of all samples was controlled to 50 nm.

The MOS capacitors were oxidized at various temperatures then the gas flow was quickly changed from O_2 to Ar at the oxidation temperature before the sample was cooled down. The oxide thickness was estimated by spectroscopic ellipsometry. For the evaluation of SiO_2/SiC interface and SiO_2 electrical characterization, Al was sputtered on the backside

after HF cleaning, RCA cleaning and reverses sputtering. Finally, Al circular electrodes (ø=300μm) were also evaporated as top-contact to form the MOS capacitors.

Table II-I. High temperature oxidation parameters.

NO.	Oxidation Temperature(℃)	Oxidation Time(min)
A	1550	10
B	1450	15
C	1350	20
D	1250	90
E	1200	200

§2.1.3 Measurement and Discussion

The capacitance-voltage (C-V) characteristics of the capacitors were measured at various frequencies including quasi-static capacitance-voltage (QSCV-the hold time is 100μs, and a sweep rate of 0.1V), 100 kHz and 1 MHz. Figure 2-1 shows the MOS capacitance of the capacitor fabricated by oxidation at 1350°C. The oxide thickness determined by ellipsometry was 52 nm, which is good agreement with capacitance equivalent thickness (CET) estimated from the maximum capacitance (C_{max}) of the C-V curves at 1 MHz to be 53 nm. The CET is given by:

$$CET = \frac{\varepsilon_0 \varepsilon_{sio_2} A}{C_{ox}} \tag{2-1}$$

A is the area of the 4H-SiC MOS gate electrode, and ε_{SiO2} is the dielectric constant of SiO_2.

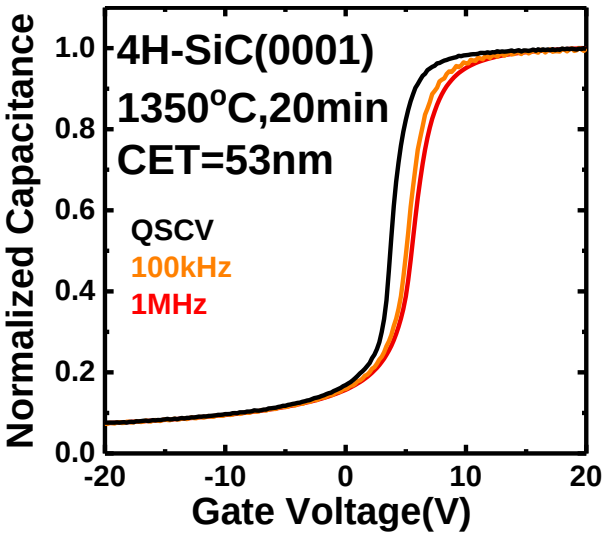

Figure 2-1. C-V characteristics of Al/SiO_2 (53 nm)/n-type 4H-SiC (0001) MOS capacitor measured by QSCV and 100 kHz.

The D_{it} values for the capacitors were estimated by the C-ψ_s method and high-low frequency method [4]. The ideal C-V curve was calculated using Possion's equation and surface potential [4]. To calculate the ideal curve, the oxide thickness, doping density of the epitaxial layer and flat-band voltage were set to 53 nm, 8.35×10^{15} cm^{-3} and 5.39 V respectively, the latter value was obtained from the C-V measurements at 1 MHz. The energy-level dependence of D_{it} calculated by the C-ψ_s method are presented in Figure 2-2 as a function of energy level, with reference to the conduction band edge of SiC. D_{it} evaluated by C-ψ_s method is given by:

$$D_{it}(C-\varphi_s)=\frac{C_{ox}}{q}\left(\frac{C_{QS}}{C_{OX}-C_{QS}}-\frac{C_{ideal}}{C_{OX}-C_{ideal}}\right) \quad (2\text{-}2)$$

q is the electronic charge, C_{QS}, C_{ox}, and C_{ideal} are the quasi-static, oxide, and ideal capacitance per area, respectively[4]. The measurements were done at room temperature on samples oxidized at 1200 to 1550°C. The samples exhibited D_{it} values of $1–5\times10^{12}$ cm^{-2} eV^{-1}, which are consistent with the reported values for as-oxidized films [5, 15]. The results revealed a clear dependence of D_{it} on the thermal oxidation temperature.

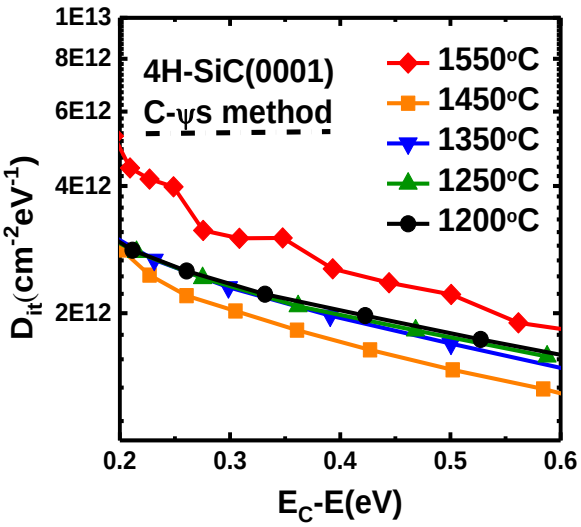

Figure 2-2. Interface state density (D_{it}) of SiO_2/SiC at room temperature as a function of energy level below the conduction band of SiC estimated by the C-ψ_s method. Five samples oxidized at temperatures from 1200 to 1550 °C were compared.

The D_{it} value for the SiO_2/SiC interfaces in samples oxidized at different temperatures was also estimated by the high-low method. The capacitors tested at the frequency 1 MHz and QSCV characteristics were used to evaluate D_{it} through the high-low method. Figure 2-3

shows the D_{it} values determined by the high–low method using:

$$D_{it}(High-Low)=\frac{C_{ox}}{q}\left(\frac{C_{Lf}}{C_{OX}-C_{Lf}}-\frac{C_{Hf}}{C_{OX}-C_{Hf}}\right) \quad (2\text{-}3)$$

D_{it} is the density of interface states responding to a frequency (f) range of f < 1 MHz. D_{it} evaluated by the C-ψ_s method is the total interface state density [4]. D_{it} evaluated by the high-low method exhibited the same trend as that determined with the C-ψ_s method. All the samples displayed D_{it} values in the range of 0.6-4×10^{12} $cm^{-2}eV^{-1}$ at 0.2eV, as shown in Figure 2-3. The SiO_2/SiC interface with the optimal D_{it} was obtained by oxidation at 1450°C. The results obtained from the high–low method agreed with the oxidation temperature dependence of the SiC/SiO_2 interface properties evaluated by the C-ψ_s method.

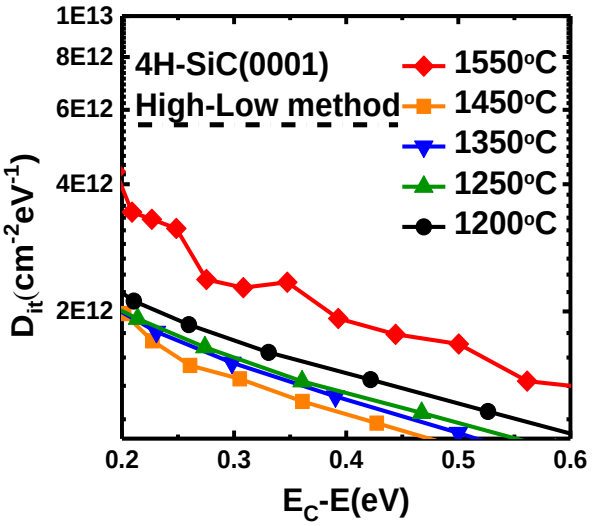

Figure 2-3. Interface state density (D_{it}) of SiO_2/SiC interface at room temperature as a function of energy level below the conduction band of SiC, estimated by high-low method. Five samples oxidized at temperatures from 1200 to 1550 ℃ were compared.

Figure 2-4 shows the D_{it} values at energy levels of E_c-E=0.3 and 0.6 eV as a function of the oxidation temperature determined by the C-ψ_s method Figure 2-4(a) and high-low method Figure 2-4(b). The D_{it} decreased with the increase of oxidation temperature up to 1450°C, but were relatively high when the oxidation temperature was above 1500°C. The improved interface properties at high oxidation temperature may be explained by favorable CO_x out-diffusion at high temperatures [13]. In addition, carbon impurities remained at the SiC/SiO_2 interface at low oxidation temperatures. Conversely, the degraded interface observed above 1450 ℃ may be related to the content of oxygen vacancies at high

temperature, as the active oxidation($SiC+O_2 \rightarrow SiO+CO$) will be dominant for high temperature region [16], the content of oxygen vacancies increasing at high temperature. The results obtained agree well with those reported previously [5].

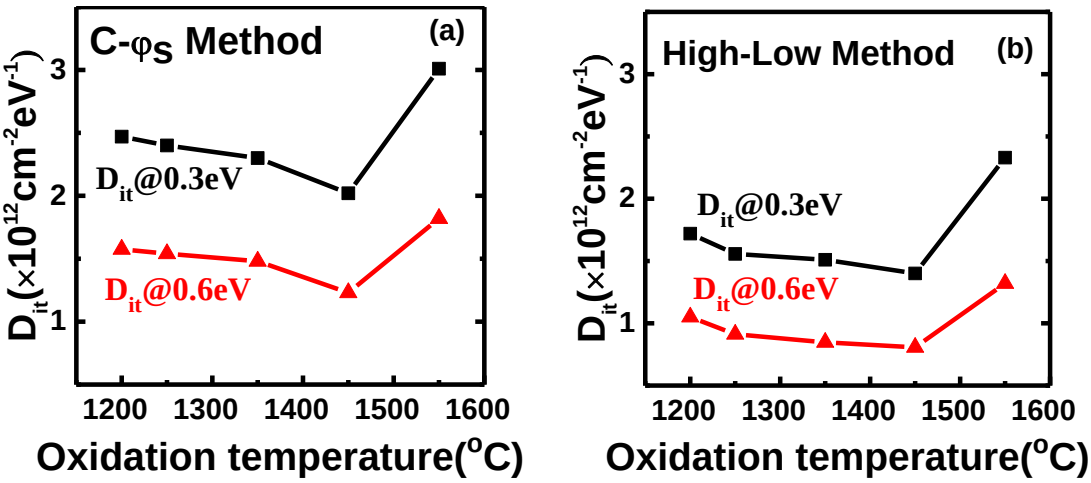

Figure 2-4. The dependence of D_{it} on oxidation temperature at energy levels of E_c-E=0.3 eV and 0.6 eV for SiC MOS capacitors fabricated by gate oxidation at various temperatures. Results of (a) the C-ψ_s method, (b) the high-low method.

Besides D_{it} at the SiO_2/SiC interface, the reliability of SiO_2 was also evaluated. To analyze the reliability of the 4H-SiC MOS capacitors, TZDB measurements were performed at room temperature. During the TZDB measurement, a voltage was applied to the gate electrodes. The voltage was increased in steps of +0.5 V till the gate oxide broke down. The oxide electric field (E_{ox}) used in these experiments is given by:

$$E_{ox} = \frac{V_g - V_{FB}}{T_{ox}} \tag{2-4}$$

V_g is the gate voltage, V_{FB} is the flat band voltage, V_{FB} was also determined from high-frequency C-V characteristics [7,17], and the V_{FB} were about 5.5-5.7 V. Then, a constant-voltage stress a little less than breakdown voltage was applied to the gate oxide at room temperature to analyze the time to breakdown (T_{BD}) of the samples.

Figure 2-5 shows the leakage current density-electric field (J-E) curves for the capacitors oxidized at different temperatures. The E_{ox} of the five samples only by oxidation are range from 8.7 MV/cm to 11.2 MV/cm. E_{ox} of the MOS capacitor oxide at 1250°C was the highest at 11.2 MV/cm which we plot it as Figure 2-6. Therefore, comparing with the samples oxidized above 1250°C shows that raising the oxidation temperature did not improve the reliability of the samples even though D_{it} was the lowest at 1450°C.

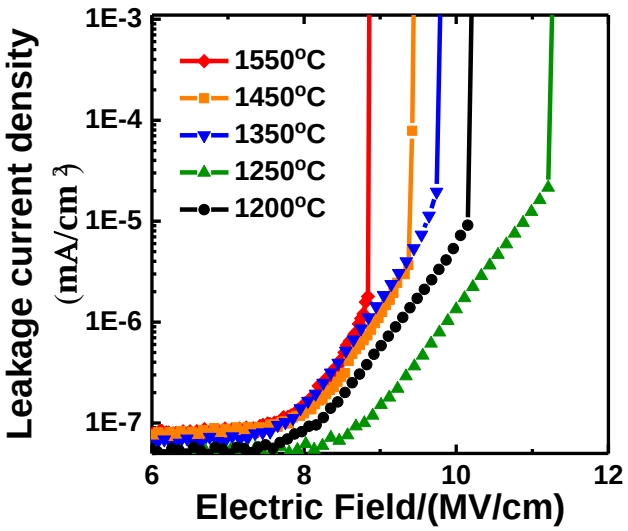

Figure 2-5. Typical J-E characteristics of SiC MOS samples oxidized from 1200 to 1550°C.

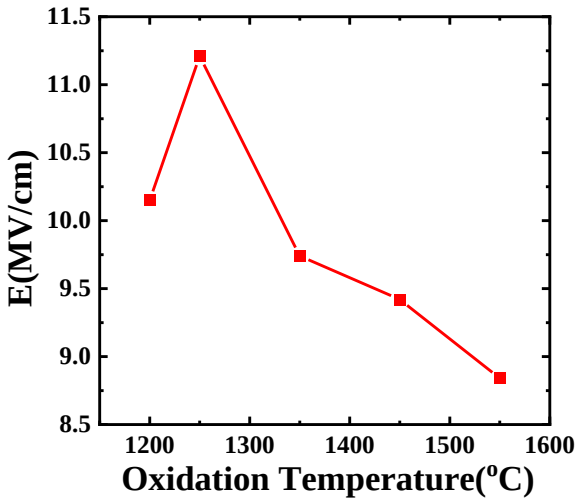

Figure 2-6. The oxidation temperature dependence of Q_{BD} at the failure rate 63.2% for SiC MOS capacitors fabricated by gate oxidation at various temperatures

The Weibull distribution plots of charge-to-breakdown were extracted from constant-voltage TDDB measurements for thermal oxides. The TDDB measurements were also performed at room temperature. Figure 2-7 depicts the TDDB measurement results for the thermally oxidized MOS capacitors. The charge-to-breakdown (Q_{BD}) was biggest when the sample was oxidized at 1250°C. The Q_{BD} value at a cumulative failure rate of 63.2% was 5.2×10^{-4} C/cm^2. Figure 2-8 displays the oxidation temperature dependence of Q_{BD} at the failure rate 63.2% for SiC MOS capacitors [17]. For sample oxidized above 1250°C, Q_{BD} decreased as the oxidation temperature increased. This illustrated the quality of the oxide layer degraded as the gate oxidation temperature increased.

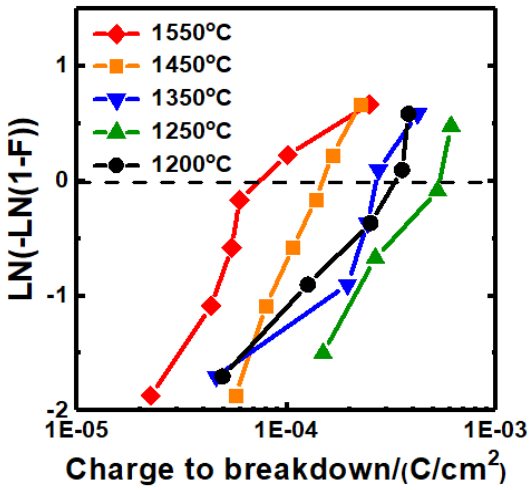

Figure 2-7. Weibull distribution of Q_{BD} obtained from TDDB measurement for SiC MOS capacitors fabricated by gate oxidation at various temperatures.

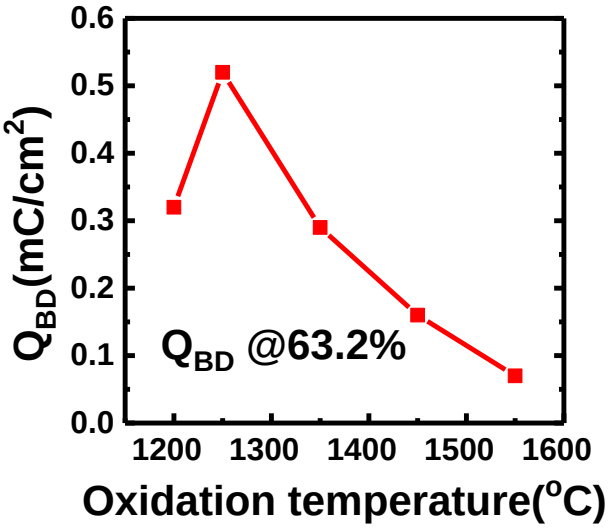

Figure 2-8. The oxidation temperature dependence of Q_{BD} at the failure rate 63.2% for SiC MOS capacitors fabricated by gate oxidation at various temperatures

§2.1.4 Results

In conclusion, ultra-high-temperature thermal oxidation of 4H-SiC Si-face was investigated. The C-V and TDDB measurements were used to characterize the gate oxide characteristics and reliability at room temperature of the SiC MOS capacitors. The C-V measurements confirmed that the optimal D_{it} was obtained for the sample oxidized at 1450°C in the energy range 0.2–0.6 eV below the conduction band edge of SiC. However, there was a trade-off between D_{it} and reliability, the sample oxidized at 1250°C showed the most reliable character of those tested.

§ 2.2 Analysis the Enhancement of Effects by Sequential Annealing in Ar and NO on 4H-SiC MOS devices

The effect of Ar annealing, NO annealing and sequential annealing in Ar and NO on interfacial characteristics and reliability of SiC MOS capacitors are investigated. The results show that sequential annealing has the best effect to improve reliability and oxide insulation. The reduction of interface state by sequential annealing is similar to that by NO annealing and better than that by Ar annealing. It suggests Ar annealing and NO annealing can remove specific defects; while sequential annealing can enhance the effect of annealing. The experiment provides new inspiration on annealing process of SiC MOS devices.

§ 2.2.1 Introduction

Silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) are expected to replace silicon-based power MOSFETs due to its excellent physical properties. Compared with other compound semiconductors, SiC is the only material can form SiO_2 layer by thermal oxidation, which can makes the silicon process transfer to SiC directly. However, C related defects generate in oxidation process, and the electrical properties of SiC MOSFETs are reduced [18,19]. In addition, the barrier height between SiO_2 and 4H-SiC is smaller than that between SiO_2 and Si, and the gate leakage of SiC MOS devices increases, which limits the lifetime of MOS devices [20]. Therefore, it is necessary to improve the manufacturing process to further increase the performance and reliability of SiC MOS devices.

In order to improve the performance and reliability of SiC MOS devices, high temperature annealing in a specific atmosphere has been widely studied. Ar annealing can reduce the interface state and improve the mobility of devices without introducing other elements and forming related defects [21, 22]. NO annealing shows better effect of passivate defect near the SiO_2/SiC interface [23-25]. Higher annealing temperature and longer annealing time can reduce interface defects better [26]. But it reduces the threshold voltage and makes the device more susceptible to the interference of gate electrode. However, the mobility and reliability of state-of-art SiC MOSFETs is far from material limit and need further improvement. The conventional way to improve the characteristics of the device is to change the experimental conditions of the existing process or annealing in a new atmosphere.

However, the combination of multiple annealing processes with complementary advantages has not been further studied. In this paper, the improvement of NO annealing affected by Ar annealing after thermal oxidation was studied, which provides new inspiration on annealing process of SiC MOS devices.

§2.2.2 Materials and Methods

The MOS structures were fabricated by using 4^{o} off-axis n-type 4H-SiC (0001) epilayers with a donor concentration of 8×10^{15} cm^{-3}. Following by standard Radio Corporation of America (RCA) cleaning, dry oxidation was carried out at $1250^{o}C$ for 90 min. The oxide thickness determined from the accumulation capacitance was about 50 nm. Then the samples were divided in groups for high temperature annealing process. The annealing process was carried out in Ar or NO atmosphere at $1300^{o}C$ under standard atmospheric pressure. SiC MOS capacitors annealed at $1300^{o}C$ in NO is expected to obtain lower interface state [27,28]. The annealing time in NO is 30 min, in case of saturation of annealing effect [29]. Under this annealing condition, the number of passivated defects per unit time is obvious, which is more beneficial to observe the effect of Ar annealing on NO annealing. Details of annealing conditions are given in Table II-II. The MOS capacitors were prepared by evaporating 200 nm Al on the oxide as gate electrode and on the bottom of SiC substrates as back electrode.

Table II-II. Details of high temperature annealing process and sample grouping

Sample	Atmosphere	Temperature	Time
as-ox	-	-	-
Ar 1300	Ar/O_2 = 9:1	$1300^{o}C$	15 min
NO 1300	N_2/NO = 9:1	$1300^{o}C$	30 min
Ar/NO 1300	Ar/O_2 = 9:1 N_2/NO = 9:1	$1300^{o}C$ $1300^{o}C$	15 min 30 min

The bidirectional capacitance-voltage test was used to characterize the near interface oxide traps (NITs). Multi frequency capacitance-voltage (C-V) method is used to measure the density of interface state (D_{it}) for SiC MOS capacitor. Current-voltage (I-V) test is used to test F-N tunneling barrier. Time dependent dielectric breakdown (TDDB) is used to characterize the reliability of gate oxide.

§2.2.3 Results and Discussion

§2.2.3.1 Bidirectional C-V Measurement

The results of bidirectional C-V measurement with frequency of 1 MHz is shown in Figure 2-9. The gate voltage direction of bidirectional capacitance-voltage measurement is from negative to positive and then back to negative. All the C-V curves show positive flat-band voltage，while the ideal flat-band voltage of SiC MOS is close to 0 V, which suggests the generation of negative defects in the preparation of SiC MOS capacitor. The curve position of sample NO1300 and Ar/NO1300 shows left drift compare with other samples, because of the introduction of N atoms. For SiC MOS devices after NO annealing, N atoms are accumulated at SiO_2/SiC interface [30]. The introduction of N atom can effectively reduce the interface state, but the NITs produced [31]. These traps can release electrons and presented as positive charge, which leads to the negative drift of C-V curve and makes the flat-band voltage close to the ideal value [32, 33]. Compared with sample as-ox, the C-V curve of sample Ar1300 shows slight negative shift, which implies some defects are repaired by Ar annealing. The sample Ar/NO1300 shows right drift compared with the sample NO1300, which suggest the repaired defects by Ar annealing inhibit the accumulation of nitrogen at the SiO_2/SiC interface. It can be deduced that the N accumulation is promoted by the un-annealed defects near the interface. All the samples show hysteresis because of the curve drift in bidirectional C-V measurement. When the gate voltage sweeps from negative to positive, NITs capture the accumulated electrons near the SiO_2/SiC interface. The time constants of these defects are longer than that of the interface state defects so that it cannot follow the AC signal at room temperature [34]. These traps have to take a long time to release electrons, and change the position of C-V curves in the later measurement [35, 36]. In practical application of MOSFETs, hysteresis will cause large off-state leakage current and small on-state current, and increase switch time and energy loss[36]. It can be easily observed that the process including NO annealing can effectively reduce the hysteresis and then improve the stability of MOS devices.

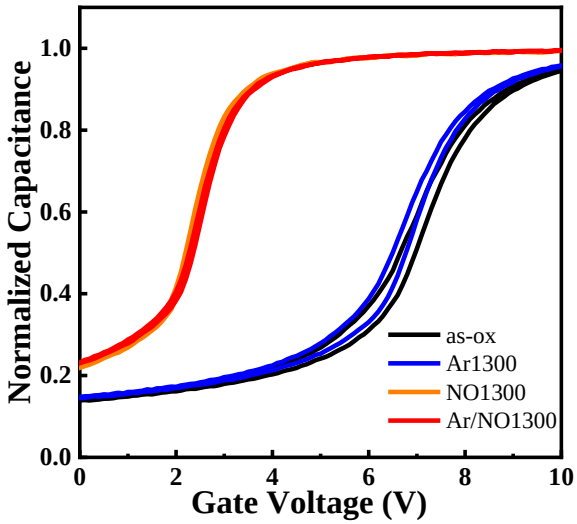

Figure 2-9. Bidirectional C-V measurement of SiC MOS capacitor

The further comparison of hysteresis for SiC MOS capacitors is described in Figure 2-10. The hysteresis is expressed by the change of flat-band voltage in bidirectional C-V measurement. All the annealed samples show decreased hysteresis compared with sample as-ox. When Ar annealing is carried out, the hysteresis voltage decrease. It indicates that Ar annealing repaired a portion of NITs [21]. The hysteresis voltage of NO annealed samples is further reduced, which suggests that the introduction of N has better effect on reducing NITs. Sample Ar/NO1300 has the lowest hysteresis voltage, indicating collaborative of Ar and NO annealing can further reduce NITs. It suggests that annealing in Ar or NO have specific effects on different kinds of NITs defects. Because the thickness of oxide layer increased in annealing process, it is not objective to just compare the hysteresis voltage. Therefore, the hysteresis voltage is converted to the effective NITs density at the interface regardless of oxide thickness:

$$N_{NITs} = \frac{A \times (V_{nFB} - V_{pFB})}{C_{ox}} \tag{2-5}$$

where V_{pFB} and V_{nFB} represent the flat-band voltage of the C-V curve sweep from negative to positive, and V_{nFB} represent respectively the flat-band voltage of the C-V curve sweep from positive to negative, C_{ox} is the oxide capacitor, and A is the area of the SiC MOS capacitor. It can be seen from Figure 2-10 that the comparation result of N_{NITs} is consistent with the previous discussion, which shows that the impact of oxide thickness on N_{NITs} is negligible. It must be note that higher electric field is applied on the samples including NO annealing process, because the lower flat-band voltage causes greater gap to the max gate test voltage, as

depicted in Figure 2-9. Therefore, the actual effect of NO annealing is better than the result depicted in Figure 2-10. It is apparent that the collaborative Ar annealing and NO annealing is effective to improve the near interface quality of SiC MOS devices.

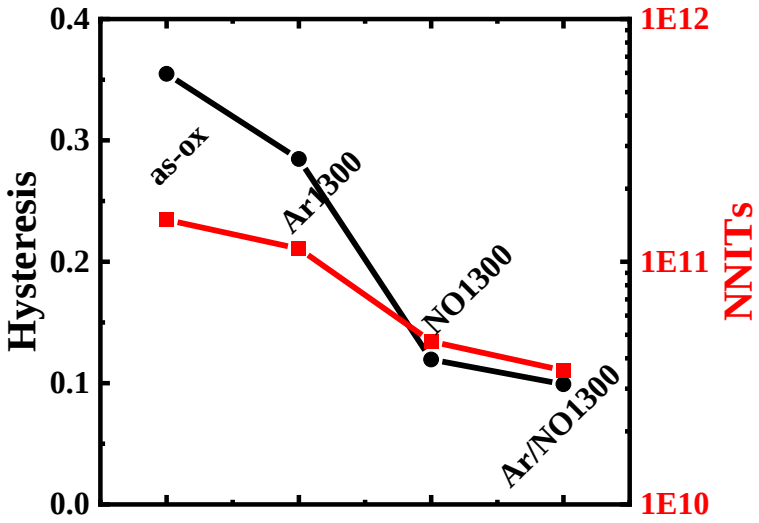

Figure 2-10. Hysteresis of flat-band voltage in bidirectional C-V measurement and calculated NITs density of SiC MOS capacitor. Connections are just for comparison.

§2.2.3.2 Interface State Density

SiC MOSFETs suffered from low channel mobility owing to the high density of interface states. To evaluate the density of interface state (D_{it}), high-low method was used [37]. The interface state defects act as capacitance to exchange charges between the bulk and the interface in low frequency measurement, but they cannot respond to this process in high frequency measurement. Capacitance differences were extracted from the high frequency and low frequency C-V characteristics, and D_{it} was calculated. In the experiment, the high frequency and low frequency characteristics was measured at 1MHz and 10 kHz. Figure 2-11 shows the D_{it} distribution relative to conduction band edge (E_c) of 4H-SiC for SiC MOS capacitance with different annealing process. Compared with the sample as-ox, Ar annealing increases the D_{it} of SiC MOS capacitor, which implies that additional defects are generated at SiO_2/SiC interface. This is because during the annealing process, additional oxidation occurs at the SiO_2/SiC interface, which increases the density of interface defects. Annealing in oxygen with low partial pressure will cause carbon residual near the interface, which may be the reason for the increase of the D_{it} for sample Ar1300 [38]. The increase of D_{it} and the decrease of NNITs in sample Ar1300 indicate that residual carbon mainly accumulates on the SiC side of the SiO_2/SiC interface, forming interface state defects such as carbon dimers [22]. It

suggests that the Ar annealing before NO annealing mainly affects the quality of the oxide layer near SiO_2/SiC interface, but has limited effect on the interface state.

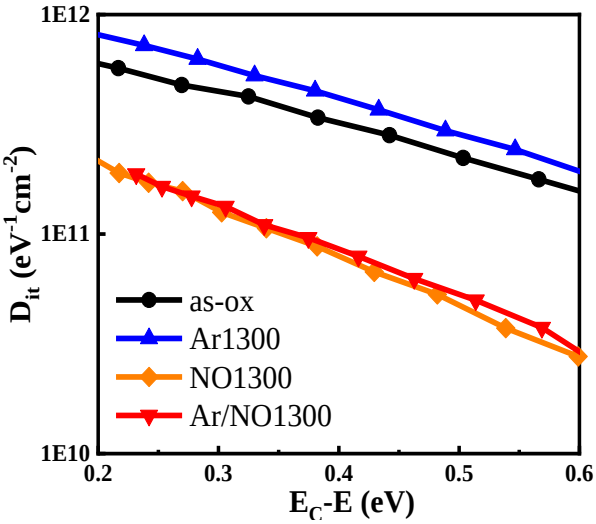

Figure 2-11. D_{it} near the conduction band of SiC MOS capacitor

§2.2.3.3 F-N barrier of Gate Dielectric

The F-N plot was calculated from J-E characteristics of SiC MOS capacitors, and depicts in Figure 2-12. Figure 2-13 shows the F-N barrier of gate oxide dielectric after different annealing processes. The F-N barrier decreased after Ar annealing, which deteriorated the insulation of SiC MOS gate oxide on high electric field. When NITs capture electrons, the conduction band of SiO_2 near the interface increases [20]. Although some defects are reduced by annealing, the F-N barrier will also be reduced, resulting in poor insulation. The F-N barrier of NO1300 is increased, which indicates that the high temperature annealing in NO at 1300°C could effectively improve the insulation of SiC MOS gate dielectric. The improvement is related to the introduction of nitrogen at SiO_2/SiC interface. Nitrogen may passivate some oxide traps, thus reducing the barrier narrowing of F-N tunneling and increasing the effective barrier height [34]. The annealed oxide traps also decreased the hysteresis in bi-direction C-V measurement, as depicted in Figure 1. Sample Ar/NO1300 shows higher F-N barrier height than sample NO1300, which indicates that Ar annealing can enhance the effect of NO annealing on passivating oxide traps and NITs.

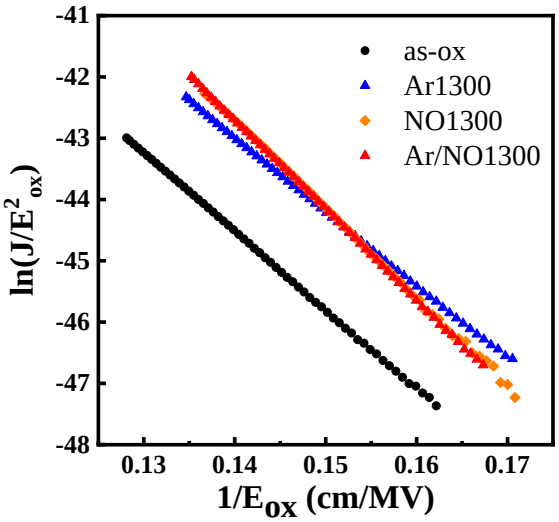

Figure 2-12. Fowler-Nordheim plots of fabricated MOS capacitors.

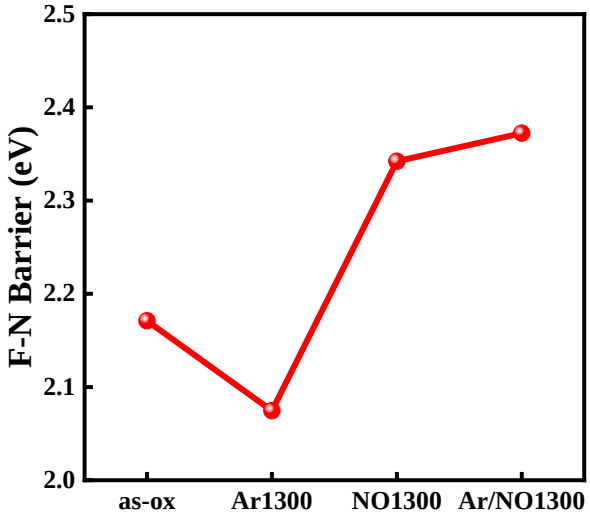

Figure 2-13. F-N barrier of SiC MOS capacitor. Connections are just for comparison.

§2.2.3.4 Reliability of Gate Dielectric

Figure 2-14 shows the Weibull distribution of SiC MOS capacitors after different annealing processes in TDDB test. All the curves of annealed samples shift to the right with different degrees, which indicates that more charge can inject into gate oxide before breakdown occurred. The breakdown charge obtained by linear fitting is shown in Figure 2-15. Compared with sample as-ox, the breakdown charges for all the annealed samples are increased. The increase of breakdown charge suggested the improvement of the reliability, and increase the lifetime of SiC MOS devices in practical applications. Compared with samples annealed in Ar, the breakdown charge of gate oxide increases significantly after high

temperature annealing in NO. It indicates that the introduction of nitrogen is helpful to improve the reliability of gate dielectric for SiC MOS capacitor [35,36]. In addition, sample Ar/NO1300 shows the maximum gate dielectric breakdown charge, which indicates that Ar annealing before NO high temperature annealing is helpful to further improve the reliability of SiC MOS capacitor gate dielectric and prolong the device lifetime.

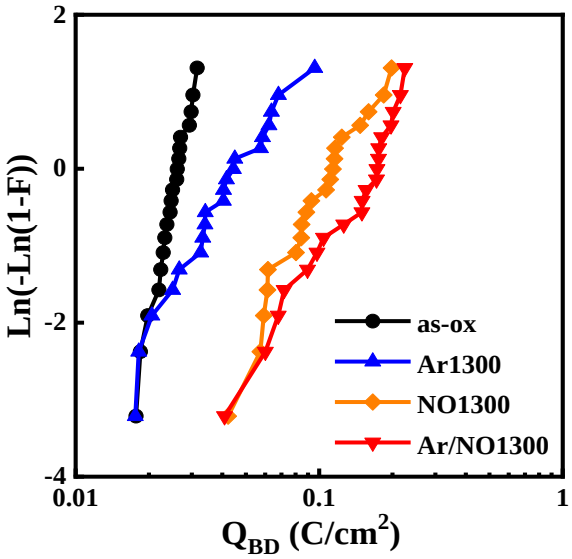

Figure 2-14. Weibull distribution of Q_{BD} obtained from TDDB measurements for the fabricated MOS capacitors.

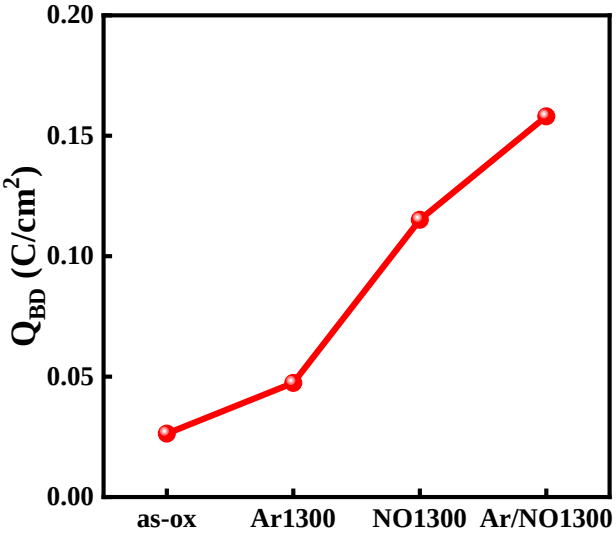

Figure 2-15. Annealing process dependence of Q_{BD} at F=63.2% obtained from TDDB measurement at 300 K. Connections are just for comparison.

§2.2.4 Discussion

The performance and reliability of SiC MOS capacitors in the experiment are summarized in Table II-III. Here we discuss the effect of Ar annealing and NO annealing effect on SiC MOS devices. C related byproducts are formed in the oxidation process, and accumulated at the SiO_2/SiC interface. These defects are electrically active and reduce electrical properties and reliability. When annealing in high temperature, C related defects are diffused from SiO_2/SiC interface into the oxide. But the residual C atoms in oxide will reduce the reliability [33]. The introduction of oxygen will oxidize these atoms into CO which are easier to diffuse out of SiO_2 layer. Furthermore, oxygen can reduce the near interface defects in oxide, and relieve the hysteresis and increase the Q_{BD}. But the reduction of NITs reduced the F-N barrier as depicts in Figure 2-13. The D_{it} of sample Ar1300 is high than as-ox, which may due to that the slow oxidation promotes the accumulation of C atoms at the interface. In NO annealing, N atoms accumulated in the SiO_2/SiC interface. Accumulated C atoms in the interface are decomposed and the D_{it} decreased. NO annealing could passivate defects in oxide whose energy is higher than 4H-SiC conductance band. These defects capture electronics accumulated at the SiO_2/SiC interface by tunneling, and narrow the effective F-N barrier [23]. Therefore, SiC MOS capacitors annealed in NO shows increased F-N barrier compared with annealed in Ar.

Table II-III. The summary of experiment characteristics of SiC MOS

Sample	**N_{NITs} (cm^{-2})**	**D_{it} (E_c-E=0.5eV) ($eV^{-1}cm^{-2}$)**	**Q_{BD} (C/cm^2)**	**F-N Barrier (eV)**
as-ox	1.49E+11	4.31E+11	0.02633	2.17
Ar 1300	1.13E+11	5.72E+11	0.04738	2.07
NO 1300	4.70E+10	1.30E+11	0.11512	2.34
Ar/NO 1300	3.56E+10	1.36E+11	0.15806	2.37

Then we discuss the effect of sequential annealing in Ar and NO. In Figure 2-10, the reduction of NITs of sample Ar1300 and sample NO1300 implies Ar annealing and NO annealing are effective to reduce near interface defects. The further reduction of NITs for Ar/NO1300 suggests Ar annealing and NO annealing passivate different defects. This conclusion is also proved by the results of TDDB measurement in Figure 2-12, where the Q_{BD} of sample Ar/NO1300 shows the maximum value. In the Figure 2-13, J-E characteristics seem shows different trend, where the F-N barrier of sample Ar1300 reduced. The phenomenon is

related to defects in the oxide near SiO_2/SiC interface. Electrons can be captured by these defects and act as negative fixed charge during measurement, and the effective barrier of SiO_2 and SiC increases. Electrons are more difficult to skip over the barrier and gate current decreased [20, 34]. After Ar annealing, some near interface defects are passivated, and the effective barrier are reduced. NO annealing passivates the defect which narrows the F-N barrier, and increases the effective barrier height [30]. Therefore, the ability of NO annealing to improve the insulation of SiO_2 layer is further enhanced by Ar annealing. The enhancement of sequential annealing is not applicable to interface state, where sample Ar/NO1300 and NO1300 shows similar distribution. It suggests the reduction of D_{it} is mainly contributed to NO annealing. The experiments imply that the combination of several annealing process could further improve the performance and reliability of SiC MOS devices, which provides new inspiration for researchers.

§2.2.5 Conclusion

In summary, the effect of Ar annealing, NO annealing and sequential annealing in Ar and NO on interfacial characteristics and reliability of SiC MOS capacitors are investigated. The processes containing NO annealing could effectively reduce the defects near the SiO_2/SiC interface and improve the reliability and insulation of SiO_2. In particular, the sequential annealing in Ar and NO could further reduce the N_{NITs} and improve the reliability of SiO_2 layer. The D_{it} of sequential annealing and NO annealing are similar, which suggests the reduction of D_{it} is mainly attribute to NO annealing. It shows that Ar annealing can improve the quality of oxide layer near the SiO_2/SiC interface and enhance the effect of NO annealing. It implies that the combination of various annealing processes may further improve the performance and reliability of SiC MOS devices, which provides new inspiration on annealing process of SiC MOS devices.

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Chapter 3: The Mechanism of the Effects of NO Annealing on the SiO_2/SiC Interface State and Reliability

§3.1 The Correlation between the Reduction of Interface State Density at the SiO_2/SiC Interface and the NO Post-Oxide-Annealing Conditions

We fabricated SiO_2/4H-SiC (0001) MOS capacitors with oxidation temperature at 1350^{o}C, followed by post-oxide-annealing (POA) in NO simply by the control of POA temperatures and times. A correlation between the reduction of interface state density and the increasing of N concentration at the interface has been indicated by C-ψ_s measurement and secondary ion mass spectrometry (SIMS). The SiO_2/4H-SiC interface density decreased when POA temperature was elevated, and the sample annealed at 1300^{o}C for 30min showed the lowest interface state density about 1.5×10^{12} $cm^{-2}eV^{-1}$ at E_c-E=0.3 eV when the N concentration is 11.5×10^{20} cm^{-3}. Meanwhile, the SiO_2 /4H-SiC interface annealed at 1200^{o}C for 120min showed the highest N concentration at the 4H-SiC/SiO_2 interface is 12.5×10^{20} cm^{-3}, whereas the interface state density is 2.5×10^{12} $cm^{-2}eV^{-1}$ at E_c-E=0.3 eV higher than 1300^{o}C for 30min. The results suggested that higher temperature POA might be much more efficiency in decreased the 4H-SiC MOS interface density with increasing the N area concentration.

§3.1.1 Introduction

Owing to its wide band gap and its high thermal conductivity, silicon carbide (SiC) is suitable for high-voltage power electronic devices with high energy efficiency. In addition, its ability to growing SiO_2 by thermal oxidation as silicon (Si) is one of the unique advantages over other wide-gap semiconductors such as GaN [1-2]. Among the typical poly of SiC (3C, 4H and 6H), 4H-SiC is the most suitable poly type for electronic applications. However, in contrast with the Si/SiO_2 interface, the 4H-SiC/SiO_2 interface features a high density of interface state (D_{it}) reaching 10^{13} $cm^{-2}eV^{-1}$, evaluated based on the differences between quasi-static and theoretical capacitances [3] (C-ψ_s method), near the 4H-SiC conduction band, which limits the inversion channel mobility of 4H-SiC metal-oxide-semiconductor (MOS) field effect transistors [4], as well as the reliability. For

the reduction of the effects of those interface defects, various passivation techniques have been extensively investigated, such as annealing in nitrous(N_2O), ammonia (NH_3) or a nitric (NO) [5]. Post-oxide-annealing (POA) in NO is regarded as the most promising method to improve the interface quality recently [6], being effectively increase channel mobility of SiC MOS and reduce interface state density at 4H-SiC/SiO_2 interface. However, it is unclear how the interface defects are reduced by nitridation [8]. To unveil the mechanism for further reduction of D_{it} after NO POA, we consider it is crucial to employ NO POA conditions suitable for the elimination of carbon precipitation or active oxidation at the interface because they are the most possible origin of those defect.

In this study, 4H-SiC MOS interface annealed in NO has been investigated by evaluating the electrical characteristics, and a correlation between the N concentration and the interface state density (D_{it}) at the SiO_2/4H-SiC interface has been indicated [7].

§3.1.2 Experiment

4H-SiC (0001) Si face wafers with a net donor concentration of 8×10^{15} cm^{-3} epitaxial layers were cleaned in diluted Hydrofluoric acid (HF), followed by the oxidation at 1350^{o}C for 20 min in 1-atm dry O_2 with furnace. After oxidation, post-oxide-annealing (POA) was carried out in NO (10% diluted in N_2) at the temperature from 1200~1300^{o}C for 30 min (Sample label: NO1300-30~NO1200-30) or the time from 30~120 min at 1200^{o}C (Sample label: NO1200-30~NO1200-120), a sample without NO annealing also prepared (w/o NO), then a circular Al electrode with a diameter of 300 μm were sputtered on the sample surface as top-contact (300 nm). Finally, 300 nm Al were sputtered as the back electrode for the SiC MOS capacitors. The structure of 4H-SiC MOS is shown in Figure 3-1 and the experimental conditions are summarized in Table III-I.

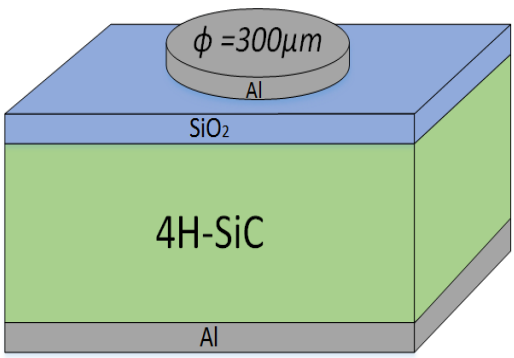

Figure 3-1. The structure of 4H-SiC MOS

Table III-I. The experimental conditions

Label	Oxidation	NO annealing
w/o NO	1350°C,20 min	/
NO1300-30	1350°C,20 min	1300 °C,30 min
NO1250-30	1350°C,20 min	1250 °C,30 min
NO1200-30	1350°C,20 min	1200 °C,30 min
NO1200-120	1350°C,20 min	1200 °C,120 min

§3.1.3 Measurement and Discussion

The C-V characteristics were measured with a small signal amplitude of 30 mV and using a voltage from -10 V to 10 V, the voltage step of 0.1 V. The capacitance-voltage (C-V) characteristics measured with various frequencies by quasi-static capacitance-voltage (QSCV) and 100 kHz are shown in Figure 3-2 for the 4H-SiC MOS capacitor annealing at 1300°C for 30 min (Sample NO1300-30). The oxide thickness determined by ellipsometer was 58 nm, which is a good agreement with capacitance equivalent thickness (CET) estimated from the maximum capacitance (C_{max}) of the C-V curves at 1MHz to be 59 nm. The CET is given by

$$CET = \frac{\varepsilon_0 \varepsilon_{sio_2} A}{C_{ox}} \tag{3-1}$$

A is the area of the 4H-SiC MOS gate electrode, and ε_{SiO2} is the dielectric constant of SiO_2 [8].

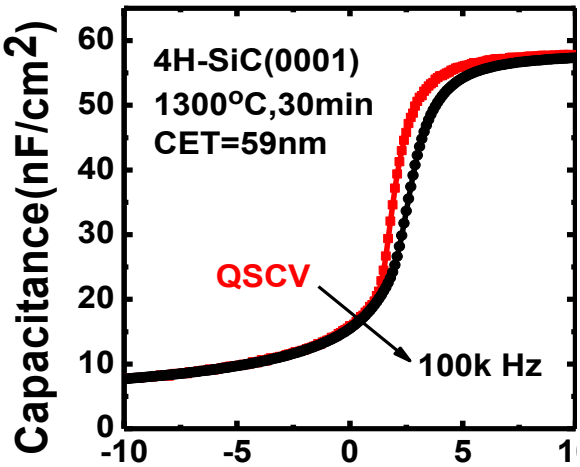

Figure 3-2. C-V characteristics of Al/SiO_2 (59 nm) /n-type 4H-SiC (0001) MOS capacitor measured by QSCV and 100 kHz. The annealing condition was annealed at 1300°C for 30min.

In order to obtain the theory CV of all samples, we first need to obtain the flat band voltage, doping concentration and C_{ox} and other parameters; these parameters can be obtained by CV test at 1MHz, as shown in Figure 3-3.

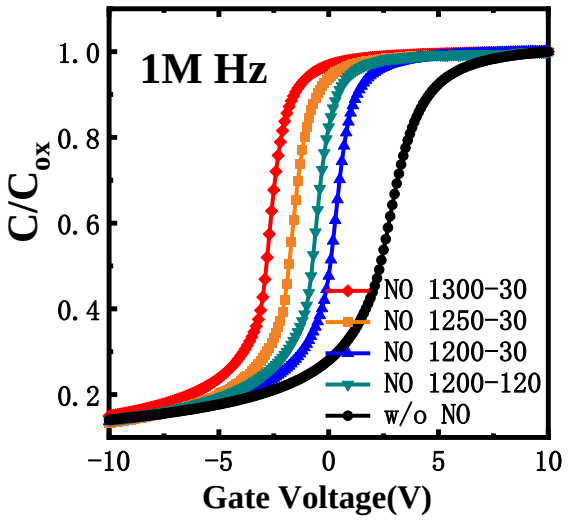

Figure 3-3. C-V characteristics of Al/SiO_2 (59 nm) /n-type 4H-SiC (0001) MOS capacitor samples in the experiment measured by 1MHz.

At the same time, we tested the QSCV of all samples in this experiment in order to obtain the CV curve of the sample under quasi-static, as shown in Figure 3-4.

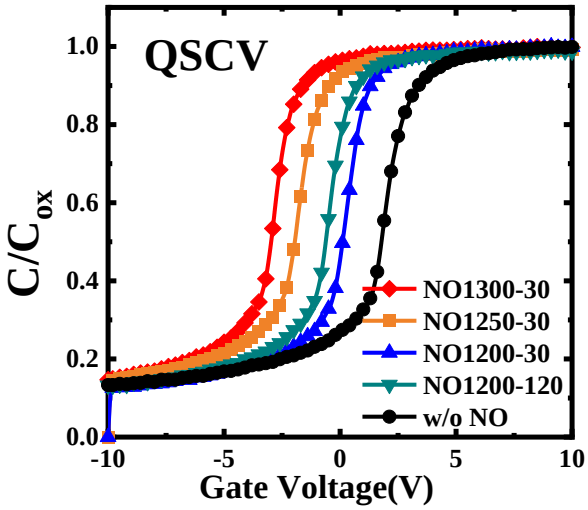

Figure 3-4. C-V characteristics of Al/SiO_2 (59 nm) /n-type 4H-SiC (0001) MOS capacitor samples in the experiment measured by QSCV.

Comparing the effect of flat band voltage with nitridation time at the same nitridation temperature; we will find that as the nitridation time increases, the flat band voltage moves in the negative direction, as shown in Figure 3-5.

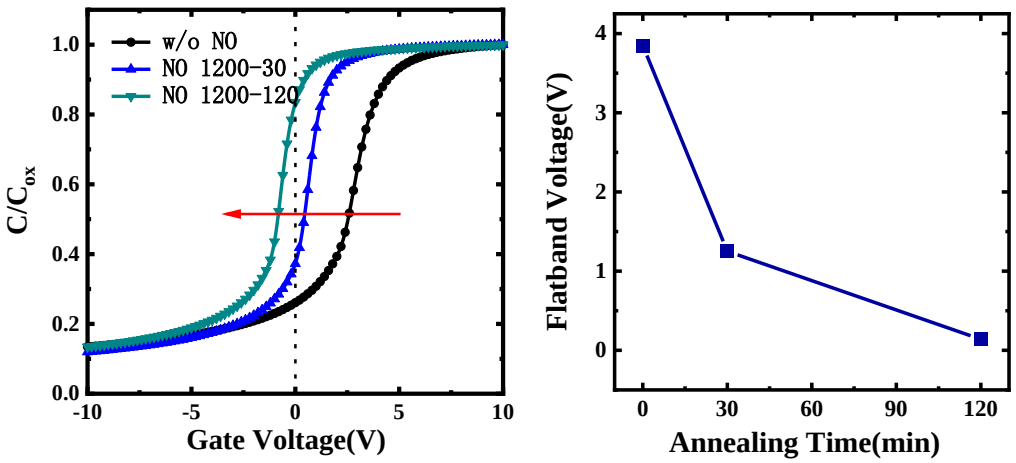

Figure 3-5. the flatband voltage dependence on nitridation time at the same nitridation temperature in the experiment measured by QSCV.

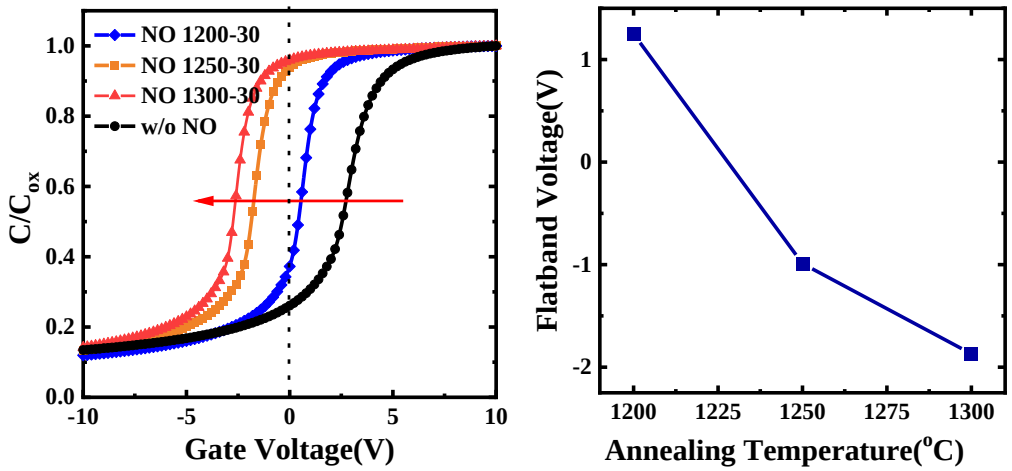

Figure 3-6. the flat-band voltage dependence on nitridation temperature at the same nitridation time in the experiment measured by QSCV.

In addition, we also compared the effect of the nitriding temperature on the flat band voltage at the same nitriding time. We can also know that as the nitriding temperature increases, the flat band voltage drifts in the negative direction seriously, even reaching Negative voltage, as shown in Figure 3-6.

According to quasi-static capacitance-voltage (QSCV) characteristics and the high frequency C-V curve, the ideal C-V curve was calculated from Passion's equation. For the calculation of the ideal curve, the doping density in epitaxy layer and the flat-band voltage were set to 8.63×10^{15} cm^{-3} and -2 V respectively by capacitance-voltage (C-V) characteristics measured with 100 kHz at room temperature (Sample NO1300-30). The

results of D_{it} are shown in Figure 3-7 as a function of energy level, with reference to the conduction band edge of 4H-SiC. The interface state density evaluated by C-ψ_s method is given by

$$D_{it}(C-\varphi_s)=\frac{C_{ox}}{q}\left(\frac{C_{QS}}{C_{OX}-C_{QS}}-\frac{C_{ideal}}{C_{OX}-C_{ideal}}\right) \quad (3\text{-}2)$$

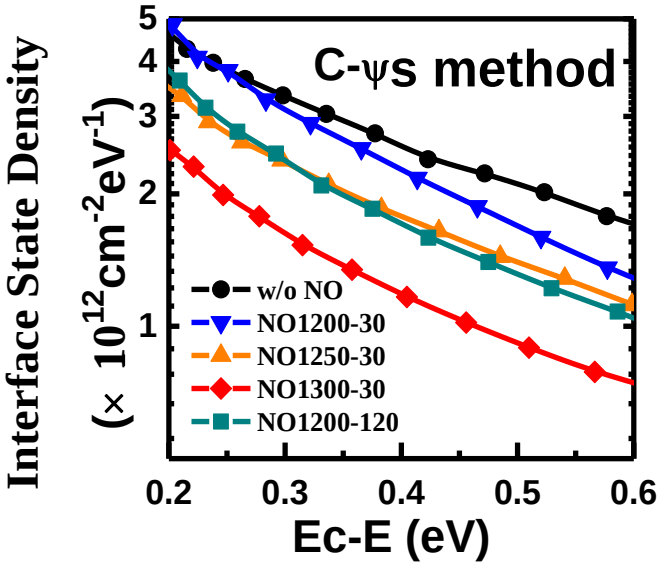

Figure 3-7. Interface defect state density (D_{it}) as a function of energy level below the conduction band of SiC, estimated by the C-ψ_s method, measured at room temperature.

The measurements were done from the samples in Table I at room temperature. As a result, for all the samples, the interface state density is about 0.5-5 $\times 10^{12}$ $cm^{-2}eV^{-1}$, which are similar with the reported values of as-annealed films[5].

To investigated the correlation between the reduction of interface state density and N concentration. Figure 3-8 shows the depth profile of N atom concentration measured by secondary ion mass spectrometry (SIMS) for the four samples annealing in NO. According to the earlier reports, the depth profile of N atoms exhibited a distinct peak at the interface for the samples annealing in NO, which is set as the origin of the horizontal axis [4,7-9]. The N peak of the samples NO1300-30~ NO1200-30 shows the N concentration increasing with the annealing temperature improving or the annealing time extending from the samples NO1200-30 ~ NO1200-120. The N concentration of sample NO1300-30 is mainly equal to sample NO1200-120, but the interface state density has a big difference.

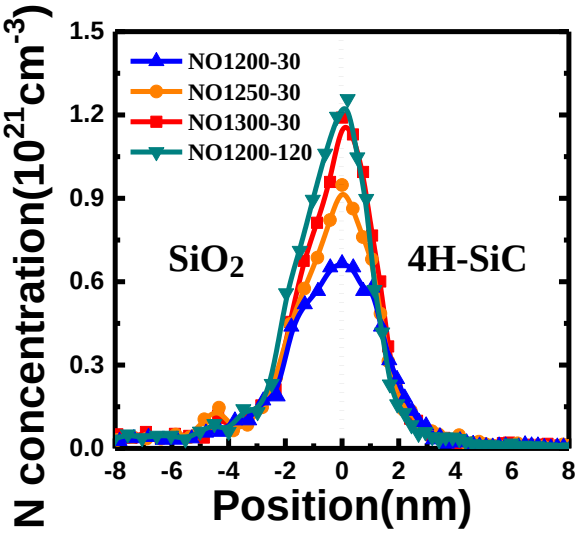

Figure 3-8. The N concentration increases by extending the annealing time or by elevating temperature at the SiC/SiO_2 interface, measured by SIMS.

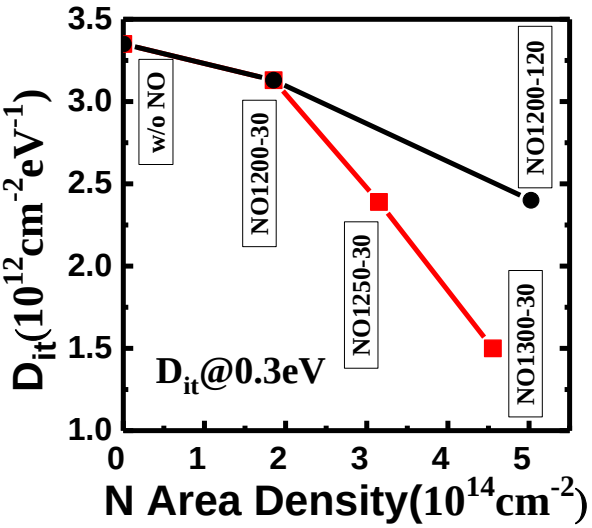

Figure 3-9. The dependence of D_{it} at E_c-E=0.3 eV on the area concentration of N atoms.

The dependence of interface state density (D_{it}) at E_c-E=0.3 eV on the concentration of N atoms calculated from SIMS profiles is shown in Figure 3-8[10]. From the result, the interface state density showed a minimum at the annealing temperature of 1300°C. The density of interface states decreased when the N concentration increased [10]. The increasing of POA temperature reduce the D_{it} remarkably than the extending of POA time under the same increasing of N concentration. This is probably the N atoms formed strong bonds with Si or C, they passivated the origin traps of interface[9]. The data can be fitted by the first-order rate equation: $N[t]=N^{*}(1-e^{-t/\tau})+c$. [11]

§3.1.4 Summary

In this article, it is revealed that the interface state density near the conductance band reduces significantly when the annealing temperature reaches to 1300°C or the annealing time extends to 120 min. In conclusion, the interface state density reduces when the POA temperature was elevated or the POA time was extended. Through SIMS measurement, it also can be concluded that the increasing of N concentration at the interface will reduce the interface state density, but the effects of temperature increasing is more remarkable.

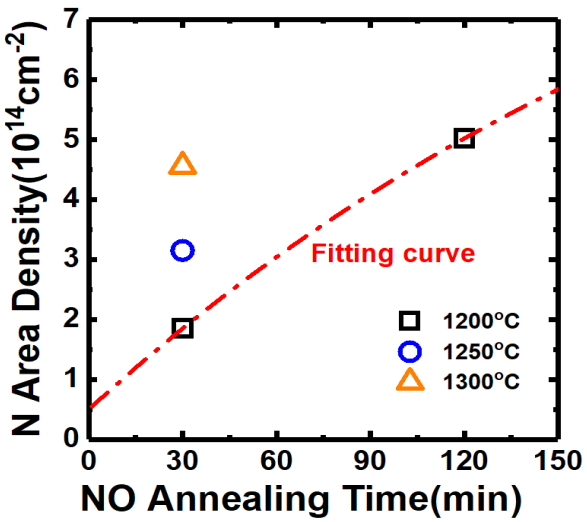

Figure 3-10. The dependence of N Area Density on NO Annealing Time.

§ 3.2 Reliability of 4H-SiC (0001) MOS Gate Oxide by NO Post-Oxide-Annealing

In this work, we investigated the oxide reliability of 4H-SiC (0001) MOS capacitors, the oxide was fabricated about 60 nm by thermal oxidation temperature at 1350^{o}C, the oxides than annealed at different temperatures and times in diluted NO (10% in N_2). The 4H-SiC MOS structure was analyzed by C-V and I-V measurement. Compared the J-E curves and Weibull distribution curves of charge-to-breakdown for fives samples under different annealing temperature and time, it shows that the high annealing temperature improves the electrical properties as the lifetime enhanced. The mode value of field-to-breakdown (E_{BD}) for thermal oxides by post-oxide-annealing in NO for 30 min at 1350^{o}C was 10.09 MV/cm, the charge-to-breakdown (Q_{BD}) of this sample was the highest in all samples, and the Q_{BD} value at 63.2% cumulative failure rate was 0.15 C/cm^2. The Q_{BD} of the sample annealing at 1200^{o}C for 120 min was 0.06 C/cm^2. The effects of NO annealing in high temperature enhance the lifetime of electrical properties and field-to-breakdown obviously. It can be demonstrated that the annealing temperature as high as 1300^{o}C for 30 min can be used to accelerate TDDB of SiC MOS gate oxide.

§3.2.1 Introduction

As an attractive material for high-voltage and high-temperature devices and its rather exceptional ability to fabricating SiO_2 through thermal oxidation as silicon (Si) [3,7,12], silicon carbide (SiC) is regards as the next-generation material for power metal-oxide-semiconductors field-effect transistors (MOSFETs) devices [13], it is expected to replace traditional Si power devices. However, thermal oxidation of SiC has been believed to induce a large number of defects, which will result in low channel mobility(μ_{FE}) (10-15 cm^2/V·s) and poor reliability of oxides [15-15]. The low channel mobility is recognized as the major affects for the insufficient 4H-SiC MOS performance. It is re-ported that post annealing in nitric oxide (NO)s or nitrous oxide (N_2O) gas can effectively improve the channel mobility for inversion-mode 4H-SiC MOSFETs[16]. It is regarded as a promising method to improve the MOS oxide quality through high temperature anneals in NO [7,12,17].

To realize SiC based MOS devices, it is important that high quality gate oxide can be fabricated. In this study, we investigate the relationship between the oxide reliability and the annealing temperature and time by analyzing time-dependent dielectric breakdown (TDDB) behaviors of the 4H-SiC MOS capacitors. We found that annealing in NO at high temperature improves the oxide lifetime and reliability obviously than enhancing the annealing time.

§3.2.2 Experiment

We fabricated five SiO_2/SiC capacitors on 4H-SiC (0001) substrate with an n-type epitaxy layer ($N_D = 8\times10^{15}$ cm^{-3}). After RCA cleaning, a 4H-SiC (0001) wafer with 4^o angel and n-type epitaxial layer was cleaned by dipping in hydrofluoric acid (HF) to remove sacrificial oxide layer. The samples were then immediately loaded into an oxidation furnace and oxidized in 1-atm dry O_2 ambient at 1350°C for 20 min. After oxidation, it was carried out in NO (10% diluted in N_2) at the temperature from 1200~1300°C for 30 min or the annealing time from 0~120 min at 1200°C .Then, a circular Al (300 nm) electrodes with a diameter of 0.3 mm were sputtered on the sample surface. Finally, 300 nm Al were sputtered as the back electrodes for the MOS capacitors. The structure and fabrication process flow are showing in Figure 3-11, and the experimental conditions and experiment results are summarized in table III-I.

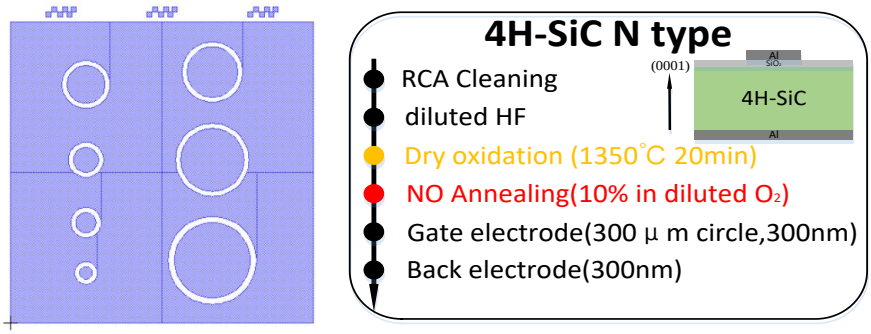

Figure 3-11. The structure of MOS-CAP fabrication process flow.

§3.2.3 Measurement and Discussion

The C-V characteristics were measured with a small signal amplitude of 30mV and using a voltage from -10 V to 10 V, the voltage step of 0.1 V. The capacitance-voltage (C-V) characteristics measured with 100 kHz are shown in Figure 3-12 for the 4H-SiC MOS

capacitors. The thickness was calculated from the accumulation capacitance of the C-V curves, which is good agreement with the T_{ox} determined by ellipsometer.

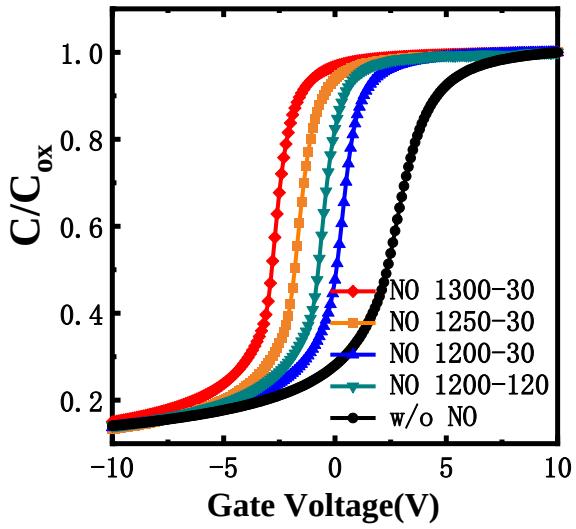

Figure 3-12. C-V characteristics of all the samples.

The thicknesses of the samples are calculated by the high frequency C-V measurement. The SiO_2 thickness of the samples is given by

$$T_{OX} = \frac{\varepsilon_0 \varepsilon_{SiO_2} A}{C_{ox}} \tag{3-3}$$

A is the area of the 4H-SiC MOS gate electrode, and ε_{SiO2} is the dielectric constant of SiO_2[18].

To analysis the reliability of the 4H-SiC MOS capacitors, time-zero dielectric breakdown (TZDB) measurements were performed at room temperature. During the TZDB measurement, a voltage was applied to the gate electrodes, step by +0.5 V until the gate oxide breakdown. The electric field (E_{BD}) used in this study is given by

$$E_{BD} = \frac{V_g - V_{FB}}{T_{ox}} \tag{3-4}$$

Where V_g is the gate voltage, V_{FB} is the flat band voltage, V_{FB} is also determined by high-frequency capacitance-voltage (C-V) characteristics. Then a constant-current stress a little less than breakdown voltage was applied to the gate oxide at 300 K to analysis the T_{BD} of the samples.

The Weibull distribution plots of charge-to-breakdown is extracted from constant-voltage TDDB measurement for thermal oxide. The time-dependent dielectric breakdown (TDDB) measurements were also performed at room temperature.

Figure 3-12 shows the high-frequency C-V of the samples using different NO annealing procedures, V_{FB} and T_{OX} estimated from the C-V characters in Figure 3-12. are summarized in Table III-II. From Figure 3-12, it can see NO annealing causing a negative shift of C-V curves. It indicates that the hole traps increase and the electron traps decreases in the thermal oxide with the increasing of annealing temperature and the extension of annealing time. The thickness of the samples unchanged essentially. The E_{BD} measured by TZDB is also in Table III-II.

Table III-II. Summary of Tox, V_{FB}, and E_{BD}

Label	Oxidation	Experiments and Results			
		NO Annealing	T_{OX} (nm)	V_{FB} (V)	E_{BD} (MV/cm)
w/o NO		/	60.12	3.5	9.386
NO1300-30		1300℃,30min	58.96	-2.03	10.09
NO1250-30	1350℃,20min	1250℃,30min	58.18	-0.667	9.825
NO1200-30		1200℃,30min	57.24	1.466	9.35
NO1200-120		1200℃,120min	59.46	0.698	9.635

Figure 3-13 shows the leakage current density-electric field (J-E) curves. The steepness of the five NO annealing samples is basically same. But the E_{BD} of the MOS capacitors annealing at 1300^{o}C is biggest 10.09 MV/cm, which indicates an increase in effective of the insulation performance by high temperature NO annealing. Compared the sample NO 1200-30 to NO 1200-120, it finds that extending annealing time also can improve the insulation of thermal oxide. But the improvement of E_{BD} did not significantly than the raising of temperature.

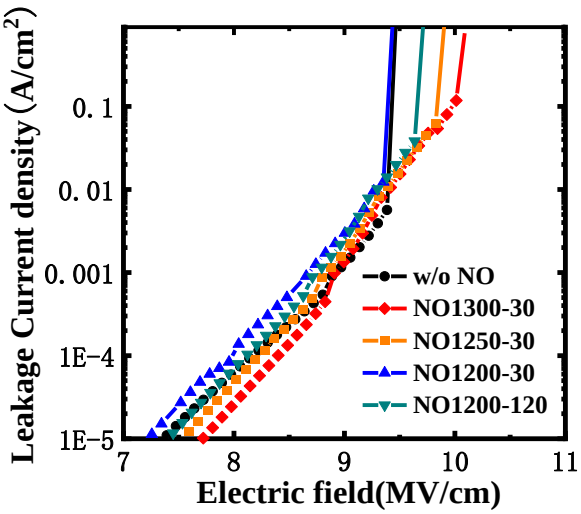

Figure 3-13. Typical J-E characteristics of five MOS samples

Figure 3-14 shows the Fowler-Nordheim plots, the effective barrier heights of the MOS-CAP were estimated from the F-N current plots. The effective barrier heights (Φ_B) is shown in Table III where m/m_0=0.42. The Φ_B of sample w/o NO is 2.358 eV, the samples after NO annealing get closed to the theoretical value between SiC and SiO_2 (2.7 eV), it indicates NO POA can enhance the insulation of the gate oxide film.

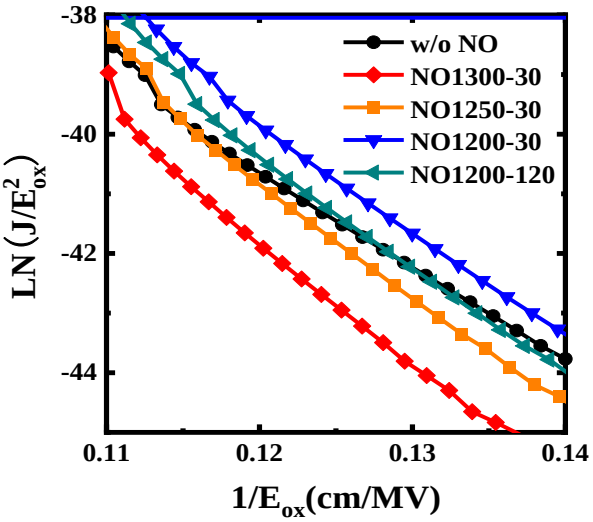

Figure 3-14. Fowler-Nordheim plots calculated by J-E curves

Figure 3-15 shows the TDDB measurement results of the NO annealing MOS-CAP. As shown in the Figure, the charge-to-breakdown (Q_{BD}) are 0.0408, 0.2223, 0.1218, 0.0575, 0.0475 C/cm^2 of the sample from w/o NO to NO1200-120, remarkable increase of Q_{BD} has

been achieved by the nitridation by NO. The sample NO 1300-30 shows the highest Q_{BD} value, which is 0.2223 C/cm^2 at 63.2% cumulative failure rate. But the sample NO1200-120 is 0.0475 C/cm^2. It indicates high temperature annealing can prove Q_{BD} obviously, it is good agreement with the TZDB results, which is also list in Table III-III.

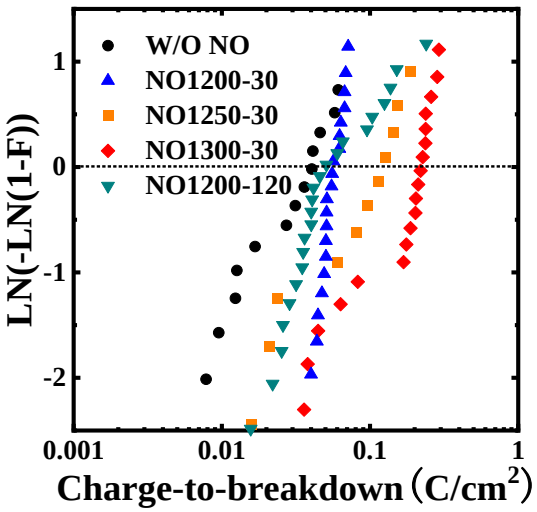

Figure 3-15. Weibull distribution of Q_{BD} obtained from TDDB measurement of five NO annealing samples

Table III-III summary of Φ_B and Q_{BD}

Label	Φ_B(eV)	Q_{BD}(C/cm^2)
w/o NO	2.358	0.0408
NO1300-30	2.740	0.2223
NO1250-30	2.655	0.1218
NO1200-30	2.610	0.0575
NO1200-120	2.676	0.0475

§3.2.4 Summary

In this article, it is revealed that the effects of NO annealing temperature and time on the reliability of 4H-SiC MOS gate oxide. And from the results of barrier height (Φ_B) and charge-to-breakdown (Q_{BD}), find it is effectively improving the insulation properties and reliability of gate oxide by higher temperature and longer times NO annealing. And from the study as shown in Figure 3-16 , it shown that annealing in higher temperature is an much more effective way to improve the reliability of 4H-SiC MOS gate oxide as compared to annealing in NO for long time.

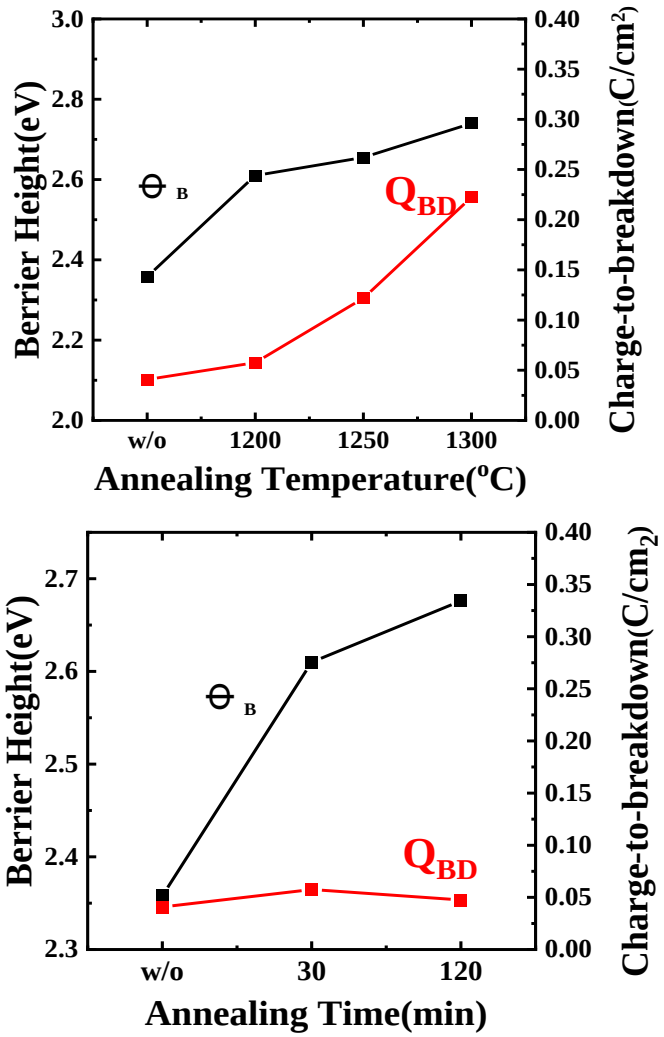

Figure 3-16. Dependence of nitridation temperature and time on barrier height and reliability

§3.3 References

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Chapter 4: Investigation on the Influence of Stress on Threshold Voltage, Interface State and Reliability

§ 4.1 Effect of Grinding-Induced Stress on Interface State Density of SiC/SiO_2

Gate oxide film on Silicon carbide (SiC) severely affects the performance of SiC metal-oxide-semiconductor field effect transistor (MOSFET). The authors investigated the influence of curvature induced stress/strain to flatband voltage (V_{fb}) and interface density (D_{it}) on SiO_2/SiC by Capacitance-voltage (C-V) measurement. The curvature of epitaxy wafers has been identified by the Thin Film Stress Measurement system. The compress/tensile curvature led to increase of the positive V_{fb} shift (negative fixed charge) of SiO_2 and the interface density of SiO_2/SiC during dry thermal oxidation process. In addition, the transverse optical (TO) phonon wavenumber of the samples related with the curvature of the film, indicating that stress mainly affected the interface of SiO_2/SiC. According to the experimental result, the authors suggested that a "free" stress oxide film might be a best choice for the application of SiC-MOSFET.

§4.1.1 Introduction

Wide band-gap materials have shown attracted interest due to the limitations of silicon for high power systems [1]. Silicon carbide (SiC) is an IV-IV wide band-gap material, which makes it higher breakdown field strength than those of many other power semiconductors. Therefore, SiC has higher doping concentration and thinner thicknesses of voltage blocking layer. The combinations of these properties make SiC devices remarkable because of lower on-resistances (R_{on}) [2]. For SiC metal oxide semiconductor field effect transistor (MOSFET) devices, especially low-voltage devices below 600V, grinding process is indispensable to make lower on-resistances due to the substrate resistance covers a large proportion [3]. Thus, a series of machining processes are indispensable to a pure SiC substrate, such as grinding, etching and Chemical Mechanical Polishing (CMP) [4]. However, there exist some problems due to the formation of damage layers after grinding process. For example, S. Tsukimoto et al. demonstrated that there exist damage layers on SiC surface layers of 0.6 μm after

grinding process, the strain distribution of the damage layers was investigated by electron back-scatter diffraction [5]. In addition, K. Shiraishi et al. Discussed the intrinsic problems of SiC/SiO_2 interfaces based on first principles calculations. The results clarified that stress free process is indispensable for high quality MOSFET [6]. However, more emphases have been placed on crystallography theory to explicate the issues of stress, but rarely were performed from the perspective of the electrical properties.

In this work, the effect of the 4H-SiC surface stress on interface state density of SiC/SiO_2 is proposed. We have carried out experiments by using two epitaxial wafers from the same manufacturer. The stress was characterized by warp and total thickness variation (TTV), the D_{it} was characterized using C-Ψ_s method, and the absorption of peak frequencies were observed by Fourier transform infrared spectroscopy attenuated total reflection (ATR-FTIR) analysis. The main purpose is to make a commercial guideline for the consideration of the grinding process of a SiC epitaxial wafer.

§4.1.2 Experiment

The experiment was carried out by using two 4^o-off-axis n-type 4H-SiC (0001) Si-face epitaxial wafers from the same manufacturer (sample A and sample B, $N_D = 8.0\times10^{15}\,cm^{-3}$). Table IV-I showed the initial information of two epitaxial wafers.

Table IV-I. The initial information of two epitaxial wafers.

Sample	Diameter [mm]	Thickness [μm]	Epi-film thickness [μm]	Doping [cm^{-3}]
A	100±0.5	350±25	12.27	8×10^{15}
B	100±0.5	230±25	12.65	8×10^{15}

Figure 4-1 illustrates the crucial steps of the experiment. By back-grinding process, the thickness of sample B was thinned from 350 ± 25 μm to 230 ± 25 μm using the SPEEDFAM 12B-5L. The warp and TTV were measured by FLX-2320-S. RCA cleaning process was to remove the organic contaminants, thin oxide layer, and ionic contamination. Dry oxygen oxidation had proceeded at a temperature of 1350^oC for 20 minutes, with the oxide thickness of about 60 nm. After oxidation, photolithography technology has been completed by Stepper 1755i7a. Aluminum was deposited with the thickness of 3000 Å as gate electrode and the thickness of 2000 Å for back electrode to form the MOS capacitor. Capacitance-voltage properties were measured by Agilent B1500 at room temperature with

the frequencies swept from 1 kHz to 1 MHz. The interface state density was analyzed based on the difference between theoretical capacitance and quasi-static capacitance (C-Ψ_s method). The absorption of peak frequencies was observed by ATR-FTIR method by the PerkinElmer - L1050022.

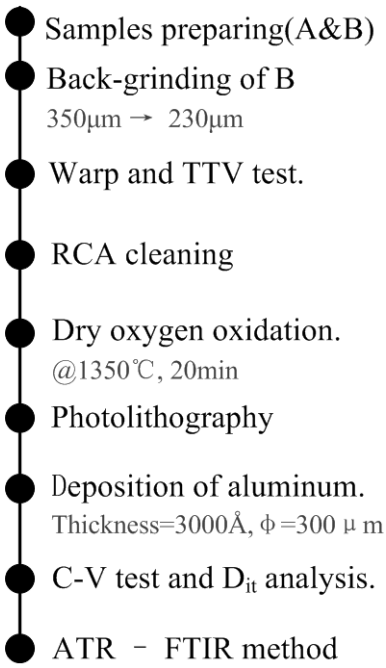

Figure 4-1. The key process flows of the experiment, including the formation of MOS capacitor and corresponding test.

§4.1.3 Results and Discussion

Table VI-II tabulates the information of these two epitaxial wafers before (sample A) and after (sample B) the back-grinding process. The parameters of the characterization of stress consist of warp and TTV. The warp is the difference between the maximum and minimum values of the median surface of a free, unclamped wafer from a reference. TTV is the difference between maximum and minimum thickness values encountered during a series of point's measurements within the wafer area [7]. After back-grinding process of the sample B, the value of warp rises from 16 μm to 57 μm and the value of TTV rise from 3 μm to 21 μm. These results suggest that the values of TTV and warp are more than 3 times higher than those before grinding process, which means that the stress increase evidently after grinding process.

Changes in the thickness of the SiC material will cause the material to deform, as shown in Figure 4-2, the deformation of the SiC material at 350 μm and 230 μm ,

respectively. The form shows the deformation before thinning.

Table IV-II. The results of stress before and after grinding by Tropel FM100 analysis.

Sample	Initial		After grinding	
	Warp[μm]	TTV[μm]	Warp[μm]	TTV[μm]
A	11.277	2.268	/	/
B	14.026	2.891	57.001	21.225

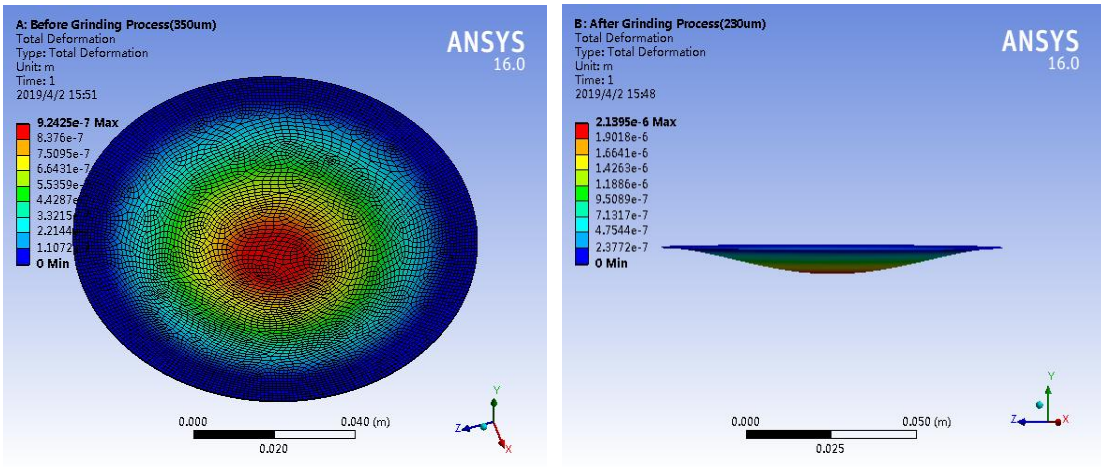

Figure 4-2. Deformation of SiC before thinning (350 um) and after thinning (230 um)

According to the above Figure 4-2 (left), the maximum shape corresponding to the SiC material before thinning (350 um) becomes 0.942 um, and Figure 4-2 (right) after thinning (230 um) shows the maximum shape of the sample in the form of longitudinal distribution the variable is 2.139 um, which shows that the thinning process can lead to an increase in the deformation of the sample, that is, the warpage of the sample increases.

Similarly, the change in the thickness of the SiC material will cause the stress of the material to change. As shown in Figure 4-3, the stress distribution on the surface of the sample and the longitudinal stress distribution before and after the thinning of SiC from 350 um to 230 μm, respectively. The stress at the edge of the SiC epitaxial wafer is relatively large, the maximum stress before thinning is about 1.57×10^5 Pa, and the value of the stress after thinning increases to about 2.40×10^5 Pa, which shows that the thinning process will As a result of the increase in stress value, the stress value increases approximately 1.53 times comparing with the original stress value without considering external forces.

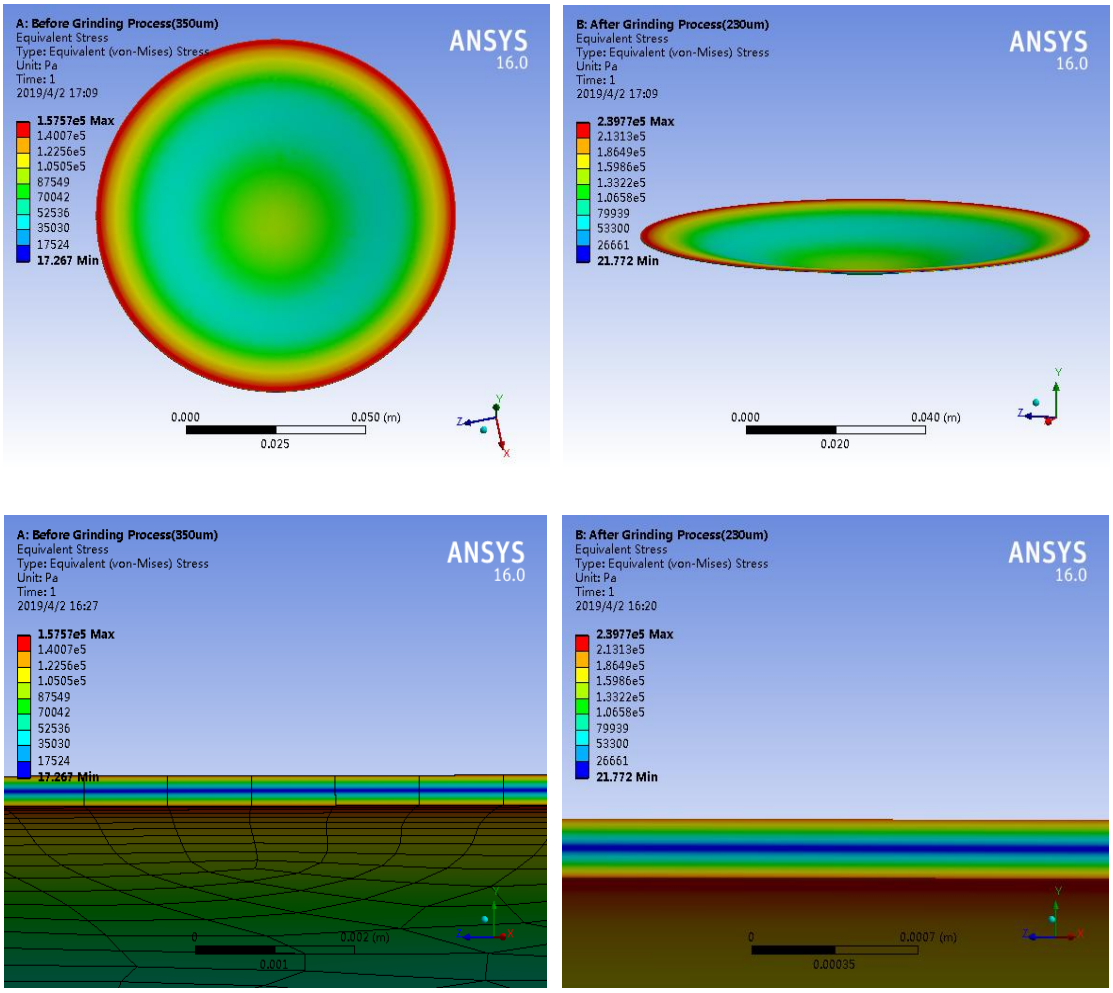

Figure 4-3. Stress distribution before SiC thinning (350 um) and after thinning (230 um)

Interface quality is evaluated by interface state density, which can be estimated by high-low frequency C-V measurement or conductance method with the frequency from 1 kHz to 1MHz [8-9]. H.Yoshioka et al. proposed a modified theory named C-Ψ_s method based on the quasi static and theoretical capacitance. The interface state density using C-Ψ_s method is given by [10]

$$D_{it} = \frac{(C_d + C_{it})_{QS} - C_{d,theory}}{Aq^2} \qquad (4\text{-}1)$$

Where C_d and C_{it} is the semiconductor capacitance and the interface-state capacitance, $(C_d+C_{it})QS$ is the (C_d+C_{it}) measured under the quasi-static conditions, the $C_{d,theory}$ is the theoretical semiconductor capacitance, A (7.065×10^{-4} cm^{-2}) is the area of gate electrode, and q is the electric charge. Measurements were carried out at room temperature. The frequencies were from 1 kHz to 1 MHz Gate voltage was swept from depletion region to accumulation region at a voltage-sweep rate of 200 mV/s. Figure 4-4,4-5 shows the C-V and interface state

density distribution of the sample A and the sample B. It is noted that the D_{it} of sample B is higher than that of sample A. This result suggests that the interface state density would increase after back-grinding process.

In order to further validate the effect of stress on D_{it} of SiC/SiO_2 qualitatively, Fourier transform infrared spectroscopy attenuated total reflection was performed. ATR-FTIR is a effective method to analyze microscopic properties of substrates and films of SiO_2 [11]. The ATR-FTIR measurements were carried at room temperature and under vacuum condition. The resolution was set to 4 cm^{-1}, and the wave number region from 1000 to 1300 cm-1. With the incidence angle of 45 °, a three-time reflection system on a single-crystalline ZnSe prism was employed. Figure 4-7 illustrates the absorption of peak frequencies of the samples. The results showed that the absorption rate of sample B is higher than that of sample A, which means that the surface roughness of sample B is greater. Thus, we can conclude that the interface density of sample B is greater than sample A. This result is consistent with above quantitative analysis.

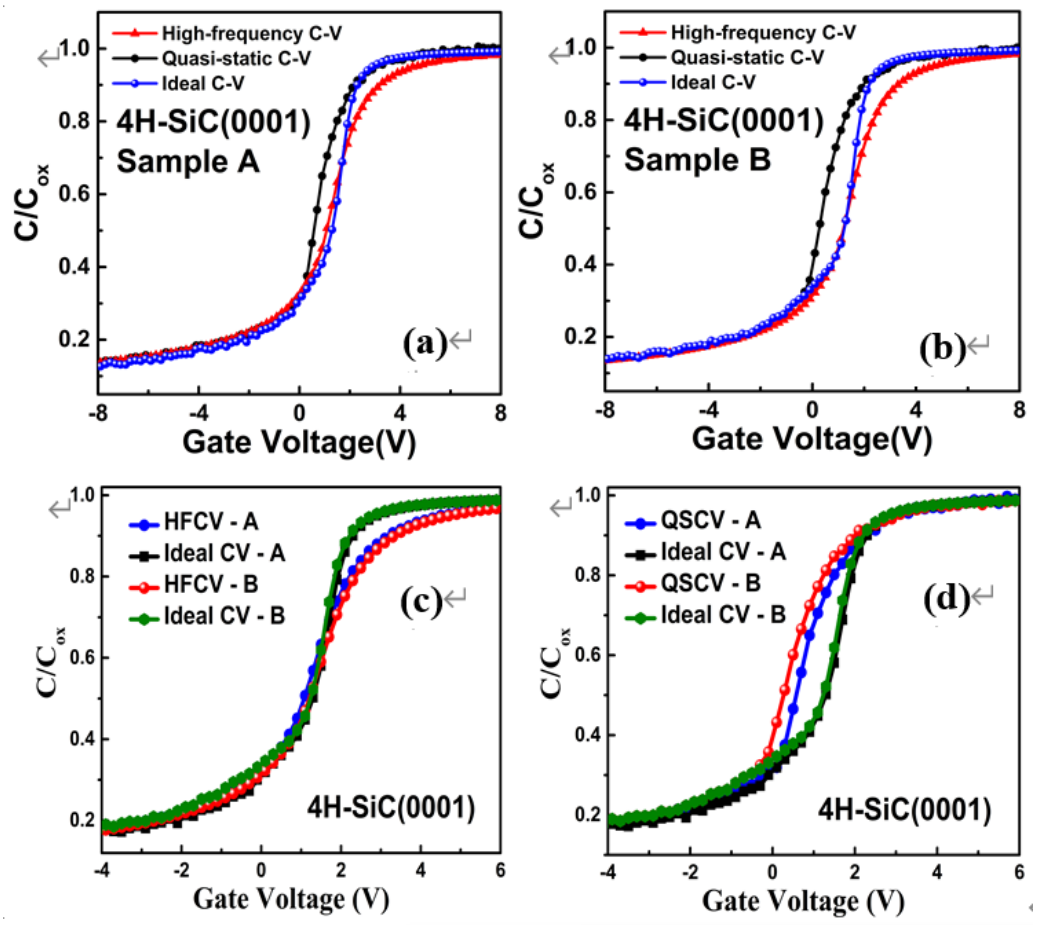

Figure 4-4. The C-V characters of the samples.

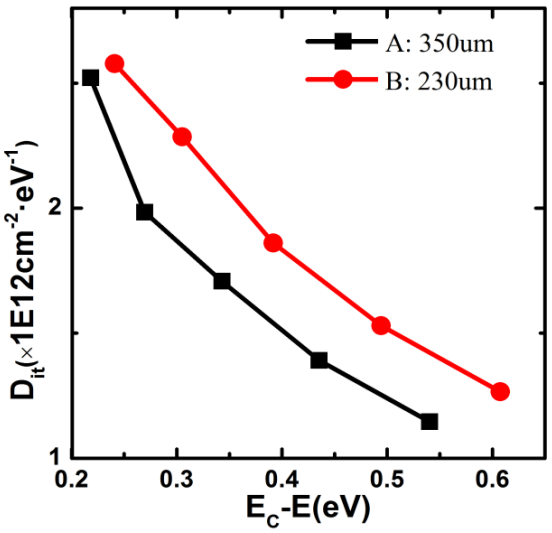

Figure 4-5. The interface state density of SiC/SiO_2 versus E_c-E.

The D_{it} of sample B is higher than that of sample A.

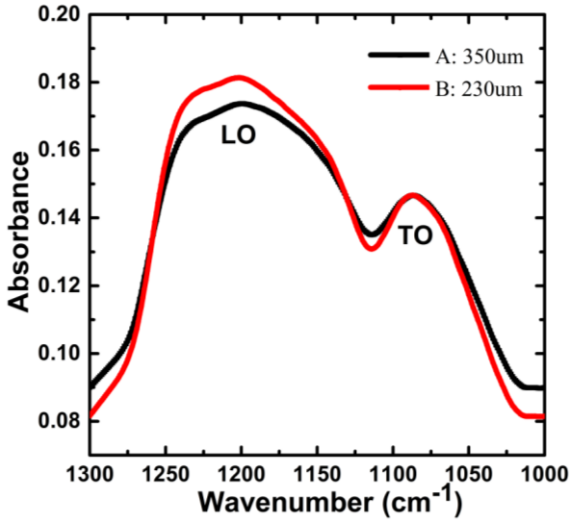

Figure 4-7. The ATR-FTIR analysis results.

§4.1.4 Conclusion

The effect of grinding-induced stress on interface state density of SiC/SiO_2 was investigated. It is found that the parameters of stress increased by three times after grinding process, and there is a small increment of the interface state density. These results suggest that the interface state density of SiC/SiO_2 increases with the grinding-induced increasing stress. Therefore, the grinding process of SiC epitaxial wafer should be regarded with some care.

§ 4.2 Influence of Curvature Induced Stress to the Flatband Voltage and Interface Density on 4H-SiC MOS Structure

Gate oxide film on Silicon carbide (SiC) severely affects the performance of SiC metal-oxide semiconductor field effect transistor (MOSFET). The authors investigated the influence of curvature induced stress/strain to flat-band voltage (V_{fb}) and interface density (D_{it}) on SiO_2/SiC by Capacitance-voltage (C-V) measurement. The curvature of epitaxy wafers has been identified by the Thin Film Stress Measurement system. The compress/tensile curvature led to increase of the positive V_{fb} shift (negative fixed charge) of SiO_2 and the interface density of SiO_2/SiC during dry thermal oxidation process. In addition, the transverse optical (TO) phonon wave number of the samples related with the curvature of the film, indicating that stress mainly affected the interface of SiO_2/SiC. According to the experimental result, the authors suggested that a "free" stress oxide film might be a best choice for the application of SiC-MOSFET.

§ 4.2.1 Introduction

For a long time, SiC has been thought as one of the most suitable power device material for high-power and high-temperature electronics due to its high critical (breakdown) electric field strength and high thermal conductivity. Additionally, SiC is attractive because, like Si, its native oxide is SiO_2, so that we can employ the thermal oxidation technical to form a SiO_2 layer as gate insulator for a MOSFET having a SiO_2/SiC interface. However, different from the ideal SiO_2/Si interface, SiO_2/SiC interfaces formed by thermal oxidation of SiC contain many interface trap sites, which is the most critical limitation of the channel mobility of MOSFET.

The interface of SiO_2/SiC has been improved to some extent by performing certain processes, such as higher temperature oxidation [12] and NO post-oxidation annealing [13]. However, it is unclear how the interface traps are passivated by nitridation [2]. Recently, an ex-situ and in-situ experiment suggested that physical stress in SiO_2/SiC stacks formed by the thermal oxidation of SiC [14]. Furthermore, a near-interface oxides at thermally grown SiO_2/SiC interfaces is investigated using infrared spectroscopy demonstrated that a strong correlation between the stress of near-interface oxides and the formation of near-interface oxide traps [15].

To find out the physical origin of the correlation between poor SiO_2/SiC interface traps and the oxidation processes, a first-principle calculation is discussed that the stress at SiO_2/SiC interface during the thermal oxidation of SiC is critical for understanding the formation of the interface defects [16]. However, the experiment results of SiO_2/SiC interface density on the physical stress have not yet been clarified. In this study, we report here an investigation of stress in SiO_2/SiC structures, formed by dry-O_2 oxidation, especially paying attention to the shift of flat-band voltage from C-V measurement and interface density with C-ψ_s method [10].

§4.2.2 Experiment

4-inch SiC full wafers were selected to the experiment, which were sufficiently large (>2-inch) to measured curvature caused by stress. 4°-off-axis n-type 4H-SiC (0001) Si-face substrates with a 12 μm n-type epitaxial layer doped with nitrogen at the effective carrier density (N_d-N_a) $8\times10^{15}cm^{-3}$ were used to fabricate MOS capacitors. The radius of curvature (R) of the samples were measured by a Thin Film Stress Measurement system, FLX-2320-S. The curvatures of the selected tensile samples A and B curvature of -0.0132 and -0.0091 (1/m), respectively. Boron ions were implanted at a fixed energy (110 keV) and different doses into the (000-1) C-face, back side, of sample C and D at room temperature. After Boron implanting, we noticed that the implanted samples C and D become to compress, which were tensile in the initial stage.

Sample C was implanted with an energy of 110 keV and a dose of 1×10^{16} cm^{-3}, and sample D was implanted with an energy of 110 keV and a dose of 5×10^{15} cm^{-3}. Figure 4-8 shows the map of the stress distribution on the surface of the SiC material before and after ion implantation. The results show that there is a significant change in the stress distribution of the SiC material after ion implantation.

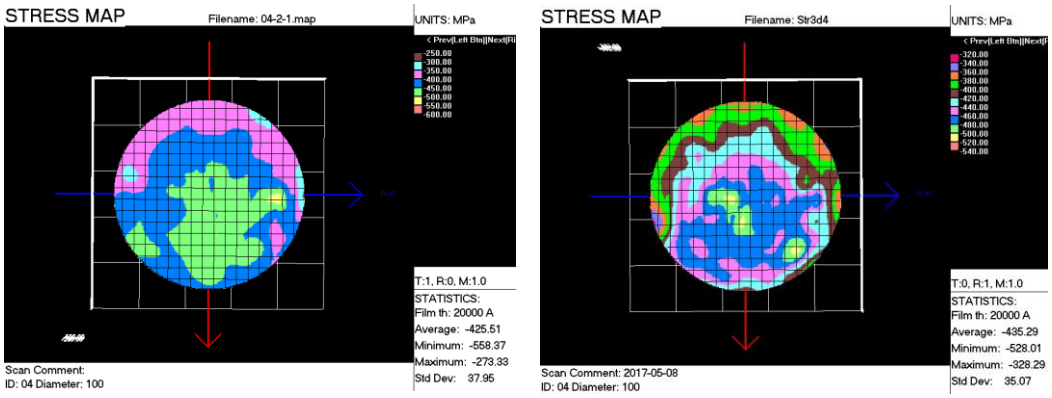

Figure 4-8. Surface stress distribution of SiC before and after boron ion implantation on the back

For different doses of ion implantation, the degree of change of the strain corresponding to the sample is also different. Table VI-III shows the corresponding relationship between the radius of curvature and the stress / strain. From this, it can be seen that the sample A initially receives a small tensile stress after a large dose After the ion implantation, the sample is converted into the sample C under less compressive stress, while the sample B is subjected to a larger initial tensile stress and converted into a sample D under greater compressive stress after a small dose of ion implantation.

Table IV-III. Boron Implantation Dose, Curvature and stress of samples

Sample	Implantation Dose(cm^{-2})	Curvature (1/m)	Stress/Strain
A	w/o	-0.0132	tensile--
B	w/o	-0.0091	tensile-
C	1.0×10^{16}	0.0262	compress+
D	5.0×10^{15}	0.0783	compress++

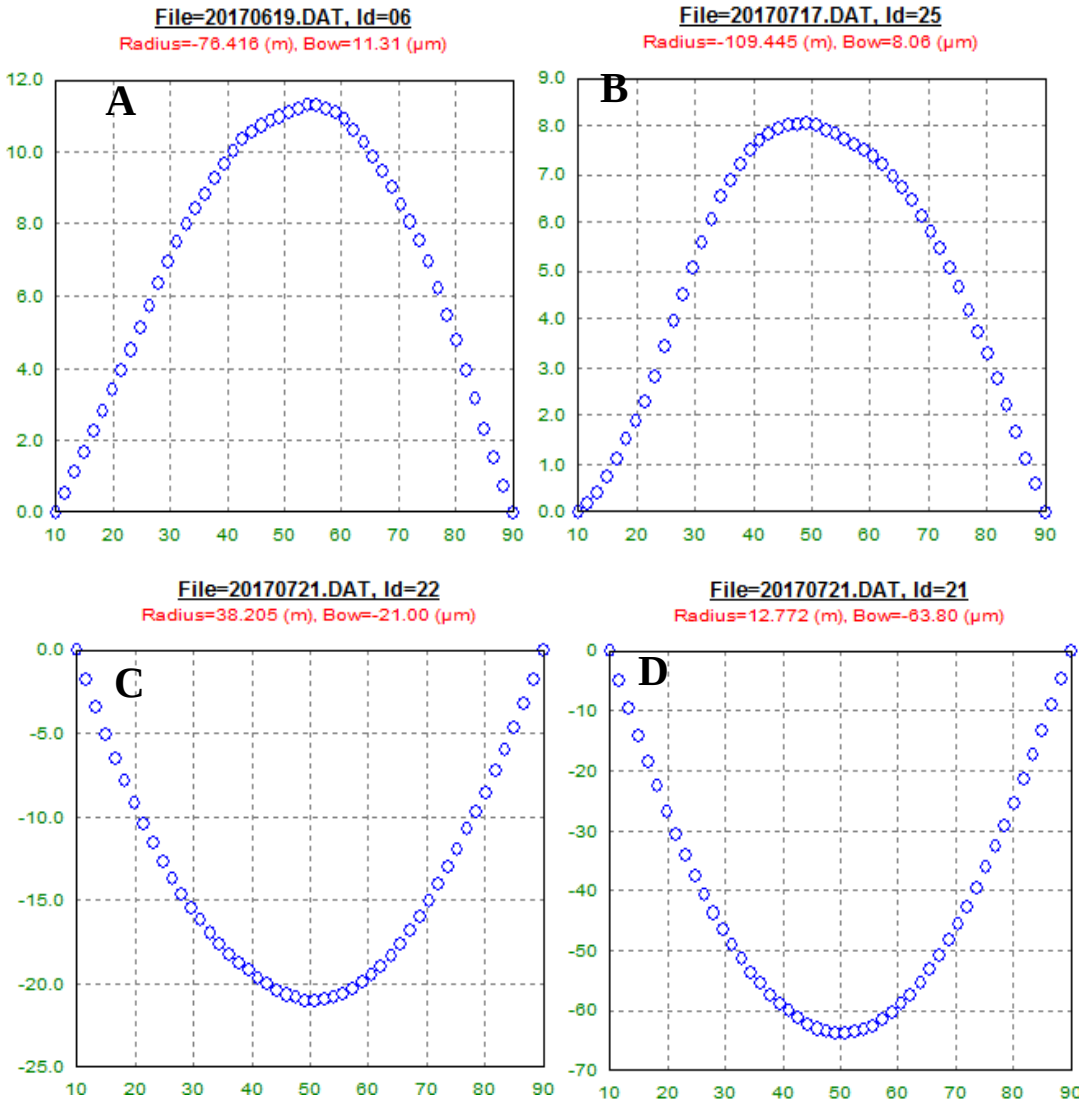

Figure 4-9. Stress state changes before and after boron ion implantation on the backside

Figure 4-9 shows the relationship between stress and curvature and warpage. From the analysis of Figure 4-9 (a) and 4-9 (b), it can be seen that the value of stress will increase approximately linearly with the increase of curvature and warpage. Figure 4-9 (c) and 4-9 (d) show that the stress value has a negative correlation with bow and radius.

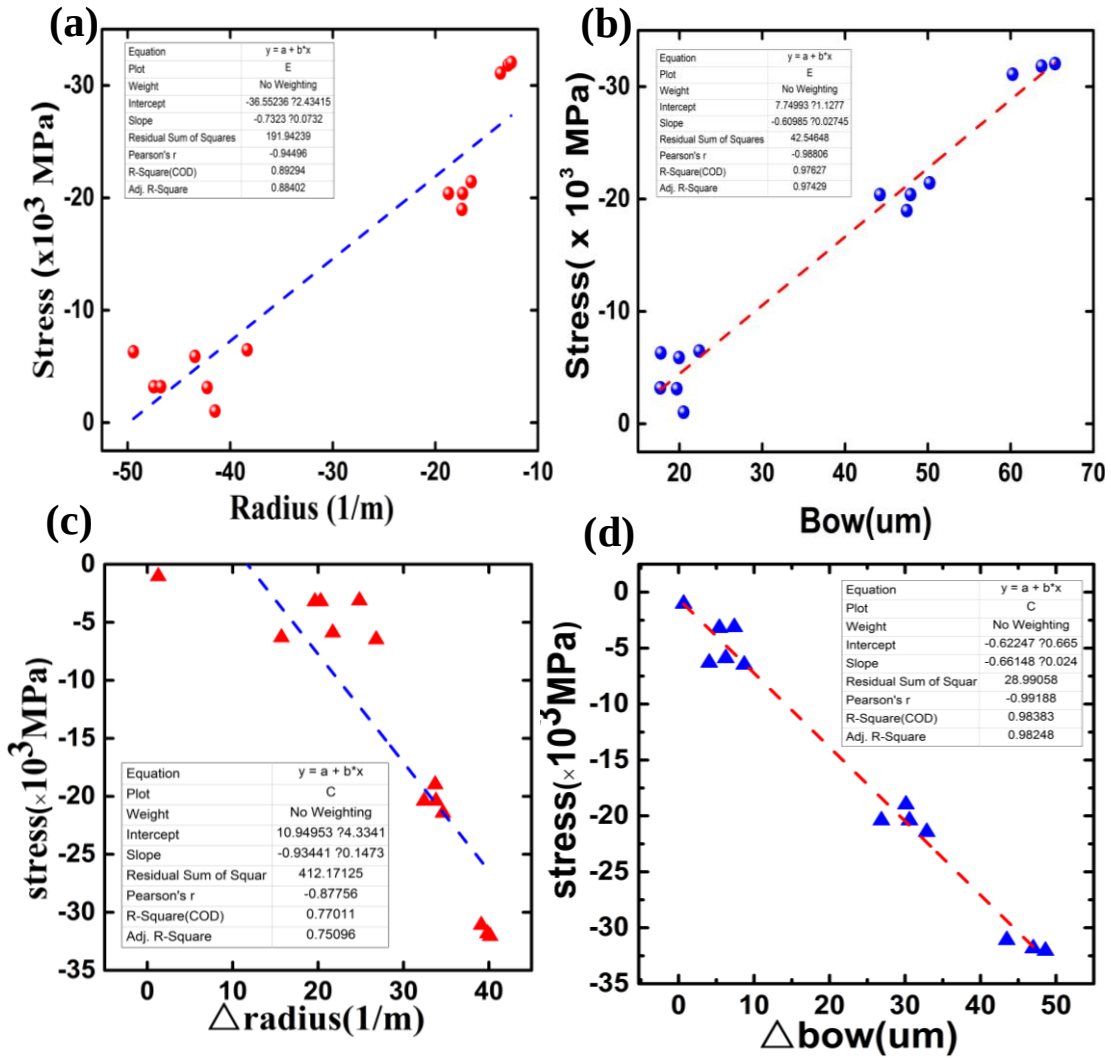

Figure 4-10. Relationship between stress value and radius and bow

The standard Radio Corporation of America (RCA) cleaning process was performed to remove native oxides and other impurities on the surface of the samples prior to loading samples into furnace. Subsequently these samples underwent dry oxidation at 1150°C for 2 h in O_2 and then were cooled to room temperature. After oxidation, Al was sputtered on the backside after HF cleaning and anti-sputtering. Finally, Al circular electrodes (ø=300μm) were also evaporated as top-contact to form the MOS capacitors. C-V measurements were performed using an Agilent B1500A in a shielded dark box at room temperature.

§4.2.3 Measurement and Discussion

Figure 4-11 shows the C-V characteristics of sample A. The high frequency C-V characteristics were measured at f=100 kHz with a small signal amplitude of 30 mV and the quasi-static C-V were measured at the sweep rate of ramp voltage 50 mV/s. According to the (Quasi-Static Capacitance-Voltage) QSCV and the high frequency C-V curve, the ideal C-V curve was calculated from Poisson's equation, as shown in Figure 4-11.

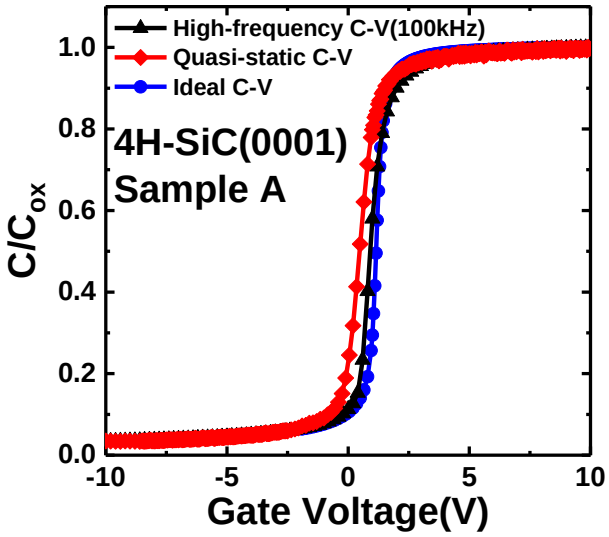

Figure 4-11. C-V characteristics of n-type 4H-SiC (0001) MOS capacitor.

The flat-band voltage (V_{fb}) of tensile (sample A and B) and compress (sample C and D) samples was estimated from the 100 kHz high-frequency C-V characteristics. As shown in Figure 4-12, a positive V_{fb} shift voltage was obtained for the tensile samples (A and B), indicates that negative fixed charge appears during dry oxidation. These results coincide well with those obtained in a previous dry oxidation study [17]. Even though it is also reported a negative V_{fb} instability during wet oxidation proton act as positively charge mobile ions [18].

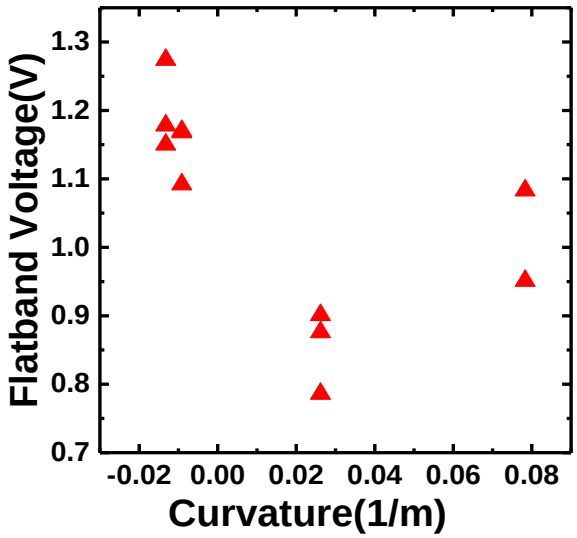

Figure 4-12. The relationship between curvature and V_{fb}.

We also notice that the compress stress before oxidation affect greatly the V_{fb} and that the V_{fb} of sample C is close to the ideal value. These results imply that relieving the tensile stress can restrict the generation of negative fixed charges. The large V_{fb} of tensile sample might be attributed to the large number of electrons traps at the interface [19]. On the contrary, the V_{fb} of sample D shifts back to a positive value, which means the non-negligible negative charges exist at the SiO_2/SiC interface or in SiO_2 again.

We evaluate the interface state density by the C-Ψ_s method [10]. The value of D_{it} were expressed as follows:

$$D_{it}(C-\varphi_S)=\frac{C_{ox}}{q}\left(\frac{C_{QS}}{C_{OX}-C_{QS}}-\frac{C_{Ideal}}{C_{OX}-C_{Ideal}}\right) \tag{4-2}$$

Where q is the electronic charge, C_{QS}, C_{ideal}, and C_{ox} are the quasi-static, ideal, and oxide capacitance per area, respectively. The results of interface state density (D_{it}) are shown in Figure 4-13 as a function of energy level, with reference to the conduction band edge of 4H-SiC. The values of D_{it} at E_c-E=0.2eV of sample C is 3.01×10^{12} eV^{-1} cm^{-2}, which is approximately on one third of that of the sample A. Therefore, it is clear that tensile stress relieved by ion implantation is effective for reduction of D_{it} and V_{fb} discussed above. However, it should be noted that the C-V characteristics and D_{it} of bigger compress sample B is larger than C, although the curvature quality before C-face ion implantation are similar. Therefore, extreme compress stress would be another reason for the increase of D_{it}.

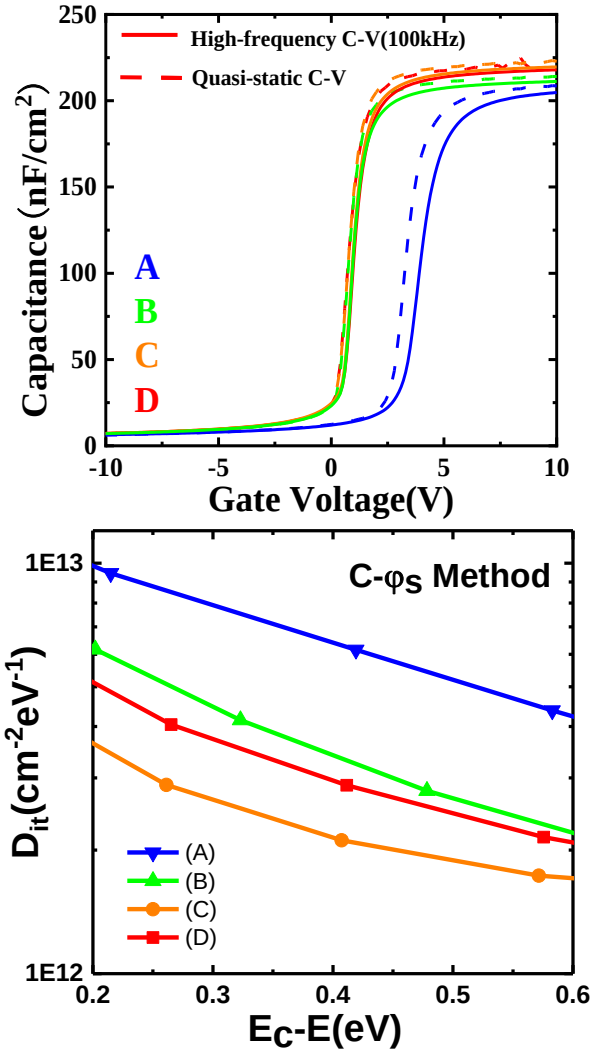

Figure 4-13. Interface defect state density (Dit) as a function of energy level below the conduction band of SiC, estimated by the C-ψ_s method, measured at room temperature.

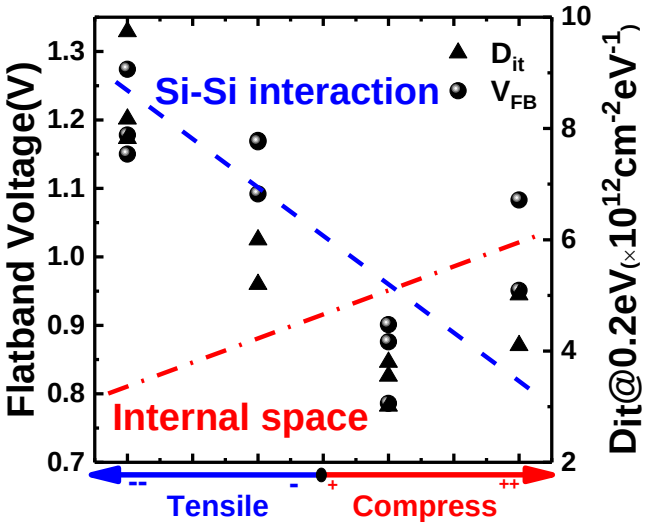

Figure 4-14 shows the relationship between tensile/compress stress and D_{it}.

This result reveals that D_{it} decreases as the release of tensile stress and increases along with the compress stress increases. Therefore, the reduction of D_{it} was thought to be caused by the termination of implantation relieved tensile/compress stress. We are assuming two reason caused defects. Firstly, a Si-Si interaction defects caused by 2nd nearest neighbor Si-Si atom [2]. The tensile stress leads an expand of the Si-C bond, so that the oxygen atom easier insert to the bonds, which lead to the formation of interface states near conduction band bottoms.

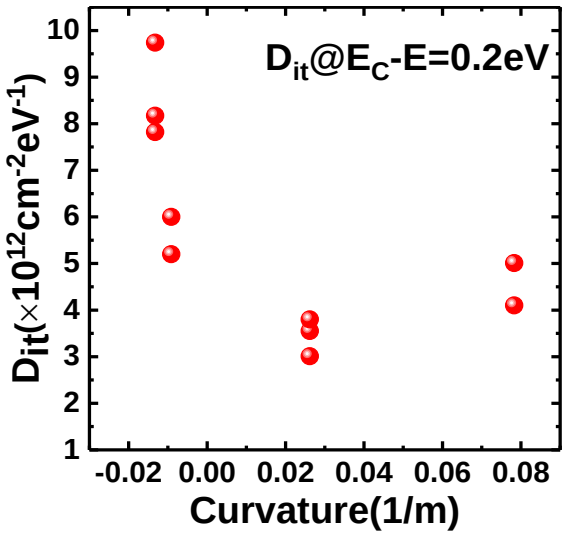

Figure 4-15. The relationship between curvature and D_{it} @E_c-E=0.2eV

To unveil the mechanism of the results, a Fourier transform infrared (FTIR) spectroscopy for stress characterization had been performed. We employed FTIR attenuated total reflection (ATR), which has also been applied for studies on microscopic structures of thermally grown oxides on SiC [20-21], to analyze the stress of SiO_2. The ATR measurements were carried out on a single reflection system and a single-crystalline ZnSe prism with the incidence angle of 45^o was employed on Varian Excalibur 3100. As shown in Figure 4-16, the dominant features in these spectra are the TO and LO modes arising from asymmetric Si-O stretching motions of the constituent SiO_4 tetrahedra.

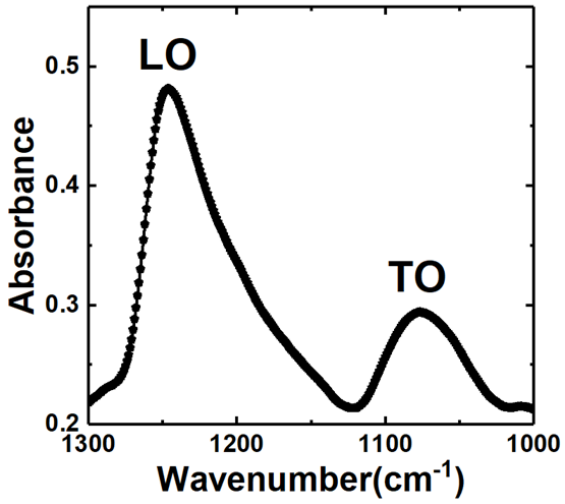

Figure 4-16. Infrared spectra of thermally grown SiO_2.

As shown in Figure 4-17, the wavenumber of the LO phonon in the sample A (tensile--) and B (tensile-) was observed at around 1300 cm^{-1} and red-shifted approximately to 1258 cm^{-1} relative to the compress samples C, whereas the deeper compress sample D (compress^{++}) was increased back to 1300 cm^{-1}. It is known that LO phonon wavenumber red-shifts are caused by two possible factors: change of stoichiometry (SiO_x) and decrease of Si-O-Si bond angle [22], which indicating a lowest stress in sample C led to a best-behaved V_{fb} and D_{it} behaved.

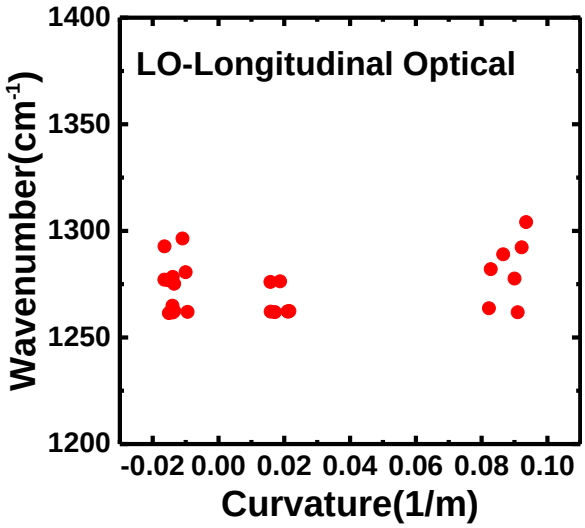

Figure 4-17. Change of LO wavenumbers with curvature.

§4.2.4 Summary

In conclusion, the flatband voltage (fixed charge) and interface density of SiO_2/SiC has been studied by C-V measurement. The curvature of epitaxy wafers has been identified by the Thin Film Stress Measurement system. The compress/tensile curvature led to increase of the positive V_{fb} shift (negative fixed charge) of SiO_2 and the interface density of SiO_2/SiC during dry thermal oxidation process. In addition, the TO peak frequency of the samples related with the curvature of the film, indicating that stress mainly affected the interface of SiO_2/SiC. The results are thought to be important for the industrial application of SiC and SiC-based devices on the practical epitaxy wafer selection.

§4.3 Influence of Curvature Induced Stress on First Principle Calculation and the Reliability on 4H-SiC (0001) Thermally Grown SiO_2 Gate Oxide

The effect of biaxial strain on the band gap of SiO_2/4H-SiC (0001) was studied by first-principles calculation. It is found that the compressive and tensile strains lead to a change in the band gap of SiO_2/4H-SiC (0001), where the structure at 2% compression is the equilibrium state of the strain structure. The size of the band gap is mainly affected by the O-2p state in SiO_2 and the C-2p and Si-3p states in SiC. Therefore, the value of E_g can be adjusted by strain. The smaller the tensile, the larger the E_g, the smaller the interface state. The larger the compression, the smaller the E_g, and the larger the interface state. At the same degree of bending, the compression is greater than the E_g of the tensile. These results indicate that the strain method can be used to adjust the band gap of SiO_2/4H-SiC, thereby changing the interface state. On the other hands, gate oxide films on silicon carbide (SiC) markedly affect the performance of SiC metal-oxide-semiconductor field effect transistors (MOSFETs). We used current-voltage (I-V) measurements to investigate the influence of curvature induced stress/strain on the breakdown electric field and the charge-to-breakdown (Q_{BD}) at SiO_2/SiC, defined here as time-zero dielectric breakdown and time-dependent dielectric breakdown, respectively. The curvature of the epitaxy wafers was characterized by a thin film stress measurement system. The compression/tensile curvature decreased E_{BD} and Q_{BD} during the dry thermal oxidation process. Furthermore, first-principle calculations suggested that the energy levels of the samples were related to the lattice constants of the SiC crystal, indicating that stress mainly affected the SiO_2/SiC interface. We suggest that a "stress free" oxide film might be the best choice for SiC-MOSFET applications.

§4.3.1 Introduction

Silicon carbide (SiC) is considered to be the most suitable material for power devices applied in high-power and high-temperature electronics owing to its high critical (breakdown) electric field strength and high thermal conductivity. Additionally, SiC is attractive because, like Si, its native oxide is SiO_2, enabling thermal oxidation to form a SiO_2 layer as gate insulator for metal-oxide-semiconductor field effect transistors (MOSFETs) having a SiO_2/SiC interface. However, unlike ideal SiO_2/Si interfaces, SiO_2/SiC interfaces formed by thermal oxidation of SiC contain many interfacial trap sites, which not only reduce the channel

mobility of SiC-MOSFETs but also decrease the performance reliability.

The interface of SiO_2/SiC can be improved to some extent by performing certain processes, such as high-temperature oxidation [12] and NO post-oxidation annealing [13]. However, it is unclear how interfacial traps are passivated by nitridation [2]. Recently, ex situ and in situ experiments have suggested that physical stress accumulates in SiO_2/SiC stacks formed by the thermal oxidation of SiC [16]. Furthermore, investigations of near-interface oxides at thermally grown SiO_2/SiC interfaces by infrared spectroscopy have shown a strong correlation between the stress of near-interface oxides and the formation of near-interface oxide traps [15].

To find out the physical origin of the correlation between poor SiO_2/SiC interface traps and the oxidation processes, a first-principle calculation is discussed that the stress at SiO_2/SiC interface. The calculation showed the stress induced during the thermal oxidation, the results of calculation is critical to understanding the formation of the SiO_2/SiC interface defects [22]. The experiment results of SiO_2/SiC interface density on the physical stress have not yet been clarified.

The compressive/tensile curvature is thought to increase the positive V_{fb}-shift (negative fixed charge) of SiO_2 and the interface density of SiO_2/SiC during dry thermal oxidation process, [23] indicating that stress mainly affects the SiO_2/SiC interface. In previous reports, the lowest interface state density was obtained for an oxide formed at a curvature of 0.0262 1/m, the lowest stress/strain. However, the reliability, such as the electric field (E_{BD}) and the charge-to-breakdown (Q_{BD}) of thermal oxide SiO_2, has not been investigated.

To realize SiC based MOS devices, it is important that high quality gate oxide can be fabricated. Since the relative positions between the atoms affect the band structure, the lattice mismatch of the heterostructure causes strain generation, and the band gap (E_g) can be adjusted the desired structural and electronic properties can be obtained. This lattice mismatch can result in biaxial strain in the (0001) plane or uniaxial strain in the [0001] direction. At present, based on density functional theory (DFT), the band gap modulation of strain method has been studied in SiC structures [23, 24].

In this study, since in DFT, local density approximation (LDA) or generalized gradient approximation (GGA) tends to seriously underestimate the band gap of semiconductors due to the self-interaction errors inherent in local processing. The Heyd-Scuseria-Ernzerhof (HSE06) mixing function is very close to the experimental value in calculating the Eg of a semiconductor [25]. For example, in our calculations, the unstrained 4H-SiC has an E_g of 3.2 eV which is very close to the experimental value of 3.3 eV. However, if the GGA-Perdew-Burke-Ernzerhof (PBE) method is used, the E_g is only 2.24 eV. Therefore, in this paper, we use the HSE06 mixing function in the first-principles calculation to study the effect of the biaxial strain parallel to the (0001) plane on the band gap of the SiO_2/4H-SiC structure.

We also investigated the effects of stress in SiO_2/SiC structures, formed by dry-O_2 oxidation, paying close attention to the E_{BD} and the Q_{BD} at the SiO_2/SiC interface by I-V measurements, namely, time-zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB), respectively.

In this study, all calculation is performed the first principle study by the Vienna Ab initio Simulation Package Code (VASP), which is based on the density function theory [8]. And the structural relaxation was performed under the GGA using exchange-correlation given by PBE scheme [26]. The electronic structures of bulk SiC and SiO_2 were determined through the HSE06 hybrid functional [27]. The parameter AEXX uses 40%. We used Projector-Augmented Wave (PAW) potential with the cutoff energy of plane-waves used in the calculation was 550 eV. The geometry relaxations and electronic structure calculations were performed applying the 6×3×1 k-points meshes using the Monkhorst-Pack scheme. When structural relaxation and calculations are performed, it stops until all Feynman-Hellmann forces are less than 0.02 eV / Å.

We modeled a supercell composed of 6 bilayers of 4H-SiC (1×√3) and 10 Å thick of β-tridymite SiO_2. The single crystal cell structure of 4H-SiC and SiO_2 is shown in Figure 4-18(a) and (b) respectively. An interface is formed on the 4H-SiC (0001) plane and the Si surface of 4H-SiC is in contact with the oxygen atom of SiO_2. Both the top and bottom layers of the model are H terminated and that for the entire structure contains 43 atoms. In addition, the slabs were separated by a vacuum layer more than 15 Å thick. In our

calculations, a stress of -5% to 5% is applied to the biaxial strain parallel to the (0001) plane. Then, the bottom H atom and the three 4H-SiC bilayers remain fixed, and all remaining atoms are relaxed to complete the optimization of SiO_2/4H-SiC and its strain structure. The degree of biaxial strain is defined as $\varepsilon = (a-a_0)/a_0 \times 100\%$, where a_0 *(a)* denote the lattice constants of the equilibrium (strained) crystal. $E>0$ ($\varepsilon<0$) signifies the tensile (compressive) strain.

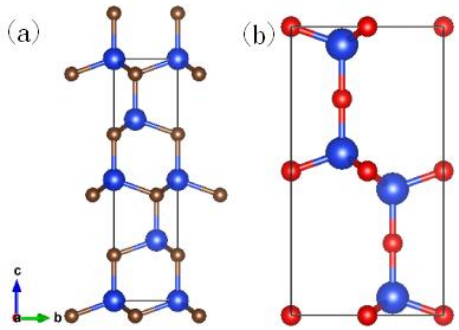

Figure 4-18. The single crystal structure of (a) 4H-SiC and (b) SiO_2. The blue, red, and pink circles are Si, O, and C atoms, respectively.

We compare the calculation results of this paper, previous experimental values and other calculation methods to obtain the lattice constants a_0, c_0 and E_g of 4H-SiC, as shown in Table IV-IV. It can be seen that there is good agreement between our calculation results and the theoretical data of previous experiments, which indicates that the calculation method used is reasonable. Figure 4-19 shows the SiO_2/4H-SiC (0001) structure in the stress-free state of this study, which has been relaxed. On the basis of this, a stress of -5% to +5% is simultaneously applied to the *a*-axis and the *b*-axis (biaxial) of the SiO_2/4H-SiC (0001) structure.

Table IV-IV. The lattice constants a_0, c_0 and E_g of 4H-SiC obtained in the calculation results herein, previous experimental values and other calculation methods.

	Calculated	Experimental	Other theoretical
a_0 (Å)	3.094	3.073	3.082
c_0 (Å)	10.14	10.125	10.095
E_g (eV)	3.2	3.3	2.24

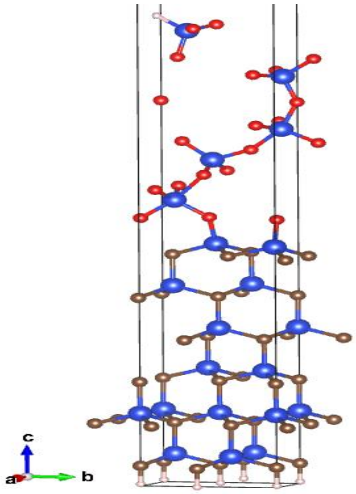

Figure 4-19. The supercell structures of the SiO_2/4H-SiC(0001) in the stress-free state. The blue, red, pink, and brown circles are Si, O, H, and C atoms, respectively.

§4.3.2 Experiment method

We selected 4-inch SiC full wafers for the experiments, which were sufficiently large (>2-inch) to allow the curvature caused by stress to be measured. The 4°-off-axis n-type 4H-SiC (0001) Si-face substrates with a 12 μm n-type epitaxial layer doped with nitrogen at an effective carrier density (N_d-N_a) 8×10^{15} cm^{-3} were used to fabricate MOS capacitors. The radius of curvature ® of the samples was measured by a thin film stress measurement system (FLX-2320-S). The curvatures of the selected tensile samples A and B were −0.0132 and −0.0091 (1/m), respectively. Boron ions were implanted at a fixed energy (110 keV) and at different doses into the $(000\bar{1})$ C-face/back side, of samples C and D at room temperature. After boron implantation, we noticed that the implanted samples C and D were compressed, which indicated an initial tension (see Table IV-V).

Table IV-V. Boron implantation dose, curvature, and stress of samples.

Sample	Implantation Dose (cm^{-2})	Radius （m）	Curvature (1/m)	Stress /Strain
A	w/o	-75.587	-0.0132	tensile--
B	w/o	-109.445	-0.0091	Tensile-
C	1.0×10^{16}	38.205	0.0262	compress+
D	5.0×10^{15}	79.504	0.0783	Compress++

The standard Radio Corporation of America cleaning process was performed to remove native oxides and other impurities on the surface of the samples prior to loading the samples

into furnace. Subsequently the samples were subjected to dry oxidation at 1150 ℃ for 2 h in O_2 and then cooled to room temperature. After oxidation, Al was sputtered onto the sample backside after HF cleaning and anti-sputtering. Finally, Al circular electrodes (ø = 300 μm) were evaporated as top-contacts to form the MOS capacitors. The C-V measurements were performed with an Agilent B1500A probe station in a shielded dark box at room temperature.

§4.3.3 Results and Discussion

Figure 4-20 shows the strain dependence of the total energy difference (E_0) of the SiO_2/4H-SiC (0001) structure. It can be seen from Figure 4-20 that when ε is at -5% to 5%, the curve shows smooth characteristics and no abnormal points. This suggests that the biaxial strain along the *a* and *b* directions may be reasonable, and the strain effect in the SiO_2/4H-SiC (0001) structure can be studied. The calculated minimum values of E_0 is located at ε=-2%, indicating that the equilibrium lattice of 2% compression could be the ground state of these strain structure. [15]

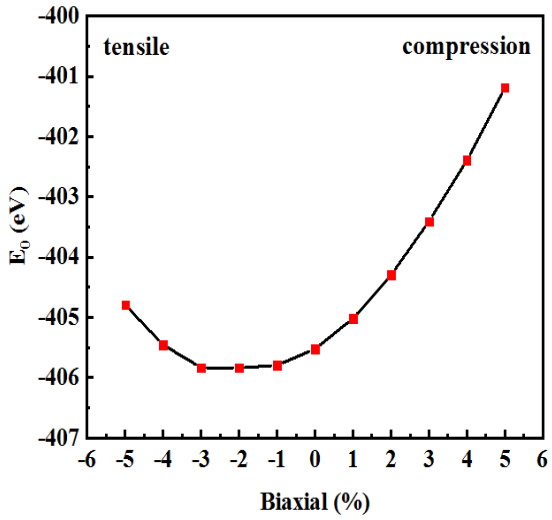

Figure 4-20. The total energy difference (E_0) in supercells with respect to the equilibrium value as a function of strain ε for SiO_2/4H-SiC(0001).

Figure 4-21 shows the bandgap (E_g) as a function of the strain ε of the SiO_2/4H-SiC(0001). It can be clearly seen from Figure 4-22 that the band gap size of the structure can be adjusted by strain. For SiO_2/4H-SiC(0001), E_g monotonically decreases when applied in a tensile and compressed state, and the maximum value, that is, the equilibrium value, is ε=-2%. In addition, a small fluctuation can be seen near the strain of about -4%, which may be caused by structural transformation.

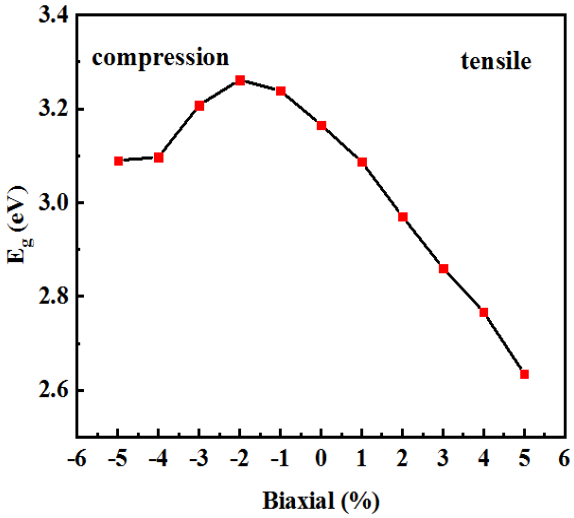

Figure 4-21. Band gap (E_g) as a function of strain ε for the SiO_2/4H-SiC(0001).

In previous experimental studies § 4.2.3, it was found that during dry thermal oxidation, the curvature of compression/tensile resulted in a change in the flat band voltage and an increase in the SiO_2/4H-SiC interface density, as shown in Figure 4-14. It is also proved that the stress affects the interface of SiO_2/4H-SiC [15]. In order to more intuitively observe the change of band gap and interface of SiO_2/4H-SiC(0001) structure under the influence of different stresses, the total density of states before and after stress (ε= ±5%, ±2%, 0%) is plotted. It can be seen from the Figure 4-21 that when the SiO_2/4H-SiC(0001) structure is in an equilibrium state where the stress is ε=-2%, it has the largest band gap value, and the interface state at this time is relatively minimum. When the stress is ε=+5%, the band gap value of SiO_2/4H-SiC(0001) structure is the smallest, and the interface state at this time is relatively largest. Therefore, as shown in Figure 4-21 and Figure 4-22, the smaller the tensile of the SiO_2/4H-SiC(0001) structure, the larger the E_g and the smaller the interface state. In contrast, the larger the SiO_2/4H-SiC(0001) structure is compressed, the smaller the E_g and the larger the interface state. Moreover, at the same degree of strain, the compression is greater than the E_g of the tensile. By comparing the trends of tensile and compression in Figure 4-22 and Figure 4-14, it is found that the calculation results are basically consistent with the results observed in the experiment, and the stress does affect the interface of SiO_2/4H-SiC by changing the band gap of the structure.

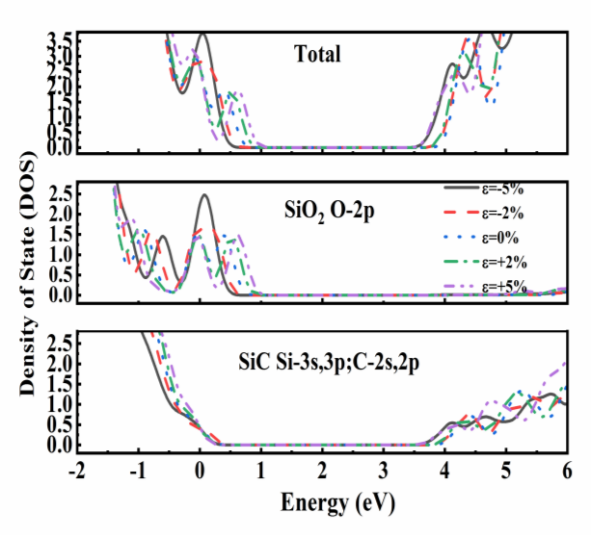

Figure 4-22. Under different stresses ε (-5%, -2%, 0, +2%, +5%), (a) The total electron density of states (DOS) of our model SiO_2/4H-SiC(0001) interface calculated with the HSE06 functional and corresponding local electronic density of states decomposed in Si, C, and O (b) O-2p in SiO_2,(c) Si-3s, 3p and C-2s, 2p in SiC.

In view of the importance of strain to changing the interface of the device, it is necessary to study the strain effect of SiO_2/4H-SiC. Next, under different stress conditions (-5%, -2%, 0%, +2%, +5%), strain effects were studied by plotting PDOS of different atoms and comparing them with the corresponding total DOS. By comparison, it is found that the band gap of SiO_2/4H-SiC structure under stress is determined by CBM and VBM. Among them, VBM is derived from the 2p state of O atom in SiO_2, and O PDOS is shown in Figure 4-22(b). Moreover, as the tensile stress increases or the compressive stress decreases, the main portion of O PDOS near the VBM gradually shifts to a region of higher energy, causing the VBM of the total DOS to move toward its transfer direction. However, CBM is derived from the 2s, 2p state of C atoms in SiC and the 3s and 3p states of Si atoms, and SiC PDOS composed of s and p orbitals of C atoms and Si atoms in SiC is shown in Figure 4-22(c). Unlike VBM, as tensile and compressive stresses increase, SiC PDOS near the CBM gradually shifts to lower energy regions, moving the CBM of the total DOS toward its transfer direction. Taking the unstrained state (ε=0%) as an example, by comparing the total DOS near the CBM with Si PDOS and C PDOS, the C 2s, 2p state, and the Si-3s and 3p states contribute to the total DOS, but C 2p And the Si 3p state dominates, as shown in Figure 4-23. Therefore, the PDOS near the CBM and VBM changes the band gap of the strain structure as the tensile and compressive movements, which in turn affects the state of the interface. This may be mainly affected by the strained SiC

substrate, resulting in a change in the in-band energy level of the SiO_2/4H-SiC structure. And this change may affect the characteristics of the MOSFET, such as mobility.

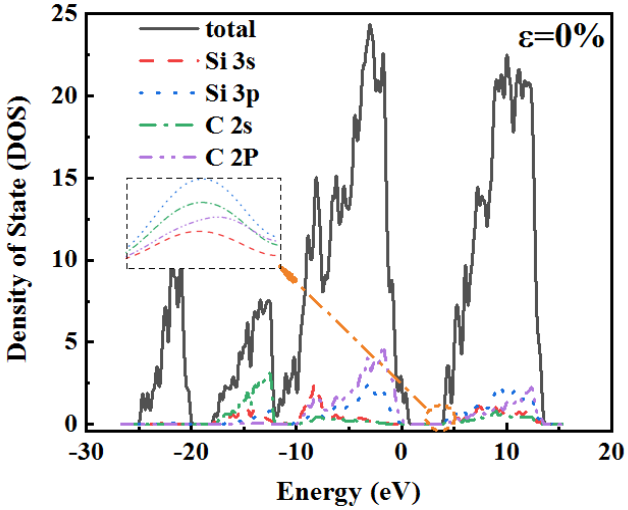

Figure 4-23. The stress is ε=0%, The total electron density of states (DOS) of our model SiO_2/4H-SiC (0001) is compared with the 2s and 2p density of states of C atoms in SiC and the 3s and 3p density of states of Si atoms.

We modelled the structure using six bilayers of 4H-SiC (1×√3) and a 10-Å thick β-tridymite SiO_2 layer, with the interface at the SiC (0001) surface, saturating all the Si dangling bonds with O. Both the top and bottom layers of the model were H terminated and the entire structure contained 43 atoms. In addition, a sufficiently thick vacuum region of 15 Å was inserted. All calculations were performed with density functional theory (DFT) in the Vienna Ab initio Simulation Package Code. We used the projector-augmented wave potential with plane wave cutoff energy of 550 eV. The k-points of 6×3×1 for Brillouin zone sampling were generated with the Monkhorst–Pack scheme. The DFT calculations were performed under the generalized gradient approximation with the exchange-correlation given by the PBE (Perdew–Burke–Ernzerhof) scheme [7, 8]. Structural optimization was performed until all the Feynman–Hellmann forces were less than 0.02 eV/Å. For the obtained structure, we investigated the electronic structures using the HSE06 hybrid functional. The calculated band gap of the 4H-SiC/SiO_2 was approximately 3.17 eV, which agreed well with the experimental value of 3.26 eV.

The first-principles calculations indicated that biaxial strain parallel to the (0001) faces lowered the conduction band leading to the formation of interfacial states D_{it} near the bottom of the conduction band [26] in 4H-SiC/SiO_2. The stress-free strain is defined $\varepsilon = (a-a_0)/a_0$ %,

where a_0 (a) denotes the lattice constants of the equilibrium (strained) crystal. $\varepsilon > 0$ ($\varepsilon < 0$) signifies the compressive (tensile) strain. The stain imposed along the a-axis varied from −5% to 5% in our calculations.

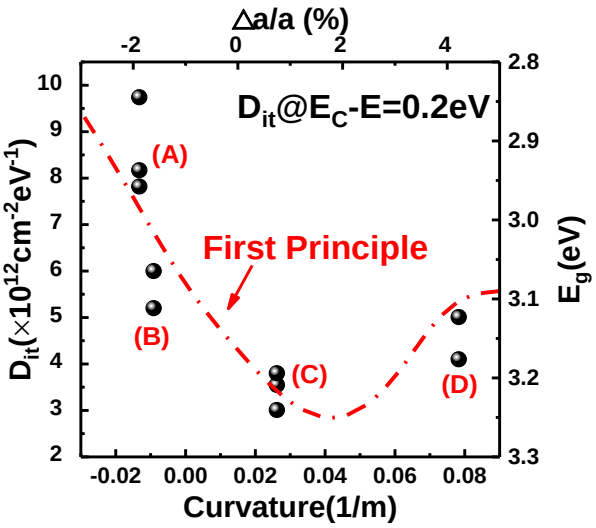

Figure 4-24. (Color online) Relationship between curvature for D_{it} with Ec−E = 0.2 eV, and fitting by first-principle calculations

According to a recent report [23], the compressive/tensile curvature increases the interface density of SiO_2/SiC during dry thermal oxidation processes, as shown in Figure 4-24. The first-principle calculations of ε and the SiC band gap are not symmetric about the axes, but distributed in the Figure with a relationship similar to that between the SiC substrate curvature and D_{it}. We note that the shape of the tensile ($\varepsilon < 0$) curvature strongly depended on the SiC band gap, whereas the change of compression ($\varepsilon > 0$) was slight and smoothed at $\varepsilon > 4$.

The wavenumber showed only a slight dependence on the shape of curvature and the distribution was discrete (see Figure 4-25). Therefore, the change of wavenumber was essentially weak in SiO_2/SiC interface, leading to a relatively lower energy level of the $\varepsilon = 2$, which is also the smallest band gap (D_{it}). As a result, the energy level of $\varepsilon = 2$ is smaller than that of $\varepsilon = -3$ and $\varepsilon = 5$ by approximately 2 eV. Hence, the D_{it} of the SiO_2/SiC interface strongly depends on the curvature as schematically illustrated (see Figure4-24). The interface defects and strain can be affected by the curvature of SiC substrate resulting in local changes of the band gap and energy levels, which finally degrade the n-MOSFET properties, such as mobility.

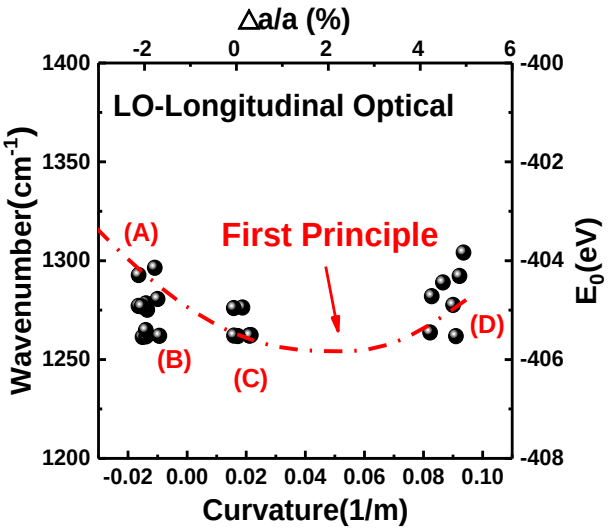

Figure 4-25. (Color online) Change of LO wavenumbers with curvature and fitting by first-principle calculations.

§4.3.3.1 TZDB Measurement

The C-V characteristics were measured with small signal amplitude of 30mV and using a voltage from -10 V to 10 V, the voltage step of 0.1V. The capacitance-voltage (C-V) characteristics measured with 100 kHz for the 4H-SiC MOS capacitors. The thickness was calculated from the accumulation capacitance of the C-V curves, which is a good agreement with the T_{ox} determined by ellipsometer, both are about 15 nm.

The thicknesses of the samples are calculated by the high frequency C-V measurement. The SiO_2 thickness of the samples is given by

$$T_{OX} = \frac{\varepsilon_0 \varepsilon_{SiO_2} A}{C_{ox}} \tag{4-3}$$

A is the area of the 4H-SiC MOS gate electrode, and ε_{SiO2} is the dielectric constant of SiO_2.

To analyze the reliability of the samples, we performed TZDB measurements at room temperature. During the TZDB measurements, a voltage was applied to the gate electrodes of the 4H-SiC MOS-CAP. The voltage was increased in +0.5-V steps until breakdown of the gate oxide. The electric field (E_{BD}) used in this experiment is given by [27]

$$E_{BD} = \frac{V_g - V_{FB}}{T_{ox}} \tag{4-4}$$

where V_g is the gate voltage, V_{FB} is the flat band voltage, which was also determined from the high-frequency C-V characteristics. A constant-current stress slightly lower than the breakdown voltage was applied to the gate oxide at room temperature to analyze the time to breakdown (T_{BD}) of the samples.

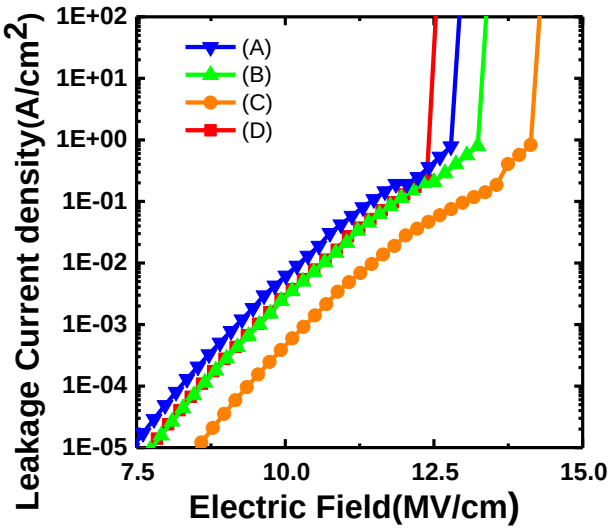

Figure4-26. Typical J-E characteristics of SiC MOS samples.

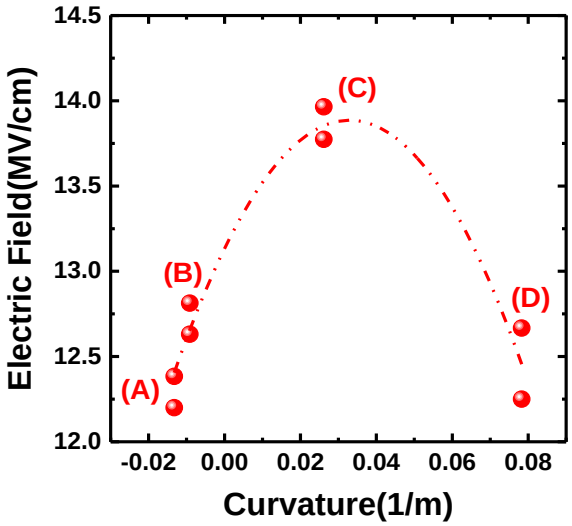

Figure 4-27. Relationship between curvature and E_{BD}.

The leakage current dependence on the density-electric field (J-E) curves for the capacitors oxidized at different curvatures are shown in Figure 4-26, the oxide breakdown characteristics obtained from TZDB measurements. At an electric field as high as about 7.5 MV/cm, the leakage current density is under 1×10^{-5} A/cm^2. Above 7.5 MV/cm, the current exponentially increases in accordance with the theoretical Fowler-Nordheim (FN) tunneling current. The steepness of the four samples oxidized at different curvatures ranged from 12.2

to 14.0 MV/cm^2. The E_{BD} of the MOS capacitor oxide at a curvature of 0.0262 1/m, i.e., the lowest stress/strain, had the highest value of 14.0 MV/cm. The stress/strain decreased the reliability of the samples, as shown in Figure 4-27 The sample (C) shows the maximum value of the E_{BD} as the lowest oxidation strain/stress, which is similar to previous reports on interfacial density.[6]

§4.3.3.2 TDDB Measurement

The Weibull distribution plots of the Q_{BD} were extracted from constant-voltage TDDB measurements for thermal oxides on the same samples as in Figure 4-28. The TDDB measurements were also performed at room temperature. The TDDB measurement results for the thermally oxidized MOS capacitors are shown in Figure 4-28. It is clearly shown that the slope of sample (A) is different with other samples, it means sample (A) has the different failure model. Beside the stress of sample (A) is largest unique one, the failure model may be related to the extreme maximum stress, the diffusion mechanism of the sample is different from other samples during the oxidation process.

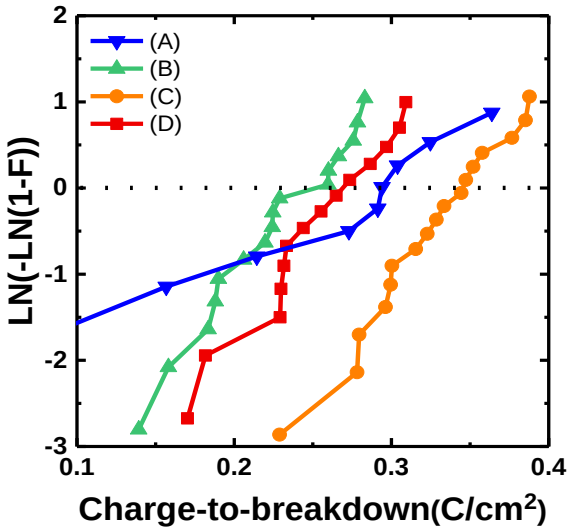

Figure 4-28. (Color online) Weibull distribution of Q_{BD} obtained from TDDB measurements of SiC MOS capacitors under different curvatures.

Besides the Q_{BD} values at thermal oxides cumulative failure rate of 63.2% for the different radius samples on the 4H-SiC were also analyzed. The value of Q_{BD} was also greatest, 0.34 C/cm^2, when the sample was formed at a curvature of 0.0262 1/m (sample C), i.e., the lowest stress/strain on the 4H-SIC wafer. The Q_{BD} value at the cumulative failure rate of 63.2% was 0.34 C/cm^2. As a result, the improvement in the reliability of thermal oxides grown on the 4H-SiC Si face has been achieved during the lowest stress/strain sample.

It seems that a tensile sample B is reduced in the reliability. Furthermore, in the case of compress sample D, the Q_{BD} distribution shows a slight worst. It is also believed that the improvement in oxide reliability is related to the decrease in the interface density. During the TDDB measurements, the tensile and compress stress /strain, which are acting as strained on Si-O bonds.

Because of the different failure model of sample (A), only the oxidation temperature dependence of Q_{BD} is shown in Figure 4-29, at a failure rate 63.2% for the SiC MOS capacitors (B), (C), and (D). For the sample oxidized strain/stress, Q_{BD} decreased as the oxidation strain/stress increased. This is because the quality of the oxide layer degraded as the gate oxidation strain/stress increased. Ultimately, we can conclude that the more stress wafers as well as more strained Si-O bonds in the B ion-implantation treated sample can result in more interface density on SiO_2/SiC and worst reliability on SiO_2 oxide.

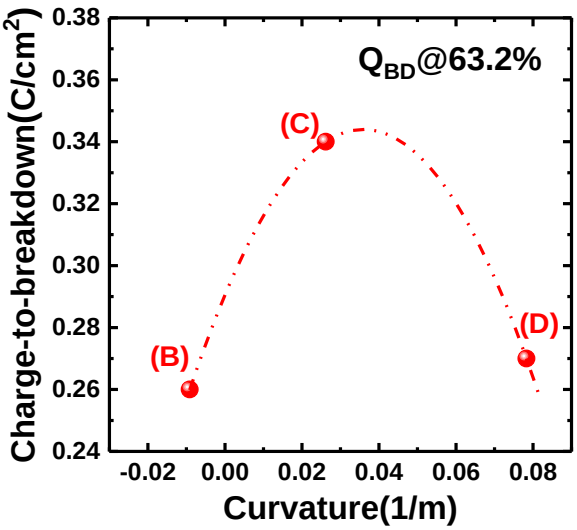

Figure 4-29. (Color online) Curvature dependence of Q_{BD} at the failure rate 63.2% [plots of (B), (C), and (D)].

§4.3.4 Conclusions

In conclusion, we studied the effect of biaxial strain on the SiO_2/4H-SiC (0001) band gap using the HSE06 hybrid function in first-principles calculations. The calculation results support previous experimental phenomena. When SiO_2/4H-SiC (0001) is compressed by 2% (ε=-2%), the structural band gap value E_g is the smallest and the interface state is the smallest as the ground state of these strain structures. In addition, the E_g value of SiO_2/4H-SiC (0001) can also be adjusted by strain, and the smaller the tensile, the larger the E_g and the smaller the

interface state. In contrast, the larger the SiO_2/4H-SiC (0001) is compressed, the smaller the E_g and the larger the interface state. Moreover, at the same degree of bending, the compression is greater than the tensile E_g. In addition, small fluctuations seen around a strain of about -4% may be caused by structural transformation. In addition, the study also found that the O-2p state in SiO_2 and the C-2p and Si-3p states in SiC cause changes in the strain structure band gap by affecting VBM and CBM, respectively.

The band gap of SiC and its energy levels were calculated by first-principle calculations, and the energy levels (E_0) of the samples related to the lattice constants of the SiC crystal, indicating that stress mainly affected the SiO_2/SiC interface. Furthermore, we studied E_{BD} and Q_{BD} by I-V measurements. The curvature of the epitaxy wafers was characterized by a thin film stress measurement system. The excessive compressive/tensile curvature, induced by stress/strain, decreased reliability of SiO_2 films, expressed by E_{BD} and Q_{BD} during dry thermal oxidation processes. Furthermore, the sample with optimal reliability was obtained for the oxide formed at a curvature of 0.0262 1/m, i.e., the lowest stress/strain. This finding is consistent with previous reports concerning by interface density, which is also demonstrated by the first-principle calculations. We suggest that a “stress free” oxide film might be the best choice for SiC-MOSFET applications. These results will be useful for industrial applications of SiC and SiC-based devices and practical epitaxy wafer selection.

§4.4 References

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Chapter 5: Conclusion and Future Works

§5.1 Summary and Conclusions

With the development of silicon carbide material processing technology in recent decades, 4H-SiC Schottky barrier diodes and MOSFETs have already entered the stage of commercialization. However, the current market share of silicon carbide devices is not so high due to their high manufacturing cost of silicon carbide devices makes the market price of silicon carbide devices which is exceed 10 times that of silicon-based devices; on the other hand, it is the unreliability of silicon carbide devices, especially for MOSFET devices in circuits that are often operated under high-frequency switching. Since the successful development of 4H-SiC devices, it has faced many problems such as how to obtain a higher channel mobility, a higher reliability gate oxide film, and whether it can maintain stable operation after receiving a stress impact in a complex circuit. In general, improving the channel mobility can be solved by optimizing the manufacturing process, such as a dense oxide layer, the use of NO annealing and a low-defect SiC / SiO_2 interface, etc. To btain a gate oxide with higher reliability requires a special structure designed to shield the excessively high electric field strength in the oxide layer; and the reliability of the device after receiving stress in the circuit is an important indicator for evaluating whether a power system can maintain stable operation for a long time. In short, before silicon carbide based devices can truly replace silicon-based devices in electronic and electronic systems, these problems must be solved well.

The main research work of the gate oxide process and reliability in this paper are as follows:

(1) Traditional Si materials, because the activation energy of their Si-Si bond is only 1.23 eV, during the oxidation process, the oxidation temperature generally does not exceed 1200^{o}C. Compared with silicon devices, silicon carbide has a higher activation energy, 3.12 eV, and requires an oxidation temperature of more than 1200^{o}C. For this problem, we confirmed that the optimal D_{it} was obtained for the sample oxidized at 1450^{o}C in the energy range 0.2–0.6 eV below the conduction band edge of SiC. However, there was a trade-off

between D_{it} and reliability, the sample oxidized at 1250^{o}C showed the most reliable character of those tested.

(2) For reduced the tradeoff between interface density and reliability on oxidation temperature, NO anneal is applied for post oxidation anneal (POA). It is suggest that the interface state density reduces when the POA temperature was elevated or the POA time was extended. We also worked that the effects of NO annealing temperature and time on the reliability of 4H-SiC MOS gate oxide. And from the results of field-to-breakdown (E_{BD}) and charge-to-breakdown (Q_{BD}), find it is effectively improving the insulation properties and reliability of gate oxide by high temperature NO annealing. During the further results, we found that the reduction of D_{it} is mainly attribute to NO annealing and higher temperature, not only NO but also Ar annealing, is proof to improve the quality of oxide layer near the SiO_2/SiC interface and enhance the effect of NO annealing.

(3) In this paper, by commercial silicon carbide epitaxial material, the defects on the interface state and reliability of the gate oxide film are investigated. The effect of grinding-induced stress on interface state density of SiC/SiO_2 was investigated and also calculated by first-principle calculations, and the energy levels (E_0) of the samples related to the lattice constants of the SiC crystal, indicating that stress mainly affected the SiO_2/SiC interface. Furthermore, we studied the excessive compressive/tensile curvature, induced by stress/strain, decreased reliability of SiO_2 films, expressed by E_{BD} and Q_{BD} during dry thermal oxidation processes. We suggest that a “stress free” oxide film might be the best choice for SiC-MOSFET applications. These results will be useful for industrial applications of SiC and SiC-based devices and practical epitaxy wafer selection.

§5.2 Suggestion for Future Works

In the work, a high-temperature gate oxide process with good gate-oxygen interface performance and high reliability is proposed. The 4H-SiC epitaxial wafer is analyzed for research the relationship between the stress of the wafer and gate-oxygen interface state and its reliability. The first-principles calculation is also applied to confirm the experiment result. However, there are still the following issues that are worth further in-depth discussion:

(1) Although through the NO gas POA, we solved the tradeoff of the oxidation temperature on the interface state and reliability; however, due to the annealing of NO, the

flat band voltage drifted in the negative direction to the negative voltage, making the threshold voltage of the MOSFET device unable to fit the expectations of the power device, that is 3-5V.

(2) We conducted a static test of the reliability of TDDB for gate oxygen under extreme electric fields, but we hope to establish a simple device screening method to eliminate the risk of failure caused by material defects, stress and process problems.

(3) This work is based on the SiC-VDMOSFET device with planar gate-oxygen structure, and it has researched on the Si-face (0001) gate-oxygen process. The a-face ($11\bar{2}0$) gate-oxygen process for the U-groove gate oxygen structure of SiC-UMOSFET will also be valuable for future research.

Acknowledgements

After two years' study for research and full papers publication, and another half year's writing, this thesis was finally accomplished. Without of the help of many people, it could never be completed, thus here I would like to express my sincere gratitude towards them.

First and foremost, I owe my heartfelt thanks to my distinguished and cordial supervisor, Professor Jin-Ping Ao, who influenced me with his insightful ideas and meaningful inspirations, guided me with practical academic advice and feasible instructions, and enlightened me while I was confused during the writing procedure. His thought-provoking comments and patiently encouragements are indispensable for my accomplishment of this thesis. My selection of interface state and reliability as the theoretical framework is deeply motivated by his profound knowledge. Without his dedicated assistance and insightful supervision, this thesis would have gone nowhere.

Then, my faithful appreciation also goes to the prestigious and distinguished Director of High-Frequency High-Voltage Device and Integrated Circuit R&D Centre in Institute of Microelectronics of Chinese Academy of Sciences, Professor Zhi Jin, whose splendid and diversified advices have empowered me with solid language capability and upright academic attitude. I would like to gratefully acknowledge Department of High-Frequency High-Voltage Device and Integrated Circuit R&D Centre, Faculty of Institute of Microelectronics, Chinese Academy of Sciences for providing the resources and needs during the thesis. I would like to extend my appreciation to Mr. Atsushi Kamada for him unconditional help during this research.

Ultimately, thanks go to my parents who are my mentor and guardian from the very beginning in primary school. Without their refined education and care, I could never grow up in such a joyous and cosy environment nor have the courage to confront any obstacles on my way to success.

Publication List

Scientific Papers

1) **Hengyu Xu**, Caiping Wan, Bo Li, Huiping Zhu and Jin-Ping Ao, Influence of curvature induced stress on first principle calculation and the reliability of 4H-SiC (0001) thermally grown SiO_2 gate oxide, Microelectronics Reliability, Vol. 100–101, pp 113317 (2019).

2) **Hengyu Xu**, Caiping Wan and Jin-Ping Ao, Reliability of 4H-SiC (0001) MOS Gate Oxide by NO Post-Oxide-Annealing, Materials Science Forum, Vol. 954, pp 109-113, (2019).

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