112 Gb/s PAM-4 Silicon Photonics Receiver Integrated with SiGe-BiCMOS Linear TIA

Daisuke Okamoto, Yasuyuki Suzuki, Koichi Takemura, Junichi Fujikata, and Takahiro Nakamura

***Abstract*—We have developed a silicon photonics receiver integrated with a SiGe-BiCMOS linear transimpedance amplifier (TIA) using the flip-chip bonding technology to assist in resolving the I/O bottleneck problem in inter-chip data communication. The proposed device demonstrated optical 112 Gb/s four-level pulse amplitude modulation (PAM-4) operations and clear eye openings without any equalization for the pseudorandom binary sequence $2^{15} - 1$ signal. The 3 dB bandwidth and transimpedance gain were designed to be 37.1 GHz and 60.1 dBΩ, respectively, at a supply voltage of 3.3 V. The consumption current of the linear TIA was 95.1 mA, and it resulted in a power consumption of 314 mW (2.8 pJ/bit). A linear TIA circuit is a key technology for PAM-4 operation; therefore, we discussed the linearity of our receiver response through eye diagrams and simulation. The measured eye diagrams agreed with the simulation results, and the proposed device maintained a linear response for up to 450 $\mu A_{p\text{-}p}$ input current. In addition, its operation rate of 112 Gb/s is the highest operation rate reported for a silicon photonics PAM-4 receiver based on flip-chip 3D integration with a germanium photodetector and a SiGe-BiCMOS linear TIA.**

***Index Terms*— Linear amplifier, optical interconnects, optical receivers, optoelectronic integrated circuit, PAM-4, SiGe-BiCMOS, silicon photonics.**

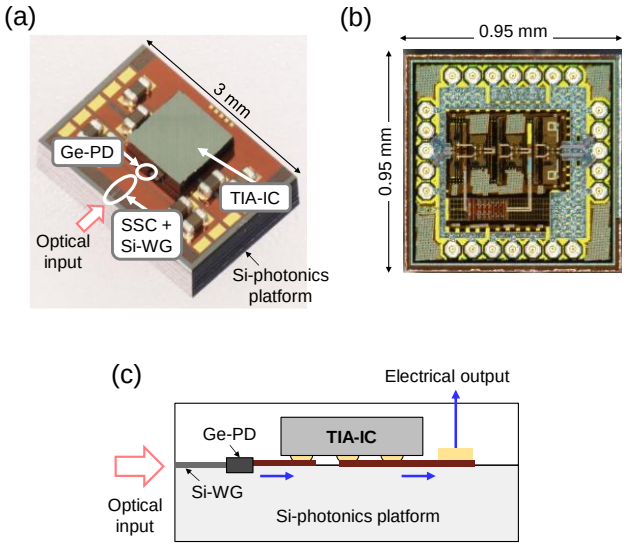

Fig. 1. Photographs of (a) the fabricated silicon photonics receiver chip and (b) the SiGe-BiCMOS TIA chip. (c) Schematic cross section of the receiver with description of the main components.

I. Introduction

THE total amount of worldwide data generation is expected to reach 847 ZB/year in 2021 due to the recent advances in the Internet of Things technologies [1]. Because machine learning and big data analysis require massive computational power, parallel computations are performed by accelerator clusters consisting of GPUs or FPGAs with a large I/O bandwidth of over 1 Tb/s in data centers or high-performance computers [2], [3]. However, switch ASICs connecting those processors require tens of Tb/s of total aggregate bandwidth [4]. As a result, we are facing an I/O bottleneck problem in inter-chip data communication.

Silicon photonics is a promising technology to solve these bottlenecks and implement high-performance, low-power, reliable, and highly integrated optical interconnects that satisfy the growing demands of data centers [5]–[7]. It enables mass production and cost reduction using the mature CMOS process technology for large-area wafers [8]. Therefore, we proposed a chip-scale optical transceiver based on the silicon photonics technology [6] and demonstrated non-return-to-zero (NRZ) 25 Gb/s × four-channel operations at 85 °C with a 28 nm CMOS transimpedance amplifier (TIA) in our previous work [9].

Four-level pulse amplitude modulation (PAM-4) has been proposed [10], [11] to meet the strong demand for a receiver with a wider bandwidth [12]–[14]. Optical interconnects based on PAM-4 can increase the transmission bandwidth while maintaining the size and cost of receivers and transmitters. We targeted over 100 Gb/s/channel optical PAM-4 transceivers to realize a silicon photonics-embedded interposer with 51.2 Tb/s total bandwidth by integrating 512 channels [15].

In this study, we developed a silicon photonics receiver

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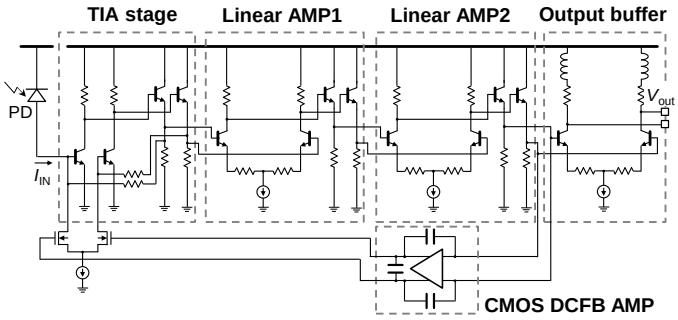

Fig. 2. Block diagram of the TIA circuit based on the SiGe-BiCMOS technology.

integrated with a SiGe-BiCMOS linear TIA using flip-chip bonding technology. In addition, we discussed the circuit designs of the linear TIA and the receiver characteristics for 112 Gb/s PAM-4 (56 Gbaud) operations.

II. 112 Gb/s Optical Receiver Based on Silicon Photonics

A. Optical Receiver Chip Design

Photographs of the proposed optical receiver that was fabricated using silicon photonics technology and a SiGe-BiCMOS TIA chip are displayed in Figs. 1(a) and (b), respectively. Fig. 1(c) illustrates the schematic cross section of the receiver. We fabricated a silicon photonics platform using 40 nm node CMOS technology with a 300 mm silicon-on-insulator wafer [8]. A tapered spot-size converter (SSC) with a 160 nm tip width, a silicon waveguide (Si-WG) with of 350 nm width, and a waveguide-type germanium photodetector (Ge-PD) with a lateral PIN junction [16], [17] were integrated on the platform chip. We measured optical frequency response and electrical S-parameters (S_{11}, return loss) to make the equivalent circuit model of the Ge-PD. The PD showed 40 GHz bandwidth and 0.85 A/W responsivity. Circuit parameters were extracted from those results by fitting, and the intrinsic capacitance was approximately 10 fF.

We employed hybrid 3D integration for our receiver wherein the electronic and photonic chips were fabricated separately and then stacked by flip-chip bonding [9], [15], [18]. A 0.95 mm × 0.95 mm SiGe-BiCMOS TIA chip was mounted onto the 3 mm × 2.1 mm silicon photonics platform chip by Au-bump thermosonic bonding. The diameter and height of the Au bumps were approximately 60 μm and 25 μm, respectively. We utilized hybrid integration to select optimum processes for the electronic and photonic chip independently while considering both performance and cost [5]. Although wire-bonding is widely used for optoelectronics integration [10], [12]–[14], the wire inductance of several hundred pH limits the TIA design; in addition, the electrode pads can only be placed in a row at the chip periphery. In contrast, flip-chip bonding exhibits less parasitic inductance and is suitable for dense multi-channel integration wherein the pads are arranged in two dimensions [11], [15], [18]. Because power integrity is vital for high-speed

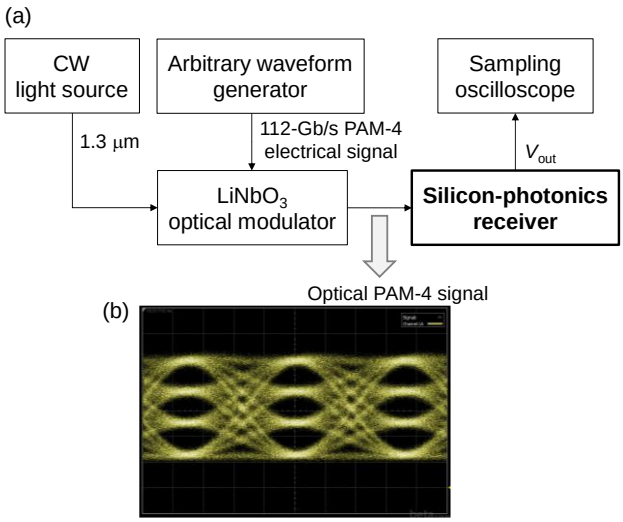

Fig. 3. (a) Block diagram of the measurement setup to investigate the receiver characteristics. (b) Eye diagram of the 112 Gb/s optical PAM-4 signal input into the receiver.

operations, decoupling capacitors of 0.1 μF were mounted in the close vicinity of the TIA chip. Optical PAM-4 signals were input into the Si-WG via SSC and converted to current signals in the Ge-PD. The current signals were linearly amplified to the PAM-4 electrical voltage signals in the TIA.

B. Circuit Design of Linear TIA

As PAM-4 transmission has a minimum of 4.8 dB penalty in signal-to-noise ratio compared to NRZ transmission, the TIA circuit requires broad bandwidth and a large output amplitude to achieve clear eye openings. In addition, linearity is significant for converting four-level optical signals into four-level electrical signals to obtain three equivalent eye openings. The SiGe-BiCMOS technology is suitable for meeting these requirements for high-speed optical PAM-4 receivers.

Our TIA-IC was implemented in the SiGe-BiCMOS technology because it provides high-speed SiGe bipolar transistors (f_t/f_{max} = 300/345 GHz) and 180 nm CMOS circuit integration. The block diagram of the linear TIA is given in Fig. 2. The photocurrent from the Ge-PD was input into the TIA stage with a feedback resistance of 250 Ω. The TIA output signals were converted to differential signals at the first linear amplifier (Linear AMP1); this was followed by the second differential linear amplifier (Linear AMP2) and a 50 Ω output buffer with 37.6 μm × 37.6 μm spiral inductors. This circuit had no variable gain amplifier (VGA), but Gilbert-cell–based VGA [19] can be implemented to extend the dynamic range. The 3 dB bandwidth and transimpedance gain Z_T, which is defined as $Z_T = \Delta V_{OUT}/\Delta I_{IN}$, were simulated to be, respectively, 37.1 GHz and 60.1 dBΩ at a supply voltage of 3.3 V. The offset of the input current of up to 900 μA in the TIA stage was canceled by a DC feedback (DCFB) loop with a low cutoff frequency of 14.2 kHz. The DCFB amplifier was designed based on CMOS to realize a compact and low power consumption circuit.

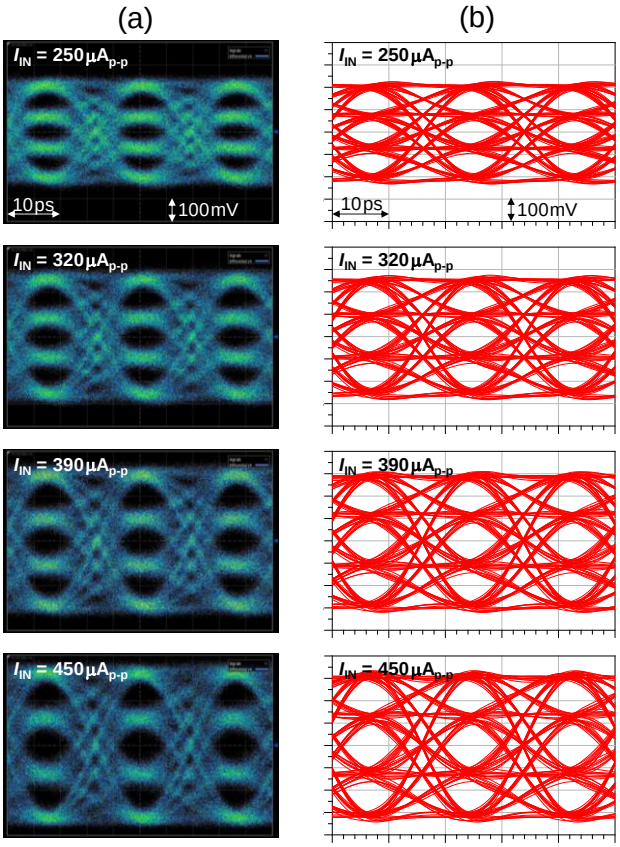

Fig. 4. (a) Measured and (b) simulated 112 Gb/s PAM-4 eye diagrams of the differential electrical outputs of the receiver at I_{IN} = 250, 320, 390, and 450 μA$_{p-p}$ (10 ps/div, 100 mV/div).

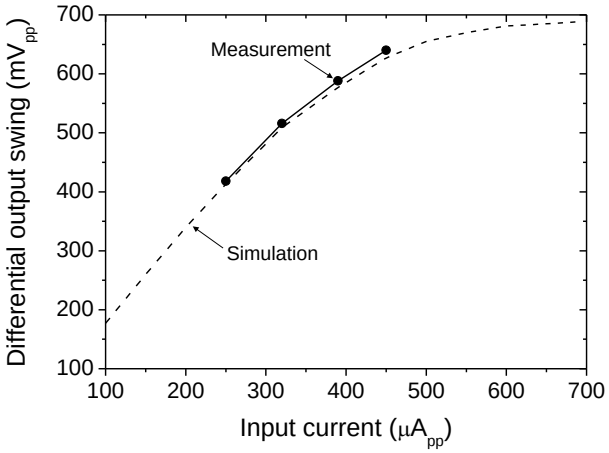

Fig. 5. Input current dependence of the measured and simulated 112 Gb/s PAM-4 eye diagrams on the differential electrical outputs of the receiver.

TABLE 1
CHARACTERISTICS OF SILICON-PHOTONICS RECEIVERS INTEGRATED WITH Ge-PDs AND SiGe-BiCMOS TIAs

	This work	[10]	[14]	[11]
IC technology	SiGe-BiCMOS 180 nm	SiGe-BiCMOS 55 nm	SiGe-BiCMOS 180 nm	SiGe-BiCMOS 55 nm
Photodiode	Waveguide Ge-PD	Waveguide Ge-PD	Waveguide Ge-PD	Waveguide Ge-PD
Integration architecture	3-D (Flip-chip)	Wire-bonded	Wire-bonded	3-D (Flip-chip)
Data rate	112 Gb/s PAM-4	106 Gb/s PAM-4	100 Gb/s NRZ	53 Gb/s NRZ
Test pattern	PRBS $2^{15}-1$	PRBS $2^{9}-1$	PRBS $2^{15}-1$	PRBS $2^{31}-1$
Power (Pj/bit)	2.8	1.5	3.5	1.1*

*Including only front-end circuit.

III. EXPERIMENTAL RESULTS AND DISCUSSION

We investigated the characteristics of the proposed receiver for 112 Gb/s optical PAM-4 input signals using the experimental setup described in Fig. 3(a). The optical PAM-4 signals in 1310 nm wavelength were generated by the iXblue 56 Gbaud PAM-4 reference transmitter ($LiNbO_3$ optical modulator) driven by the Keysight M8199A arbitrary waveform generator (AWG). To investigate the linearity of the receiver, the input optical signal must have linear signal levels and three equal eye openings. Level separation mismatch ratio (R_{LM}) is a metric for the linearity of the transmitter and is defined by

$$R_{LM} = \frac{\min(V_3-V_2, V_2-V_1, V_1-V_0)}{\frac{V_3-V_0}{3}}, \quad (1)$$

where V_i (i = 0, 1, 2, 3) is the individual signal level in PAM-4 [20]. The generated optical signal had three equivalent eye openings and its level separation mismatch ratio (R_{LM}) was 0.98, as displayed in Fig. 3(b). The outer extinction ratio was 5.5 dB at the pseudorandom binary sequence (PRBS) $2^{15}-1$ pattern. The optical signal was input into the receiver chip via an optical fiber attached to the chip edge with a coupling loss of about 3 dB. The differential electrical outputs of the receiver were measured with a sampling oscilloscope through a 67 GHz GSGSG (Ground-Signal-Ground-Signal-Ground) probe and a 20 cm long RF coaxial cable. DC probes were used to apply a TIA-IC power supply of 3.3 V and a PD bias of 5 V. The current consumption of the linear TIA was 95.1 mA, and the resulting power consumption was 314 mW (2.8 pJ/bit). To analyze the linearity of the receiver output, the input optical power was controlled via a variable optical attenuator.

The measured 112 Gb/s PAM-4 eye diagrams of the differential electrical outputs of the receiver with respective input current amplitude I_{IN} = 250, 320, 390, and 450 μA$_{p-p}$ are displayed in Fig. 4(a). Fig. 4(b) provides the simulated waveforms for the same input conditions, including the 20 cm RF cable. These input currents corresponded to the respective optical modulation amplitude P_{IN} = –5.3, –4.2, –3.4, and –2.8 dBm defined at the input of the Ge-PD. Measured stress eye closure quaternary (SECQ) values for the eye diagrams were respectively 3.0, 2.4, 1.9, and 1.6 dB. The SECQ metric for receiver electrical signals has the same definition as transmitter dispersion eye closure quaternary (TDECQ) for transmitter optical signals. The symbol error rate (SER) was 3.0×10^{-4} calculated from measured eye heights and noise figures using the sampling oscilloscope at P_{IN} = –5.8 dBm, and the minimum sensitivity for SER < 4.8×10^{-4} was estimated to be approximately –6 dBm. The integrated input-referred noise current was 4.3 μA$_{rms}$ calculated from measured output noise and the transimpedance gain [21]. The measured waveforms revealed clear PAM-4 eye openings without any equalization; they were compatible with the simulation results as well. The R_{LM} of the measured eye diagrams were respectively 0.96, 0.95,

0.94, and 0.91 for the 250–450 $\mu A_{p\text{-}p}$ inputs. Although the middle eye opening was slightly larger than the upper and lower eyes for I_{IN} = 450 $\mu A_{p\text{-}p}$ due to gain saturation, the upper and lower eyes also maintained sufficient openings. The input current dependence of the measured and simulated output amplitude are plotted in Fig. 5. Herein, output swing is defined as the difference between the highest and lowest levels of the PAM-4 eye diagram. This linear TIA was designed to linearly respond to the input current up to 450 $\mu A_{p\text{-}p}$, and the simulated differential electrical output swing for the 450 $\mu A_{p\text{-}p}$ input was 630 $mV_{p\text{-}p}$. The measured output amplitudes were compatible with the simulation results within a difference of 15 mV; their corresponding slopes were compatible as well.

Table I summarizes the characteristics of the silicon photonics receivers integrated with Ge-PDs and SiGe-BiCMOS TIAs. Previously, 106 Gb/s PAM-4 [10] and 100 Gb/s NRZ [14] transmissions have been reported with wire-bonding integration, and flip-chip integration was utilized to develop the 53 Gb/s × four-channel optical transceiver [11]. We successfully demonstrated the 112 Gb/s PAM-4 clear eye openings signal for a longer PRBS $2^{15} – 1$ test pattern than [10] by leveraging the linear response of the receiver and flip-chip 3D integration with less parasitic inductance and capacitance. This is the highest operation rate for a silicon photonics PAM-4 receiver based on 3D integration with a Ge-PD and a SiGe-BiCMOS linear TIA to the best of our knowledge.

IV. Conclusion

In this study, we developed a silicon photonics receiver integrated with a SiGe-BiCMOS linear TIA using flip-chip bonding technology. We successfully demonstrated optical 112 Gb/s PAM-4 (56 Gbaud) operations and clear eye openings in the proposed device without any equalization. The linear response of the proposed device was maintained for up to 450 $\mu A_{p\text{-}p}$ input current in both measurement and simulation waveforms. This is the highest reported operation rate for a silicon photonics PAM-4 receiver based on 3D integration. These results and performance parameters verify the ability of our receiver to be applied to a densely integrated silicon photonics-embedded interposer.

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